

EIA Standard Board Layout Drawing for BGA, CCGA, CSP, and QFN

April 2016





Figure 1: Suggested Board Layout of Soldered Pads for BGA Packages

Notes:

- Table 2a through Table 6 on page 11 contain the recommended guidelines for board layout soldered pad dimensions for the following Microsemi packages (including pad dimension for prototyping socket accordingly): CS (Chip Scale BGA, 0.8 mm pitch), FG (Fine Pitch BGA, 1.00 mm pitch), BG (Plastic Ball Grid Array, 1.27 mm pitch, CG (Ceramic Column Grid Array, 1.27 mm pitch), CG adapter socket, and QN (Quad Fine Pitch No-Lead QFN, 0.5 mm pitch).
- 2. For E-tec prototyping socket soldering, Microsemi recommends using non-silver type solder paste with 6 mils thickness.



Dim.	uCS81	uCS81	CS81	CS121	CS196	CS201	CS281
Component Land Pad Diameter (SMD)	0.33	0.33	0.35	0.35	0.35	0.35	0.35
Solder Land Diameter (SL)	0.23	0.23	0.25	0.25	0.25	0.25	0.25
Solder Mask Opening Diameter (SM)	0.33	0.33	0.35	0.35	0.35	0.35	0.35
Solder Ball Land Pitch (BL)	0.4	0.4	0.50	0.50	0.50	0.50	0.50
Line Width Between Via and Solder Land (LW)	Via In Pad	Via In Pad	0.15 to 0.20				
Distance Between Via and Solder Land (DL)	Via In Pad	Via In Pad	0.353	0.353	0.353	0.353	0.353
Via Land Diameter (VL)	See Land Diameter	See Land Diameter	0.200 to 0.250				
Through Hole Diameter (TH)	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125	0.100 to 0.125
Line Width (L)	0.075	0.075	0.075	0.075	0.075	0.075	0.075
Line Width (L) If Inner Outer Via's Staggered.	NA	NA	NA	NA	NA	NA	0.10
Line Space (S)	0.085	0.085	0.085	0.085	0.085	0.085	0.085
Pad Array	Full	Full	Full	Full	Full	Perimeter	Perimeter
Pad Matrix	6 × 6	9 × 9	9 × 9	11 × 11	14 × 14	15 × 15	19 × 19
Periphery Rows	-	-	-	-	-	4, 1, 5	2, 2, 7

Table 1a: Recommended PCB design guidelines for Microsemi CS (0.5 mm pitch BGA) package

Table 2a: Recommended PCB Design Guidelines for Microsemi CS (0.8 mm Pitch BGA) Package

Dimension	CS49	CS128	CS180
Component Land Pad Diameter (SMD)	0.35	0.35	0.35
Solder Land Diameter (SL)	0.30	0.30	0.30
Solder Mask Opening Diameter (SM)	0.45	0.45	0.45
Solder Ball Land Pitch (BL)	0.80	0.80	0.80
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.56	0.56	0.56
Via Land Diameter (VL)	0.50	0.50	0.50
Through Hole Diameter (TH)	0.25	0.25	0.25
Pad Array	Full	Perimeter	Perimeter
Pad Matrix	7 × 7	12 × 12	14 × 14
Periphery Rows	-	4	5



Power Matters."

Table 2b: Recommended PCB Design Guidelines for Prototyping Socket of CS Package

Dimension	CS49 Prototyping Socket. Microsemi P/N: SE-CS49-H	CS128 Prototyping Socket. Microsemi P/N: SE-CS128-H	CS180 Prototyping Socket. Microsemi P/N: SE-CS180-H
Socket Pin Diameter	0.45	0.45	0.45
Solder Land Diameter (SL)	0.50	0.50	0.50
Solder Mask Opening Diameter (SM)	0.60	0.60	0.60
Solder Ball Land Pitch (BL)	0.80	0.80	0.80
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.56	0.56	0.56
Via Land Diameter (VL)	0.50	0.50	0.50
Through Hole Diameter (TH)	0.25	0.25	0.25
Pad Array	Full	Perimeter	Perimeter
Pad Matrix	7 × 7	12 × 12	14 × 14
Periphery Rows	_	4	5

Table 3a: Recommended PCB Design Guidelines for Microsemi FG (1.00 mm Pitch BGA) Package

Dimension	FG144	FG256	FG324	FG484 23×23	FG484	FG676	FG896	FG1152
Component Land Pad Diameter (SMD)	0.40	0.45	0.45	0.45	0.45	0.45	0.45	0.45
Solder Land Diameter (SL)	0.35	0.40	0.40	0.40	0.40	0.40	0.40	0.40
Solder Mask Opening Diameter (SM)	0.50	0.55	0.55	0.55	0.55	0.55	0.55	0.55
Solder Ball Land Pitch (BL)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land Diameter (VL)	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60
Through Hole Diameter (TH)	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
Pad Array	Full	Full	Full	Full	Perimeter	Full	Full	Full
Pad Matrix	12 × 12	16 × 16	18 × 18	22 × 22	26 × 26	26 × 26	30 × 30	34 × 34
Periphery Rows	_	-	_	-	5 + 8 × 8	_	_	_



Dimension	FG144 Prototypin g Socket. Microsemi P/N: SE-FG144- H	FG256 Prototypin g Socket. Microsemi P/N: SE- FG256-HU	FG324 Prototypin g Socket. Microsemi P/N: SE-FG324- H	FG484 23×23 Prototypin g Socket. Microsemi P/N: SE-FG484- S-H	FG484 Prototypin g Socket. Microsemi P/N: SE-FG484- H	FG676 Prototypin g Socket. Microsemi P/N: SE- FG676-H	FG896 Prototypi ng Socket. Microsem i P/N: SE-FG896	FG1152 Prototypi ng Socket. Microse mi P/N: SE- FG1152
Socket Pin Diameter	0.45	0.45	0.45	0.45	0.45	0.45	0.45	0.45
Solder Land Diameter (SL)	0.58	0.58	0.58	0.58	0.58	0.58	0.58	0.58
Solder Mask Opening Diameter (SM)	0.73	0.73	0.73	0.73	0.73	0.73	0.73	0.73
Solder Ball Land Pitch (BL)	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15	0.15	0.15	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.70	0.70	0.70	0.70	0.70	0.70	0.70	0.70
Via Land Diameter (VL)	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.60
Through Hole Diameter (TH)	0.30	0.30	0.30	0.30	0.30	0.30	0.30	0.30
Pad Array	Full	Full	Full	Full	Perimeter	Full	Full	Full
Pad Matrix	12 × 12	16 × 16	18 × 18	22 × 22	26 × 26	26 × 26	30 × 30	34 × 34
Periphery Rows	_	_	_	_	5 + 8 × 8	_	_	_

Table 3b:	Recommended	PCB Design	Guidelines f	for Prototyping	Socket of FG Package
10010 00.		. • • • • • • • • • • • • • • • • • • •	o al a o li li o o l		

Table 4a: Recommended PCB Design Guidelines for Actel BG (1.27 mm Pitch BGA) Package

Dimension	BG272	BG313	BG329	BG456	BG729
Component Land Pad Diameter (SMD)	0.63	0.63	0.63	0.63	0.63
Solder Land Diameter (SL)	0.58	0.58	0.58	0.58	.058
Solder Mask Opening Diameter (SM)	0.73	0.73	0.73	0.73	0.73
Solder Ball Land Pitch (BL)	1.27	1.27	1.27	1.27	1.27
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.80	0.80	0.80	0.80	0.80
Via Land Diameter (VL)	0.60	0.60	0.60	0.60	0.60
Through Hole Diameter (TH)	0.30	0.30	0.30	0.30	0.30
Pad Array	Perimeter	Staggered	Perimeter	Perimeter	Full
Pad Matrix	20 × 20	25 × 25	23 × 23	26 × 26	27 × 27
Periphery Rows	4 + 4 × 4	-	4 + 5 × 5	5 + 6 × 6	-



Power Matters."

Table 4b: Recommended PCB Design Guidelines for Prototyping Socket of BG Package

Dimension	BG272 Prototyping Socket. Microsemi P/ N: SM-BG272-B	BG313 Prototyping Socket. Microsemi P/ N: SM-BG313-B	BG329 Prototyping Socket. Microsemi P/ N: SM-BG329-B	BG456 Prototyping Socket. Microsemi P/ N: SM-BG456-B	BG729 Prototyping Socket. Microsemi P/ N: SE-BG729
Socket Pin Diameter	0.55	0.55	0.55	0.55	0.55
Solder Land Diameter (SL)	0.58	0.58	0.58	0.58	.058
Solder Mask Opening Diameter (SM)	0.73	0.73	0.73	0.73	0.73
Solder Ball Land Pitch (BL)	1.27	1.27	1.27	1.27	1.27
Line Width Between Via and Solder Land (LW)	0.15	0.15	0.15	0.15	0.15
Distance Between Via and Solder Land (DL)	0.80	0.80	0.80	0.80	0.80
Via Land Diameter (VL)	0.60	0.60	0.60	0.60	0.60
Through Hole Diameter (TH)	0.30	0.30	0.30	0.30	0.30
Pad Array	Perimeter	Staggered	Perimeter	Perimeter	Full
Pad Matrix	20 × 20	25 × 25	23 × 23	26 × 26	27 × 27
Periphery Rows	4 + 4 × 4	-	4 + 5 × 5	5 + 6 × 6	-



Table 5: Recommended PCB Design Guidelines for Microsemi CCGA (Ceramic Column Grid Array or CG) Package

The recommended guidelines for the 1.27 mm pitch package pertain to the Microsemi CG624 package, the CG624 to FG484 Adapter Socket, and the CG624 to FG896 Adapter Socket. The 1.00 mm pitch recommendations relate to the Microsemi CG1152 and CG1272 packages.



All dimensions are in mm unless otherwise specified.

Section	A-A	
	CG624	CG1152/1272
Diameter	1.27 mm Pitch	1.00 mm Pitch
А	0.851 mm	0.80 mm
В	0.749 mm	0.70 mm
D	0.720 mm	0.67 mm
D	0.483 mm	0.38 mm
E	0.305 mm	0.20 mm
F	0.560 mm	0.46 mm
G	0.635 mm	0.50 mm
Н	0.635 mm	0.50 mm

Notes:

- 1. Functional surface
- 2. Normal diameter at Copper/Polyimate interface with typical edge angle

Figure 2: Recommended PCB Design Guidelines for Microsemi CCGA (Ceramic Column Grid Array or CG) Package





Note: This suggested board layout is for SMD. To use NSMD, swap SL and SM dimensions. Figure 3: **Suggested Board Layout of Soldered Pads for QFN (Top) Packages**





Figure 4: Suggested Board Layout of Soldered Pads for QFN (Bottom) Packages





Figure 5: Suggested Board Layout of Soldered Pads for QFN Packages (PCB Bottom Layer) This Suggested board layout is for reduced thermal pad, NSMD, to use SMD swap SL and SM dimensions.





Figure 6: Suggested Board Layout of Soldered Pads for QFN Packages (PCB Bottom Layer), Reduced Thermal Pad

Table 6 contains the recommended guidelines for board layout soldered pad dimension for Microsemi QN(0.5 mm pitch QFN) packages only.

Dimension	QN48*	QN68*	QN108	QN132	QN180
Component Land Pad Diameter (SMD)	0.200/0.400	0.200/0.400	0.3	0.3	0.3
Solder Land Diameter (SL)	0.200/0.400	0.200/0.400	0.3	0.3	0.3
Solder Mask Opening Diameter (SM)	0.300/0.500	0.300/0.500	0.425	0.425	0.425
Solder Land To Solder Land (LL)	0.075	0.075	0.075	0.075	0.075
Solder Mask Overlap (SO)	0.0625	0.0625	0.0625	0.0625	0.0625
Solder Land Pitch (BL)	0.400	0.400	0.5	0.5	0.5
Line Width Between Via and Via Land (LW2)	N/A	N/A	0.1	0.1	0.1
Line Width Between Via out side Via Land (LW1)	0.127	0.127	0.127	0.127	0.127
Line to Via Land (LV)	N/A	N/A	0.050 - 0.100	0.050 - 0.100	0.050 - 0.100
Via Land Diameter (VL)	N/A	N/A	0.250 - 0.400	0.250 - 0.400	0.250 - 0.400
Through Hole Diameter (TH)	N/A	N/A	0.100 - 0.250	0.100 - 0.250	0.100 - 0.250
Die Attach Pad (DP)	2.920 × 2.920	2.920 × 2.920	4.700 × 4.700	5.700 × 5.700	6.300 × 6.300
Pad Array	Perimeter	Perimeter	Perimeter	Perimeter	Perimeter
Body Size	8 × 8	8 × 8	8 × 8	8 × 8	10 × 10
Periphery Rows	1	1	2	3	3

Table 6: Recommended QFN Design Guidelines

Note: *Component Land Pad and Solder Lands are rectangular, longest dimension is perpendicular to package edge.



Power Matters."

PCB Land Pattern Design File

Download the QN132 PCB Land Patter design file from Microsemi website. This can be used to assist the layout of the board. Download the file from *http://soc.microsemi.com/download/rsc/?f=PCB_QN132_DF*.

List of Changes

The following table shows the important changes made in this document for each revision.

Previous Version	Changes in Current Version	Page
55700007-7/04.16*	Table 6: Recommended QFN Design Guidelines is updated to include QN48 data (SAR 76095).	11
55700007-6/7.08*	Table 1a: Recommended PCB design guidelines for Microsemi CS (0.5 mm pitch BGA) package was updated to include uC36 data.	3
55700007-5/3.08*	Table 1a: Recommended PCB design guidelines for Microsemi CS (0.5 mm pitch BGA) package was updated to include uC81 data.	3
	Table 6: Recommended QFN Design Guidelines was updated to include QN68 data.	11
55700007-4/2.08*	Table 1a: Recommended PCB design guidelines for Microsemi CS (0.5 mm pitch BGA) package was updated to include CS201 and CS281.	3
	Figure 5:Suggested Board Layout of Soldered Pads for QFN Packages (PCB Bottom Layer) This Suggested board layout is for reduced thermal pad, NSMD, to use SMD swap SL and SM dimensions. is new.	10
	Figure 6:Suggested Board Layout of Soldered Pads for QFN Packages (PCB Bottom Layer), Reduced Thermal Pad is new.	11
	Table 6: Recommended QFN Design Guidelines was updated.	11

Note: *The part number is located on the last page of the document.



Microsemi Corporate Headquarters One Enterprise, Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113 Outside the USA: +1 (949) 380-6100 Sales: +1 (949) 380-6136 Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

© 2016 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Powerover-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at **www.microsemi.com**.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.