SmartGen Hard Multiplier Accumulator v1.0

Handbook

Actel
POWER MATTERS

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Trademarks

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Introduction

At the basic level, SgHardMultAcc (SmartGen RTAX-DSP Multiplier-Accumulator) performs a single 18x18 two's complement signed multiplication along with an addition or subtraction with the previously registered result (P_{n-1}) so that:

P_n [40:0] = P_{n-1}[40:0] +/- (A x B)

You can choose the width of the operands, whether the result can be synchronously loaded, whether one of the operands is a constant and whether any of the operands is registered. Implementation is limited to those device families that contain MATH blocks (RTAX-DSP only at this time).

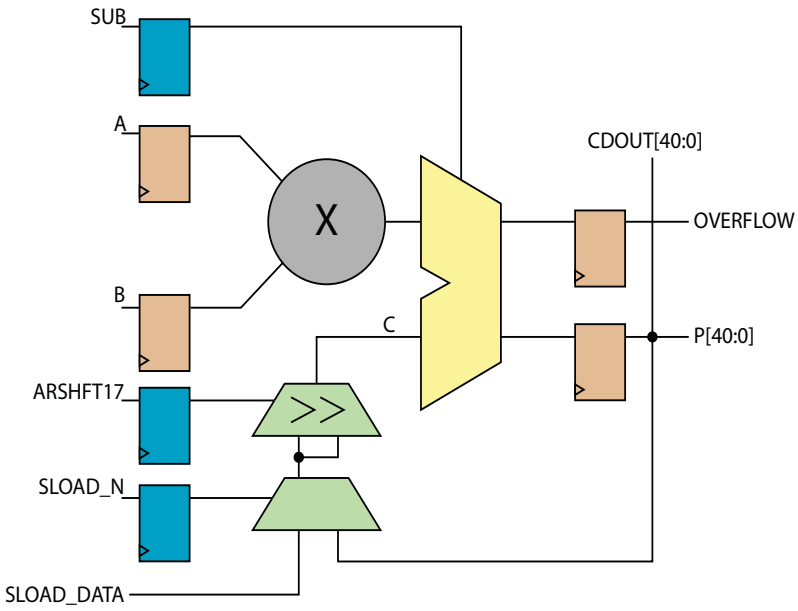

Figure 1 · SgHardMultAcc Block Diagram

The SgHardMultAcc block diagram is shown in Figure 1. Blue registers indicate control signals and brown registers are for data. Several aspects of SgHardMultAcc can be configured with a user interface that generates a structured netlist in Verilog or VHDL. For a detailed description of the user interface settings, refer to Table 2-2 on page 13.

Key Features

SgHardMultAcc has the following features:

- A structural netlist generator in Verilog or VHDL
- Configurable widths of operands A and B between 2 and 18
- Optional assignment of operand A to an 18-bit two's complement constant
- Configurable widths of operand SLOAD_DATA between 2 and 41
- Optional assignment of operand SLOAD_DATA to a 41 bit two's complement constant
- Dynamic selection of SLOAD_DATA into P[40:0] registers
- Optional operation of Arithmetic-right-shift of the previously registered result by 17 bits
- Static or dynamic selection between addition or subtraction operation

- Optional registers for A, B, SLOAD_N, ARSHFT17 or SUB with a common clock, individual active-low asynchronous clear and individual active-high enable signals
- Additional output (for cascading to the next MATH block) CDOUT[40:0], which is a copy of P[40:0]

Core Version

This handbook applies to SgHardMultAcc v1.0.

Utilization and Performance

SgHardMultAcc can be used with any devices in the RTAX-DSP family. You must create a project with Axcelerator in the Libero IDE to use the SgHardMultAcc macro. A summary of the data for SgHardMultAcc is listed in Table 1.

Table 1 · SgHardMultAcc Device Utilization and Performance

Family	FPGA Resources			Performance
	Sequential	Combinatorial	MATH	
RTAX-DSP	0	0	1	> 143 MHz

Note: Data in this table was obtained using typical synthesis and layout settings under STD Speed Grade and MIL operating conditions.

The benchmarks were obtained using the macro configuration settings shown in Table 2.

Table 2 · SgHardMultAcc Benchmark Options

Configuration Option	Setting
Function	Loadable Multiplier Accumulator (Adder/Subtractor)
Input Port A	
Use Constant	Unselected
Constant Value	N/A
Width	18
Register Port	Selected
Input Port B	
Width	18
Register Port	Selected
Input Ports SLOAD_DATA/SLOAD	
Use Constant	Not Selected
Constant Value (Hex)	N/A
SLOAD_DATA Width	41
Register SLOAD Port	Selected

Table 2 · SgHardMultAcc Benchmark Options

Configuration Option	Setting
Input Port ARSHFT17	
Arithmetic Right Shift Accumulated Data	Selected
Register Port	Selected
Input Port SUB	
Register Port	Selected
Target FPGA	
Die	RTAX4000D

1 Functional Block Description

SgHardMultAcc, shown in Figure 1 on page 5, consists of a single MATH18x18 macro configured for two's complement signed multiply operation followed by addition or subtraction with the previously registered result, as shown in Table 1-1.

Table 1-1 · SgHardMultAcc Operand Table

P_n[40:0] =	C + (A x B), when SUB = 0
	C - (A x B), when SUB = 1
CDOUT[40:0]=	P_n[40:0]
OVERFLOW	if C +/- (A x B) > 2^{40} -1, then OVERFLOW = 1
	if C +/- (A x B) < -2^{40}, then OVERFLOW = 1
	otherwise, OVERFLOW = 0

Operand C is defined in Table 1-2.

Table 1-2 · Truth Table for Propagating Data for Operand C

SLOAD_N_q	ARSHFT17_q	Operand C
0	0	SLOAD_DATA[40:0]
0	1	{{17{SLOAD_DATA[40]}}, SLOAD_DATA[40:17]}
1	0	P_{n-1}[40:0]
1	1	{{17{P_{n-1}[40]}}, P_{n-1}[40:17]}

Register Usage

All internal registers are TMR hardened to eliminate radiation-induced single-event upsets (SEU). They have a common rising-edge clock, individual active-low asynchronous clear and individual active-high enable signals. The pinout for internal registers is shown in Figure 1-1.

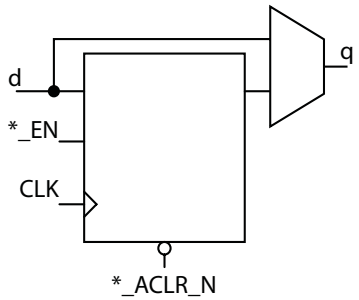

Figure 1-1 · Pinout of Internal Registers

When SgHardMultAcc is configured to use registers for any of the operands, the input and output ports shown in Table 1-3 appear in the generated macro.

Table 1-3 · SgHardMultAcc Register Ports

Register Port	Port Name		
	Rising-Edge Clock	Active-low Asynchronous Clear	Active-high Enable
A	CLK	A_ACLR_N	A_EN
B		B_ACLR_N	B_EN
SUB		SUB_ACLR_N	SUB_EN
SLOAD_N		SLOAD_ACLR_N	SLOAD_EN
ARSHFT17		ARSHFT17_ACLR_N	ARSHFT17_EN
P (along with CDOUT[40:0] and OVERFLOW)		P_ACLR_N	P_EN

SgHardMultAcc is always configured to use registers for output ports P[40:0] (along with CDOUT[40:0] and OVERFLOW). When SLOAD_N is asserted, these registers initialize their data from SLOAD_DATA on the next clock edge as long as data A or B is zero (by resetting their registers), as shown in the equation below.

$P_n[40:0] = SLOAD\_DATA + 0$

2 Interface Description

Ports

Figure 2-1 shows the SgHardMultAcc input and output ports. The ports shown are a superset of all possible ports. Only a subset of the ports are used in any given SgHardMultAcc configuration.

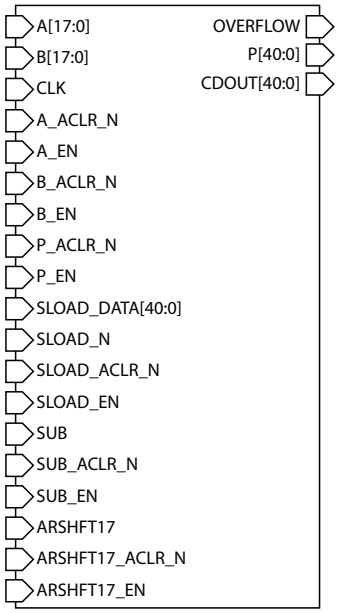

Figure 2-1 · SgHardMultAcc Pinout Diagram

The port signals for the SgHardMultAcc macro are defined in Table 2-1.

Table 2-1 · SgHardMultAcc Ports

Signal	Input/ Output	Polarity	Description
A	Input	High	Input data A
B	Input	High	Input data B
CLK	Input	Rising	Input clock for A, B, SLOAD_N, SUB, ARSHFT17, P[40:0] (along with CDOUT[40:0] and OVERFLOW) registers
A_ACLR_N	Input	Low	Asynchronous reset for data A registers
A_EN	Input	High	Enable for data A registers
B_ACLR_N	Input	Low	Asynchronous reset for data B registers
B_EN	Input	High	Enable for data B registers
P_ACLR_N	Input	Low	Asynchronous reset for result P[40:0] (along with CDOUT[40:0] and OVERFLOW) registers

Table 2-1 · SgHardMultAcc Ports

Signal	Input/ Output	Polarity	Description
P_EN	Input	High	Enable for result P_n[40:0] (along with CDOUT[40:0] and OVERFLOW) registers
SLOAD_DATA	Input	High	Synchronous load data into result P[40:0] (and CDOUT[40:0]) registers on the next clock edge as long as data A or B is zero P_n[40:0] = SLOAD_DATA + 0 See Table 1-2 on page 9 for information on how SLOAD_DATA is propagated to operand C
SUB	Input	High	Subtract operation P_n[40:0] = C + (A x B) when SUB = 0 P_n[40:0] = C - (A x B) when SUB = 1 Refer to Table 1-2 on page 9 to see how operand C is derived from P_{n-1}or SLOAD_DATA
SLOAD_N	Input	Low	When SLOAD_N = 0, load SLOAD_DATA into P[40:0] (and CDOUT[40:0]) registers on the next clock edge; ensure either A = 0 or B = 0 (by resetting their registers) P_n[40:0] = SLOAD_DATA + 0 When SLOAD_N = 1, propagate the previous value of result to P[40:0] (and CDOUT[40:0]) registers
ARSHFT17	Input	High	When asserted, a 17-bit arithmetic right-shift is performed on operand C going into the accumulator
SUB_ACLR_N	Input	Low	Asynchronous reset for SUB register
SUB_EN	Input	High	Enable for SUB register
SLOAD_ACLR_N	Input	Low	Asynchronous reset for SLOAD_N register
SLOAD_EN	Input	High	Enable for SLOAD_N register
ARSHFT17_ACLR_N	Input	Low	Asynchronous reset for ARSHFT17 register
ARSHFT17_EN	Input	High	Enable for ARSHFT17 register
P[40:0]	Output	High	Result data: P_n = C + (A x B) when SUB = 0 P_n = C - (A x B) when SUB = 1 Refer to Table 1-2 on page 9 to see how operand C is derived from P_{n-1} or SLOAD_DATA

Table 2-1 · SgHardMultAcc Ports

Signal	Input/ Output	Polarity	Description
CDOUT[40:0]	Output Cascade	High	Cascade output of result P[40:0]. CDOUT is a copy of P[40:0]; the entire bus must either be dangling or drive an entire CDIN[40:0] of another MATH block in cascaded mode.
OVERFLOW	Output	High	If C +/- (A x B) > 2^{40} -1 then OVERFLOW = 1 If C +/- (A x B) < -2^{40}, then OVERFLOW = 1 Otherwise, OVERFLOW = 0 Refer to Table 1-2 on page 9 to see how operand C is derived from P_{n-1} or SLOAD_DATA

Configuring the SgHardMultAcc Macro

SgHardMultAcc settings for configuring the macro are listed in Table 2-2. You can double-click the SgHardMultAcc macro in the Project Manager Catalog or open and configure the macro in SmartDesign (see "SmartDesign" on page 15).

Table 2-2 · SgHardMultAcc Configuration Descriptions

Name	Valid Range	Description
Function		Selects an Accumulator macro function: Multiplier with Adder; Multiplier with Subtractor; Multiplier with Adder/Subtractor; and Loadable variants of the same function: Loadable Multiplier with Adder, Loadable Multiplier with Subtractor, Loadable Multiplier with Adder/Subtractor
Input Port A		
Use Constant		Sets input port A to constant
Constant Value (Hex)	-2^{17} to (2^{17} - 1)	Two's complement value of A, if A is constant. Values shorter than 18 bits are padded with zeros. Negative values must be a full 18 bits wide.[1]
Width	2 to 18	Width of input port A (if A is not constant); if shorter than 18 bits it is sign-extended [2]
Register Port		Registers input port A (if A is not constant)
Input Port B		
Width	2 to 18	Width of input port B; if shorter than 18 bits it is sign-extended [2]
Register Port		Registers input port B
Input Ports SLOAD_DATA/SLOAD		
Use Constant		Sets input port SLOAD_DATA to constant

Table 2-2 · SgHardMultAcc Configuration Descriptions

Name	Valid Range	Description
Constant Value (Hex)	-2^{40} to (2^{40} - 1)	Two's complement value of SLOAD_DATA, if SLOAD_DATA is constant. Values shorter than 41 bits are padded with zeros. Negative values must be a full 41 bits wide.[3]
SLOAD_DATA Width	2 to 41	Width of input port SLOAD_DATA; if shorter than 41 bits it is sign-extended [2]
Register SLOAD Port		Registers input port SLOAD_N
Input Port ARSHFT17		
Arithmetic Right Shift of Cascaded Input		Selects Arithmetic right-shift of operand C. See Table 1-2 on page 9 for information on obtaining values for operand C.
Register Port		Registers input port ARSHFT17
Input Port SUB		
Register Port		Registers input port SUB
Target FPGA		
Die	RTAX2000D or RTAX4000D	Target device

1. *E.g. 0x1FFFF means +131071 (2^{17} - 1), while 0x3FFFF means -1*
2. *E.g. if the width is 8, a value of 0x7F means +127 and a value of 0xFF means -1*
3. *E.g. 0xFFFFFFFFFF means +(2^{40} - 1), while 0x1FFFFFFFFF means -1.*

3 Tool Flows

Licenses

SgHardMultAcc is included for free in the Libero® IDE Project Manager Catalog and does not require a separate license to instantiate and use in Actel devices. A complete structural netlist is provided for the macro.

SmartDesign

SgHardMultAcc is available for download from the Libero® Integrated Design Environment (IDE) IP Catalog via the web repository. Once it is listed on the Catalog, the macro can be instantiated using SmartDesign. To use it, double-click or drag it from the Arithmetic section of the Catalog onto the Canvas. For information on using SmartDesign to configure, connect, and generate cores, see the Libero IDE online help.

Figure 3-1 shows the SgHardMultAcc configuration window. The configuration window displays the configuration options for each input port and output port. After configuring and generating the macro instance, you can simulate basic functionality. The macro can then be instantiated as a component of a larger design.

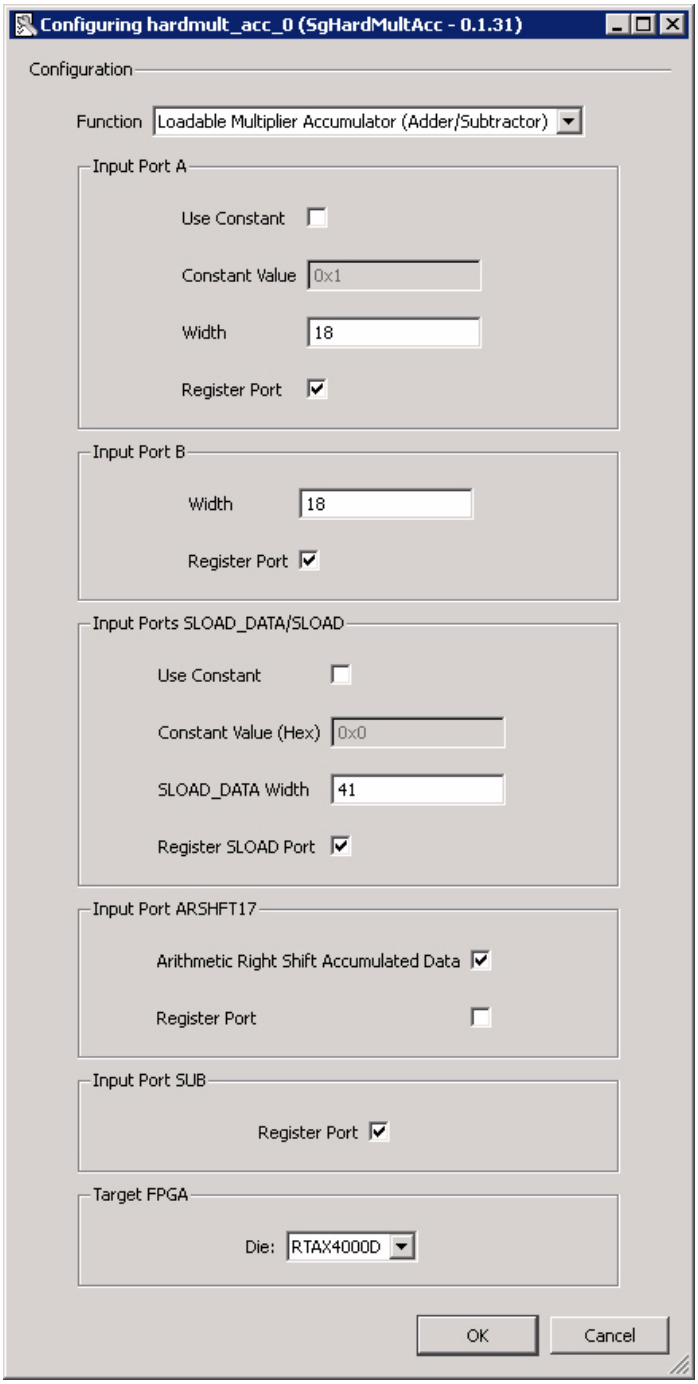

Figure 3-1 · SgHardMultAcc Configuration Window

Place-and-Route in the Libero IDE

After running synthesis on the instantiated design, click the Place&Route button in the Project Manager to open Designer. SgHardMultAcc requires no special place-and-route settings.

A

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The technical support email address is tech@actel.com.

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