SmartDesign v8.4 User's Guide

Actel®
POWER MATTERS

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Trademarks

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SmartDesign

SmartDesign has been re-designed to enable faster creation of simple to complex System on Chip (SoC) designs including processor/bus based and Fusion mixed signal designs. Complete FPGA systems and subsystems can be designed in minutes by selecting from Actel's core libraries, making quick and error-free connections, and automatically creating a synthesis ready HDL file.

Key Features

- Visual block-based design creation tool
- Replaces CoreConsole for processor, bus-based, and DirectCore subsystem creation
- Quickly select, configure, and connect proven functional blocks from Libero IDE Project Manager Catalog: DirectCores, Smartgen Cores, and Actel cells
- Import and connect user generated IP, Designer Blocks, and custom/glue-logic HDL modules including ViewDraw schematics
- SmartGuide guidance suggests compatible interfaces and notes required peripherals
- All construction is performed on a single Canvas
- All pins/ports are exposed and ready for connection on the Canvas
- Automatic or simple point-and-click manual connections
- Design-rule check disallows improper connections or unconnected ports
- Dynamic audit system informs of out-of-date configurations
- Automatic abstraction to synthesis-ready HDL: Verilog or VHDL
- Efficient construction of complex processor, bus based, Fusion mixed signal, and simple designs
- Complete FPGA SoC, FPGA subsystem, or embedded SmartDesign-in-SmartDesign

SmartDesign supports all Actel product families.

SmartDesign Design Flow

SmartDesign enables you to stitch together design blocks of different types (HDL, IP, etc) and generate a top-level design. The Files tab lists your SmartDesign files in alphabetical order.

You can build your design using SmartDesign with the following steps:

Step One – Instantiating components: In this step you will add one or more building blocks, HDL modules, components, and schematic modules from the project manager to your design. The components can be Designer blocks, SmartGen cores (cores generated from the core catalog), and IP cores.

Step Two – Connecting bus interfaces: In this step, you can add connectivity via standard bus interfaces to your design. This step is optional and can be skipped if you prefer manual connections. Components generated from the Catalog in Project Manager may include pre-defined interfaces that allow for automatic connectivity and design rule checking when used in a design.

Step Three – Connecting instances: The Canvas allows you to create manual connections between ports of the instances in your design. Unused ports can be tied off to GND or VCC (disabled); input buses can be tied to a constant, and you can leave an output open by marking it as unused.

Step Four – Validating the SmartDesign component: Verify the connectivity of your design using the Connectivity Check feature. This feature opens a special grid where design errors and warnings are organized by type and message. You can fix the errors and warnings directly in the grid. You must run the Connectivity Check again after you make your connections to check for new errors and warnings.

Step Five – Generating the SmartDesign component: In this step, you generate a top-level (Top) component and its corresponding HDL file. This component can be used by downstream processes, such as synthesis and simulation, or you can add your SmartDesign HDL into another SmartDesign.

You can save your SmartDesign at any time.

Using Existing Projects with SmartDesign

You can use existing Libero® Integrated Design Environment (IDE) projects with available building blocks in the project to assemble a new SmartDesign design component. You do not have to migrate existing top-level designs to SmartDesign and there is no automatic conversion of the existing design blocks to the SmartDesign format.

Note: SmartGen cores used in previous versions of software will work in SmartDesign, but they will NOT include standard bus interfaces if they are available. Bus interfaces (BIFs) can be recovered by regenerating the core in the latest software.

Examples of cores with standard BIFs: ASB, Flash Memory System Builder, VRPSM, AMBA DirectCore(s), and similar.

SmartDesign Frequently Asked Questions

The collection of SmartDesign Frequently Asked Questions are useful for anyone that is new to SmartDesign. All the information listed below is explained in detail in other sections of the help, but the information is summarized here for easy reference. Click any question to go to the corresponding explanation.

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2. I get a message saying it's unable to generate my SmartDesign due to errors, what do I do? What's the Connectivity Checker?
3. Is there an easy way for me to tie off multiple pins at once?

General Questions

What is SmartDesign?

SmartDesign is a design entry tool. It's the first tool in the industry that can be used for designing System on a Chip designs, custom FPGA designs or a mixture of both types in the same design. A SmartDesign can be the entire FPGA design, part of a larger SmartDesign, or a user created IP that can be stored and reused multiple times. It's a simple, intuitive tool with powerful features that enables you to work at the abstraction level at which you are most comfortable.

It can connect blocks together from a variety of sources, verify your design for errors, manage your memory map, and generate all the necessary files to allow you to simulate, synthesize, and compile your design.

How do I create my first SmartDesign?

From the Project Manager Project Flow window, in the Design Entry Tools section, click the SmartDesign icon:

Instantiating Your SmartDesign

Where is the list of Cores that I can instantiate into my SmartDesign?

The list of available cores is displayed in the Project Manager Catalog. This catalog contains all DirectCore IP, SmartGen cores, and Actel macros (cells).

How do I instantiate cores into my SmartDesign?

Drag and drop the core from the Catalog onto your SmartDesign Canvas. The configurator for that core opens automatically. Choose your configurations, click OK, and an instance of your core appears on the SmartDesign Canvas.

I have a block that I wrote in VHDL (or Verilog); can I use that in my SmartDesign?

Yes! Import your HDL file into the Project Manager (File > Import Files). After you do this, your HDL module will appear in the Project Manager Hierarchy. Then, drag-and-drop it from the Hierarchy onto your SmartDesign Canvas.

Working in SmartDesign

How do I make connections?

Let SmartDesign do it for you. Right-click the Canvas and choose **Auto Connect**.

Auto Connect didn't connect everything for me, how do I make manual connections?

1. Select the pins you want connected by using the mouse and the CTRL key.
2. Right-click one of the selected pins and choose **Connect**.
3. For bus interface pins you can do the same thing, OR: Right click a bus interface pin, choose **Find Compatible Bus Interfaces**. A dialog box will display a list of the compatible bus interfaces in the design that you can connect to. Choose the bus interface you want to connect to from the list and click OK.

How do I connect a pin to the top level?

Right-click the pin and choose **Promote to Top Level**. You can even do this for multiple pins at a time, just select all the pins you want to promote, right-click one of the pins and choose **Promote to Top Level**. All your selected pins will be promoted to the top level.

Oops, I just made a connection mistake. How do I disconnect two pins?

Use CTRL+Z to undo your last action. If you want to undo your 'undo', hit redo (CTRL+Y).

To disconnect pins you can:

- Right-click the pin you want to disconnect and choose **Disconnect**
- Select the net and hit the delete key

I need to apply some simple 'glue' logic between my cores. How do I do that?

For basic inversion of pins, you can right-click a pin and choose **Invert**. An inverter will be placed at this pin when the design is generated. You can also right-click a pin and choose Tie Low or Tie High if you want to connect the pin to either GND or VCC.

To tie an input bus to a constant, right-click the bus and choose **Tie to Constant**. To mark an output pin as unused, right-click the pin and choose **Mark as Unused**.

To clear these, just right-click on the pin again and choose **Clear Attribute**.

My logic is a bit more complex than inversion and tie offs - what else can I do?

You have full access to the Actel library cells, including AND, OR, and XOR logic functions. These are located in the Project Manager Catalog, listed under Actel Cells. Drag the logic function you want onto your SmartDesign Canvas.

How do I create a new top level port for my design?

Scroll your design all the way to the left. Right-click the block on the far left of your Canvas (this represents the top level of your design) and choose **Add Port**.

How do I rename one of my instances?

Double-click the instance name on the Canvas and it will become editable. The instance name is located directly above the instance on the Canvas.

How do I rename my top level port?

Right-click the port you want to rename and choose **Modify Port**.

How do I rename my group pins?

Double-click the group pin name in the instance and it will become editable.

I need to reconfigure one of my Cores, can I just double click the instance?

Yes.

I want more Canvas space to work with!

Maximize your workspace (CTRL-W), and your Canvas will maximize within the Project Manager. Hit CTRL-W again if you need to see your Hierarchy or Catalog.

Working with Processor-Based Designs in SmartDesign

How do I connect my peripherals to the bus?

Make sure you have the proper bus core that is compatible with your peripheral instantiated in the design. Click **Auto Connect** and SmartDesign will automatically form the connections.

But I need my peripheral at a specific address or slot.

Right-click the Canvas and choose **Modify Memory Map** to invoke the Modify Memory Map dialog that enables you to set a peripheral to a specific address on the bus.

The bus core will show the slot numbers on the bus interface pins. These slot numbers correspond to a memory address on the bus.

Verify that your peripheral is mapped to the right bus address by viewing your design's Memory Map.

How do I view the Memory Map of my design?

In the Project Manager menu bar, choose **SmartDesign > Show Memory Map/Data Sheet**. This creates a datasheet of your design, including the pin out, cores used, and memory map.

The memory map section will also show the memory details of each peripheral, including any memory mapped registers.

How do I simulate my processor design?

SmartDesign automatically generates the necessary Bus Functional Model (BFM) scripts required to simulate your processor based design. A top level testbench for your SmartDesign is generated automatically as well.

Create your processor design, generate it, and you will be able to simulate it in Model*Sim*.

I have my own HDL block that I want to connect as a peripheral on the AMBA bus. How can I do that?

If your block has all the necessary signals to interface with the AMBA bus protocol (ex: address, data, control signals) then:

1. In the Project Manager Catalog (inside the Bus Definitions tab), find the AHB or APB slave interface.
2. Drag this bus definition onto your instance on the Canvas. A dialog box opens, asking you to map the signals on your instance to the required bus definition signals. Complete this mapping and click OK.

Now your instance has a proper AMBA bus interface on it. You can manually connect it to the bus or let Auto Connect find a compatible connection.

Making Your Design Look Nice

Can the tool automatically place my instances on the Canvas to make it look nice?

Yes. Right-click the Canvas white space and choose **Auto Arrange Instances**.

My design has a lot of connections, and the nets are making my design hard to read. What do I do?

You can disable the display of the nets in the menu bar (Canvas > Nets). This automatically hides all the nets in your design.

You can still see how pins are connected by selecting a connected pin, the net will automatically be visible again.

You can also selectively show certain nets, so that they are always displayed, just right click on a connected pin and choose **Show Net**.

My instance has too many pins on it; how can I minimize that?

Try grouping functional or unused pins together. For example, on the CoreInterrupt there are 8 FIQSource* and 32 IRQSource* pins, group these together since they are similar in functionality.

To group pins: Select all the pins you want to group, then right-click one of the pins and choose **Add pins to group**.

If a pin is in a group, you are still able to use it and form connections with it. Expand the group to gain access to the pin.

Oops, I missed one pin that needs to be part of that group? How do I add a pin after I already have the group?

Select the pin you want to add and the group pin, right-click and choose **Add pins to <name> group**.

I have a pin that I don't want inside the group, how do I remove it?

Right-click the pin and choose **Ungroup selected pins**.

How can I better see my design on the Canvas?

There are zoom icons in the toolbar: 

From left to right, they are: Zoom in, Zoom out, Zoom to fit, and Zoom range. You can also maximize your workspace with CTRL-W.

Generating Your Design

Ok, I'm done connecting my design, how do I 'finish' it so that I can proceed to synthesis?

In the Project Manager toolbar, click the Generate Design icon  or right-click the Canvas and choose **Generate Design**.

I get a message saying it's unable to generate my SmartDesign due to errors, what do I do? What's the Connectivity Checker?

In the Project Manager toolbar, click the Connectivity Checker icon: 

The connectivity checker will give you a list of all the errors and warnings in your design, including unconnected input pins, required pin connections, configuration incompatibilities between cores, etc.

Errors are shown with a small red octagon and must be corrected before you can generate, warnings may be ignored.

What does this error mean? How do I fix it?

Review the Connectivity Checker topic for an explanation of errors in the Connectivity Checker and steps to resolve them.

Is there an easy way for me to tie off multiple pins at once?

Yes, if you are in the Connectivity Checker grid, you can select multiple pins by highlighting the rows that they are in. Multi-selecting works just like your typical spreadsheet editor.

Once all the pins have been selected, right-click one of the pin names and choose **Tie Low** or **Tie High**. Make sure you only have input pins selected otherwise the menu item won't be enabled.

Getting Started with SmartDesign

Creating a New SmartDesign Component

1. From the **File** menu, choose **New** or press the **SmartDesign** button in the Project Manager Project Flow window. The **New** dialog box opens (see figure below - file types vary depending on your project settings).

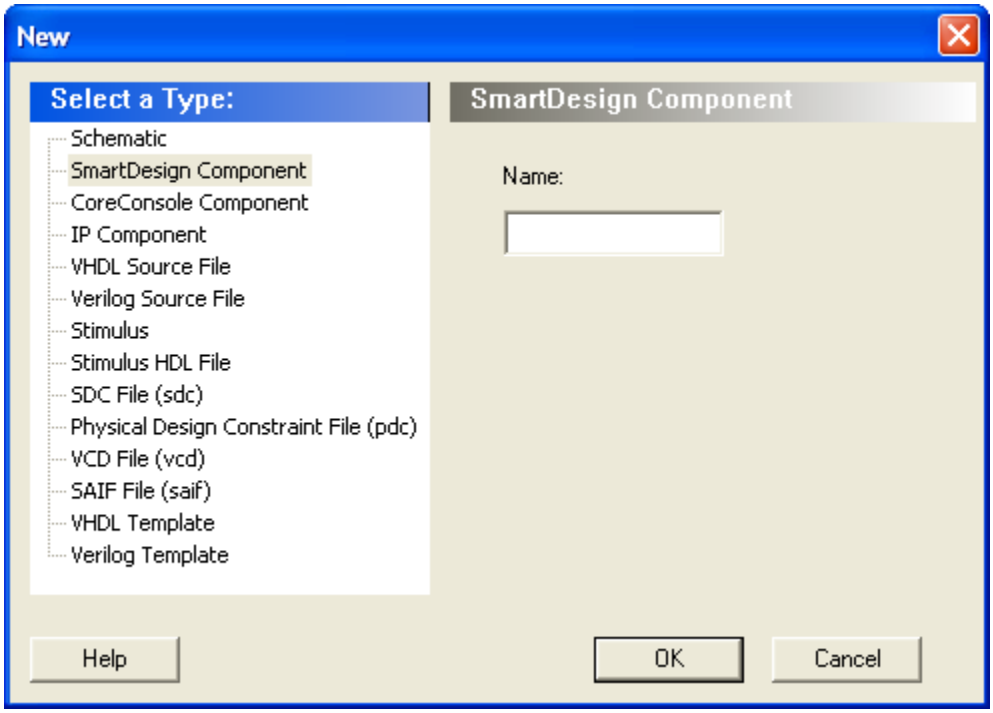


Figure 1 · New Dialog Box

2. Select **SmartDesign Component**, enter a component name and click **OK**. The component appears in the Hierarchy tab of the Design Explorer. Also, the main window displays the design Canvas.

Note: The component name must be unique in your project.

Opening an Existing SmartDesign Component

To open an existing component do one of the following:

- In the Design Explorer, click the **Hierarchy** tab and double-click the component you want to open.
- In the Design Explorer, from the Files tab, expand the Components list and double-click the component you want to open.

The main window displays the SmartDesign Canvas for the SmartDesign component.

Saving/Closing a SmartDesign Component

To save the current SmartDesign design component, from the File menu, choose **Save** <component_name>. Saving a SmartDesign component only saves the current state of the design; to generate the HDL for the design refer to Generating a SmartDesign component.

To close the current SmartDesign component without saving, from the **File** menu, choose **Close**. Select **NO** when prompted to save.

You can also close a SmartDesign component by right-clicking the name of the SmartDesign tab in the work area window and choosing **Close**, as in the figure below.

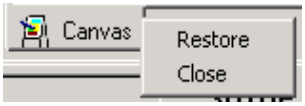


Figure 2 · Close a SmartDesign

Importing a SmartDesign Component

Importing an existing SmartDesign component into a SmartDesign project will not automatically import the sub-components of that imported SmartDesign component.

You must import each sub-component separately.

After importing the sub-components, you must open the SmartDesign component and replace each sub-component so that it references the correct component in your project. .

Deleting a SmartDesign Component from the Libero IDE Project

To delete a SmartDesign component from the project:

1. In the **Design Explorer**, click the **Hierarchy** tab.
2. Select the SmartDesign component that you want to delete. Right-click the component name and select **Delete from Project** or **Delete from Disk and Project**, or click the **Delete** key to delete from project.

Memory Maps / Data Sheet

If your design contains standard Bus Instances such as the DirectCore AMBA bus cores, CoreAPB or CoreAHB, then you can view the Memory Map Configuration of your design. To do so, from the SmartDesign menu, choose **Show Memory Map / Data Sheet**.

The design's memory map is determined by the connections made to the bus component. A bus component is divided into multiple slots for slave peripherals or instances to plug into. Each slot represents a different address location and range to the Master of the bus component.

The datasheet reports the memory map of the different subsystems of your design, where a subsystem is any independent bus structure with a Master and Slave peripheral attached.

Connecting peripherals to busses can be accomplished using the normal SmartDesign connectivity options:

- **Auto-Connect** - the system finds compatible bus interfaces and connects them together
- The Modify Memory Map dialog box
- Canvas - Make connections between your blocks.
- Finding compatible bus interfaces

Your application and design requirements dictate which address location (or slots) is most suitable for your bus peripherals. For example, the memory controller should be connected to Slot0 of the CoreAHB bus because on Reset, the processor will begin code execution from the bottom of the memory map.

The Memory Map View opens your default web browser to display the memory map information. An example is shown in the figure below.

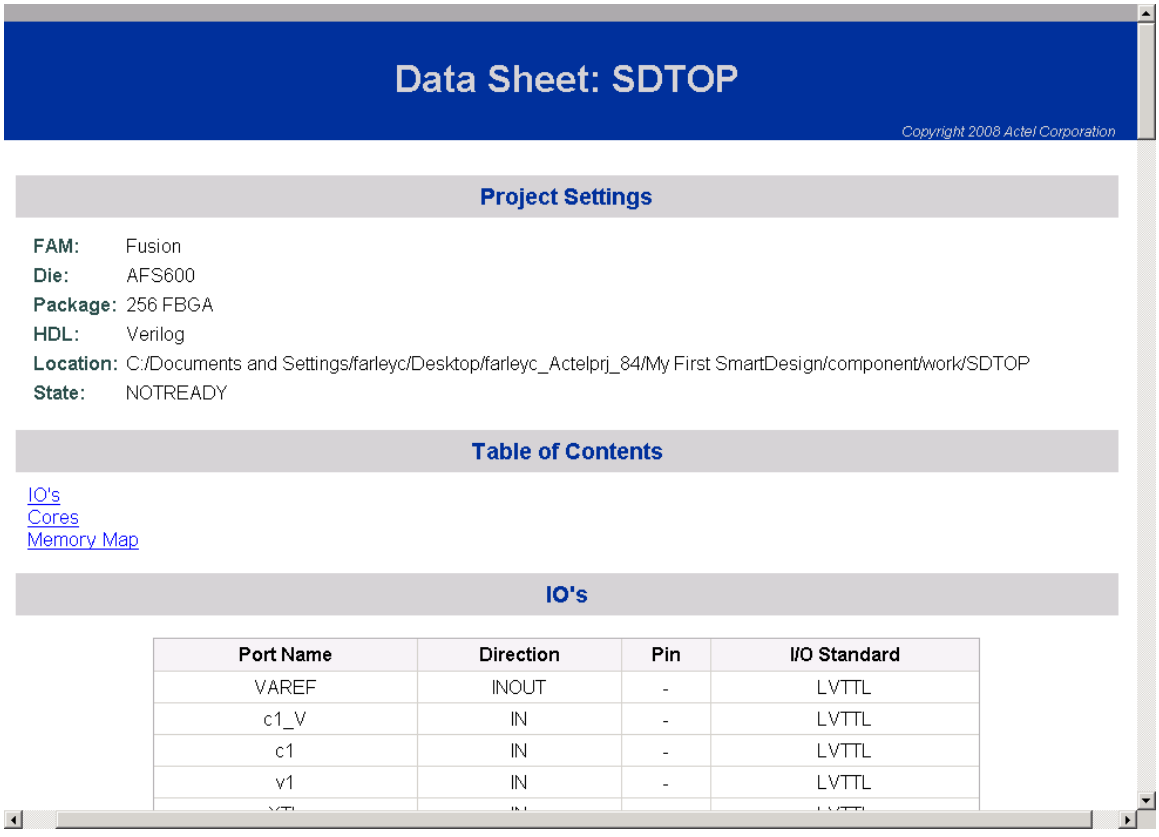


Figure 3 · Example Memory Map

Modify Memory Map Dialog Box

The Modify Memory Map dialog box (shown in the figure below) enables you to connect peripherals to buses via a drop-down menu. To open the dialog box, right-click on the Canvas or specific bus instance and choose **Modify Memory Map**.

This dialog simplifies connecting peripherals to specific base addresses on the bus. The dialog shows all the busses in the design; select a bus in the left pane to assign or view the peripherals on a bus. Busses that are bridged to other busses are shown beneath the bus in the hierarchy.

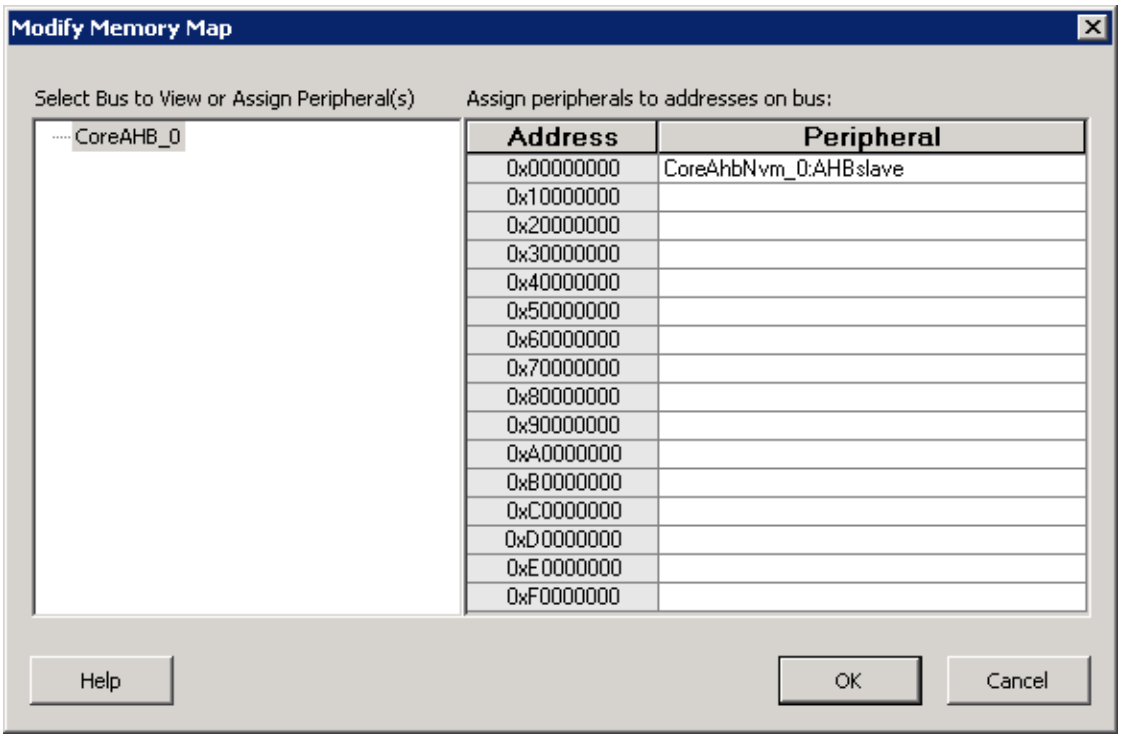


Figure 4 · Modify Memory Map Dialog Box

Click the Peripheral drop-down menu to select the peripheral you wish to assign to each address. To remove (unassign) a peripheral from an address, click the drop-down and select the empty element.

Click OK to create the connections between the busses and peripherals in the design.

Finding Files in SmartDesign

Use the Find Window to search for ports, nets, or instances in SmartDesign.

Searching for ports / nets / instances in SmartDesign highlights the objects on the Canvas.

SmartDesign User Interface

SmartDesign User Interface Overview

The SmartDesign tool is integrated into the Libero IDE Project Manager.

The Canvas is the main work area for SmartDesign. The Canvas view displays a high-level block diagram of your design.

The Grid and Schematic views are available from the SmartDesign menu in the Project Manager. These views are not required to complete your design.

The Grid displays your design in a configurable spreadsheet, enabling you to specify detailed connections for each instance in your SmartDesign.

The Schematic View displays your design elements with port names, busses, and nets.

Changes made in one view will immediately be reflected in all other views, enabling you to quickly make and see changes to your design.

You can close each view by right-clicking the name of the view inside the SmartDesign tab and choosing **Close**.

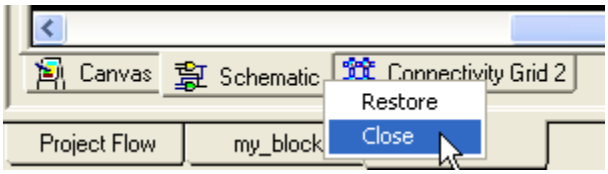


Figure 5 · Close the Active View

To re-open any view, from SmartDesign menu choose **Show Canvas View**, **Show Grid View**, or **Show Schematic View**.

Canvas View

Canvas Overview

The SmartDesign Canvas is like a whiteboard where functional blocks from various sources can be assembled and connected; interconnections between the blocks represent nets and busses in your design.

You can use the Canvas to manage connections, set attributes, add or remove components, etc. The Canvas displays all the pins for each instance (as shown in the figure below).

The Canvas enables you to drag a component from the Hierarchy, Files list, or a core from the Catalog and add an instance of that component or core in the design. Some blocks (such as Basic Blocks) must be configured and generated before they are added to your Canvas. When you add/generate a new component it is automatically added to your Hierarchy.

To connect two pins on the Canvas, select any two pins on the Canvas (Ctrl + click to select a pin), right-click one of the pins you selected and choose Connect. The Connect is disabled if you attempt to illegally connect two pins.

Click the Maximize Work Area button  to hide the other windows and show more of the Canvas. Click the button again to return the work area to the original size.

The Canvas displays bus pins with a + sign (click to expand the list) or - (click to hide list). If you add a slice on a bus the Canvas adds a + to the bus pin.

Components can be reconfigured any time by double-clicking the instance on the Canvas. You can also add bus interfaces to instances using this view. In the Canvas view, you can add graphic objects and text to your design.

Inputs and bi-directional pins are shown on the left of components, and output pins are shown on the right.

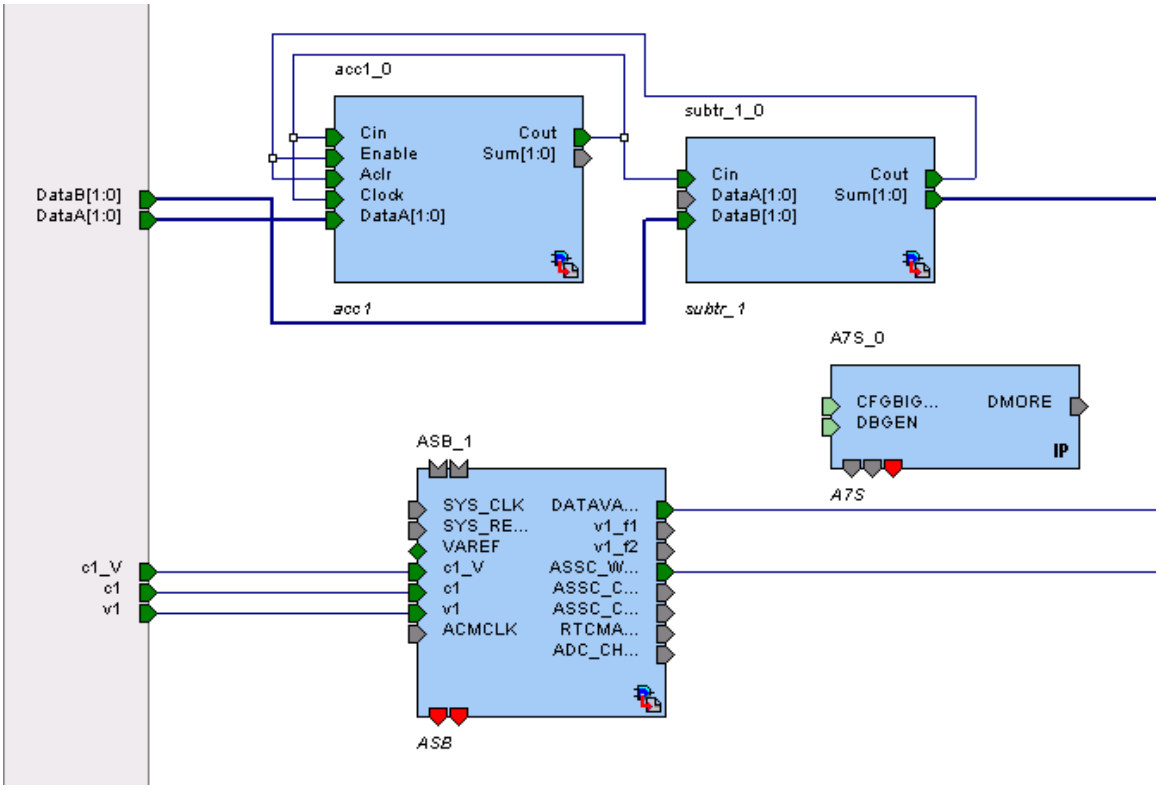


Figure 6 · SmartDesign Canvas

See Also

Canvas icons

Displaying Connections on the Canvas

The Canvas shows the instances, pins, and nets in your design (as shown in the figure below).

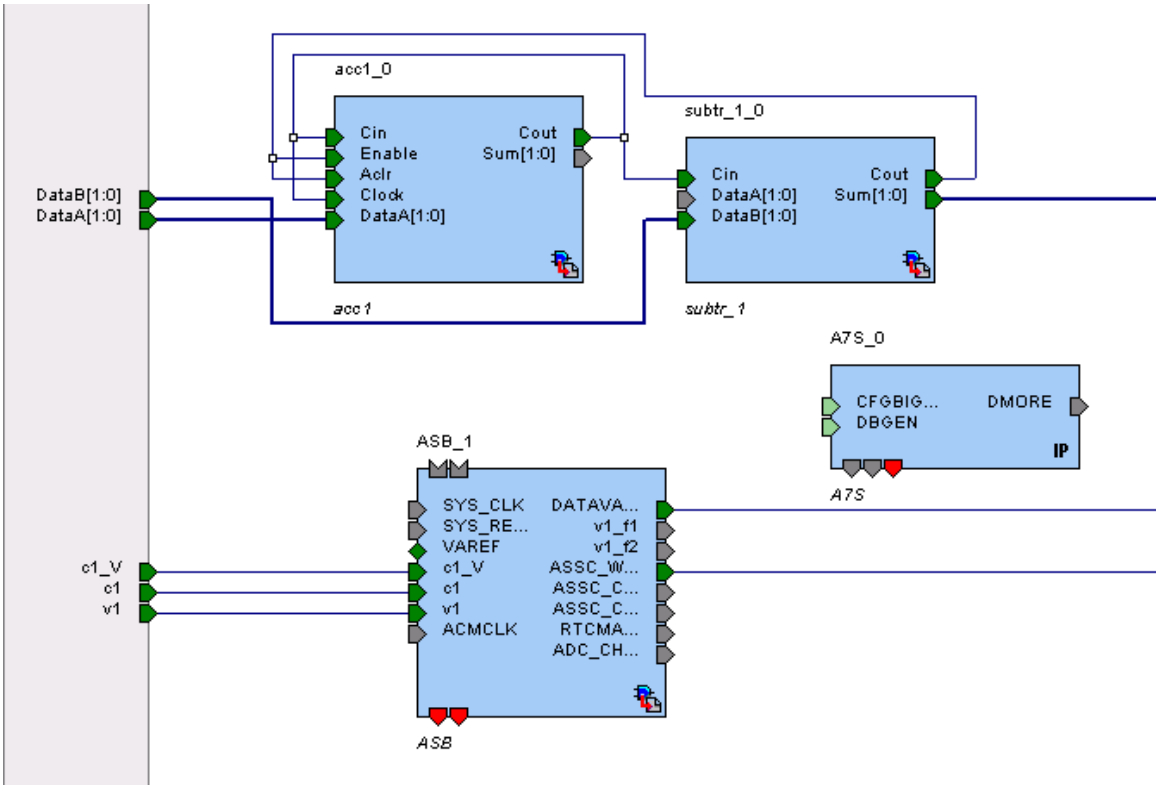


Figure 7 · Components in SmartDesign

Scalar net connections are shown in blue; bus net connections are dark blue.

Pin and Attribute Icons

Unconnected pins that do not require a connection are gray.

Unconnected pins that require a connection are red.

Unconnected pins that have a default tie-off are pale green.

Connected pins are green.

Right-click a pin to assign an attribute.

Pins assigned attributes are shown with an icon, as shown in the table below.

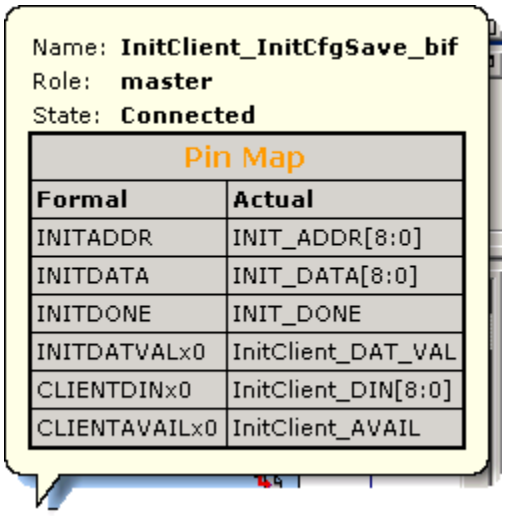
Table 1 · Pin Attribute Icons

Attribute	Icon
Tie Low	
Tie High	
Invert	
Mark as Unused	

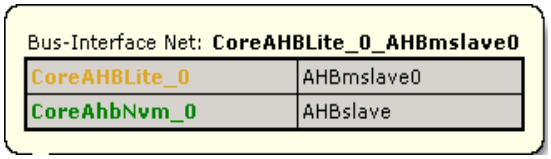
See the Canvas Icons reference page for definitions for each element on the Canvas.

Each connection made using a bus interface is shown in a separate connection known as a 'bus-interface net' (shown in brown lines).

Move the mouse over a bus interface to display its details (as shown below).



Hover over a bus interface net to see details (as shown below).



Making Connections Using the Canvas

Use the Canvas to make connections between instances.

To connect two pins on the Canvas, select any two (Ctrl + click to select a pin), right-click one of the pins you selected and choose Connect. Illegal connections are disabled; the Connect menu option is unavailable.

Promoting Ports to Top Level

To automatically promote a port to top level, select the port, right-click, and choose **Promote To Top Level**. This automatically creates top-level ports of that name and connects the selected ports to them. If a port name already exists, a choice is given to either connect to the existing ports or to create a new port with a name <port name>_<i> where i = 1…n.

Double-click a top-level port to rename it.

Bus slices cannot be automatically promoted to top level. You must create a top level port of the bus slice width and then manually connect the bus slice to the newly created top level port.

Tying Off Input Pins

To tie off ports, select the port, right-click and choose **Tie High** or **Tie Low**.

Tying to Constant

To tie off bus ports to a constant value, select the port, right-click and choose **Tie to a Constant**. A dialog appears (as shown in the figure below) and enables you to specify a hex value for the bus.

To remove the constant, right-click the pin and choose **Clear Attribute** or **Disconnect**.

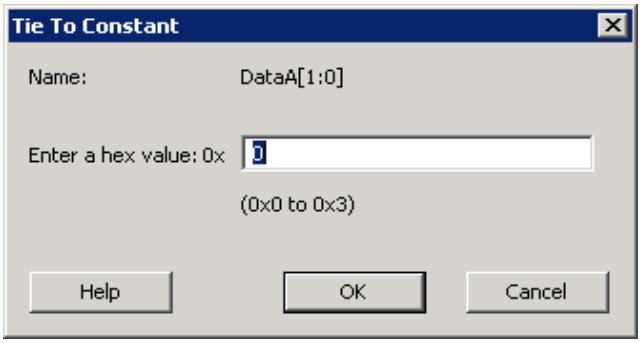


Figure 8 · Tie to Constant Dialog Box

Making Driver and Bus Interface Pins Unused

Driver or bus interface pins can be marked unused (floating/dangling) if you do not intend to use them as a driver in the design. If you mark a pin as unused the Connectivity Checker does not return Floating Driver or Unconnected Bus Interface messages on the pin.

Once a pin is explicitly marked as unused it cannot be used to drive any inputs. The unused attribute must be explicitly removed from the pin in order to connect it later. To mark a driver or bus interface pin as unused, right-click the driver or bus interface pin and choose Mark as Unused.

Simplifying the Display of Pins on an Instance using Pin Groups

The Canvas enables you to group and ungroup pins on a single instance to simplify the display. This feature is useful when you have many pins in an instance, or if you want to group pins at the top level. Pin groups are cosmetic and affect only the Canvas view; other SmartDesign views and the underlying design are not affected by the pin groups.

Grouping pins enables you to:

- Hide pins that you have already connected
- Hide pins that you intend to work on later
- Group pins with similar functionality
- Group unused pins
- Promote several pins to Top Level at once

To group pins:

1. Ctrl + click to select the pins you wish to group. If you try to click-and-drag inside the instance you will move the instance on the canvas instead of selecting pins.
2. Right-click and choose **Add pins to group** to create a group. Click + to expand a group. The icon associated with the group indicates if the pins are connected, partially connected, or unconnected (as shown in the figure below).

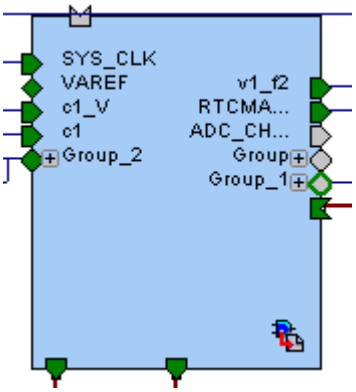


Figure 9 · Groups in an Instance on the Canvas

To add a pin to a group, Ctrl + click to select both the pin and the group, right-click and choose **Add pin to group**.

To ungroup pins:

1. Click + to expand the group.
2. Right-click the pin you wish to remove from the group and choose **Ungroup selected pins**. Ctrl + click to select and remove more than one pin in a group.

A group remains in your instance after you remove all the pins. It has no effect on the instance; you can leave it if you wish to add pins to the group later, or you can right-click the group and choose **Delete** to remove it from your instance.

If you delete a group from your instance any pins still in the group are unaffected.

To promote a group to Top level:

1. Create a group of pins.
2. Right-click the group and choose Promote to Top level.

Bus Instances

Bus Components in the Actel Core Catalog, such as CoreAHB or CoreAPB, implement an on-chip bus fabric. When these components are instantiated into your canvas they are displayed as horizontal or vertical lines. Double-click the bus interfaces of your component to edit the connections.

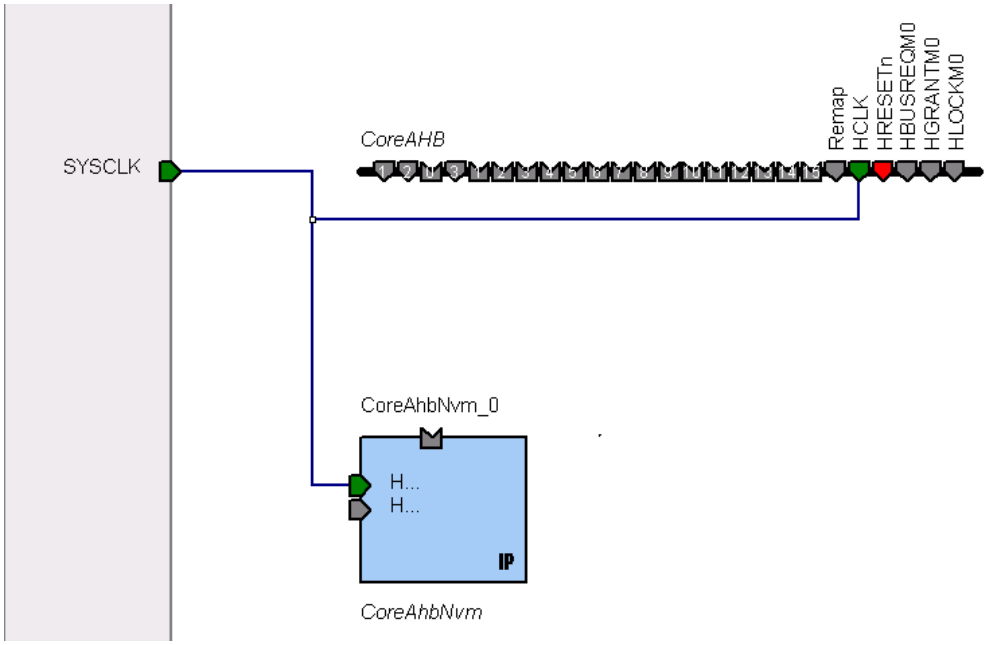


Figure 10 · Bus Instance in SmartDesign

Positioning Busses on the Canvas

You may want to adjust the positioning and orientation of a bus on your canvas in order to organize the display of your design.

Rotating Busses

Bus instances can be rotated ninety degrees (they must be horizontal or vertical). To rotate a bus instance ninety degrees left or right, right-click the black bar and choose **Shape > Rotate Left** (or Rotate Right).

Flipping Busses

You can flip a bus along the horizontal or vertical axis. To flip a bus, right-click the black bar and choose **Shape > Flip Horizontal** (or Flip Vertical). Flipping a bus instance along an axis flips ALL the instances directly connected to the bus instance, except those that are connected to another bus instance.

Adding Graphic Objects

You can document your design by adding comments and notations directly on the Canvas.

The Canvas toolbar (see figure below) enables you to add and modify decorative graphic objects, such as shapes, labels, lines, and arrows on the Canvas.

Figure 11 · Canvas Toolbar

Adding and Deleting Lines and Shapes

To add a line or a shape:

1. Select the line or shape button.
2. Click, drag and release on the Canvas. The table below provides a description of each button.

Button	Description
	Line
	Arrow
	Rectangle
	Ellipse

Note: Hold the Shift key to constrain line and arrow to 45 degree increments or constrain the proportions of the rectangle (square) or ellipse (circle).

To change the line and fill properties:

1. Select the element(s), right-click it, and choose **Properties**.

- Select **Line** to modify the color, style and width of the line.
- Select **Fill** to modify the crosshatch and the foreground and background colors.

2. Click **OK**.

To delete a line or shape, select the object and press Delete.

Adding Text

To add text, select the text tool  and click the Canvas to create a text box. To modify the text, double-click the text box and then type.

To modify the text box properties:

1. Select the text box, right-click it, and choose **Properties**.

- Select **Text** to modify the text alignment.
- Select **Line** to modify the color, style and width of the line.
- Select **Fill** to modify the crosshatch and the foreground and background colors.
- Select **Font** to modify the font properties.

2. Click **OK**.

Adding Images

To add an image to the canvas:

1. Select the image button  . The **Open** dialog box opens.
2. Select the image you want to add and click **OK**.
3. Select the image and place it in the desired location.

Rotating Elements

Select the element(s) you want to rotate and click the appropriate rotate button. See the table below for a description of each button.

Button	Description
	Free rotate
	Rotate to the left
	Rotate to the right

Flipping Elements

Select the element(s) you want to flip and click the appropriate flip button. See the table below for a description of each button.

Button	Description
	Flip vertically
	Flip horizontally

Aligning Elements

Select two or more elements on the Canvas and click the appropriate align button. See the table below for a description of each button.

Button	Description
	Align top
	Align middle
	Align bottom
	Align left
	Align center
	Align right

Grouping Graphic Objects

Objects on the Canvas can be grouped and ungrouped.

To group two or more elements, select the elements, right-click, and choose **Grouping** > **Group**.

To ungroup two or more elements, select the elements, right-click, and choose **Grouping** > **Ungroup**.

Ordering Elements (Z-order)

Elements on the Canvas can be positioned in front or in back of each other.

To change the order of the element(s), select the element and from the right-click menu, choose **Order** and select one of the available options: **Bring to Front**, **Send to Back**, **Bring Forward**, or **Send Backward**.

Auto-Arranging Instances

The Auto Arrange Instances button  arranges the instances on the Canvas. You can also right-click the Canvas and choose **Auto Arrange Instances** from the right-click menu.

Locking Instance Position

You can lock the placement of any instance on the Canvas. Right-click an instance and choose Lock Location to lock the placement. When you lock placement, the Auto Arrange Instances option has no effect on the instance.

To unlock an instance, right-click the instance and choose Unlock Location.

See Also

Bus instances

Auto-routing connections

Auto-Arrange Connections

The Auto Arrange Connections button  arranges the connections between instances. The way connections are drawn is highly dependent on the placement of the instances on the Canvas. The top-level connections are shown connected to the Top Level instance (green boxes).

Auto-arranging connections does not move instances; it places the nets between instances.

To auto-arrange your connections, right-click the canvas and choose **Auto arrange connections**.

Note: Select a placement for your instances that is reasonable with respect to connections before using Auto Route.

Replace Version for Instance

You can use the Replace Version for Instance dialog box (shown in the figure below) to restore or update version instances on your canvas without creating a new instance and losing your connections.

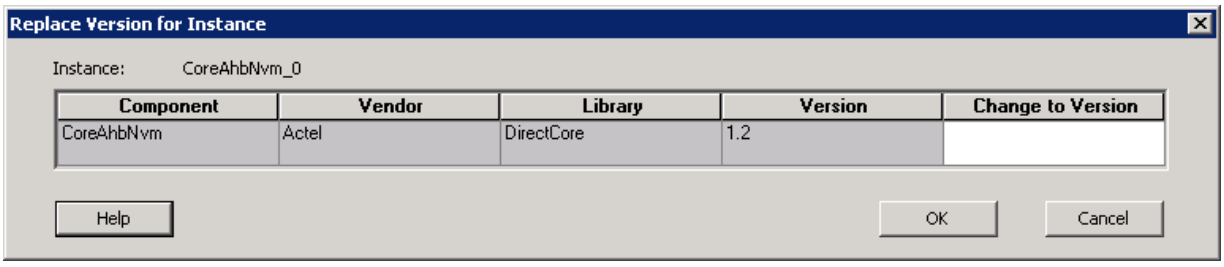


Figure 12 · Replace Version for Instance Dialog Box

To change the version of an instance:

1. From the right-click menu choose Replace Component for this Instance. The Replace Version for Instance dialog box appears.

2. Choose a new version from the Change to Version drop-down menu. Click OK.

Slicing

Bus ports can be sliced or split using Slicing. Then the sliced ports can be connected as regular ports.

To create a slice:

1. Select a bus port, right-click, and choose **Add Slice.** This brings up the **Add Slice** dialog box (see figure below).

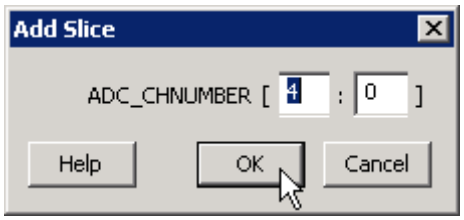


Figure 13 · Add Slice Dialog Box

2. Enter the parameters for the slice and click **OK**.

Note: Once a slice is created, other bus ports or slices of compatible size can be connected to it. Overlapping slices cannot be created for IN and INOUT ports on instances or top-level OUT ports.

To remove a slice, select the slice, right-click, and choose **Delete Slice.**

Exposing Driver Pins

Pins that are contained as part of a bus interface will automatically be filtered out of the display. These ports are considered to be connected and used as part of a bus interface.

However, there are situations where you may wish to use the ports that are part of the bus interface as an individual port, in this situation you can choose to expose the pin from the bus interface.

The only ports that are allowed to be exposed are Driver Pins. Driver pins are outputs on instances or inputs on the top-level. See Top-level connections for more information.

To expose a driver pin:

1. Select a bus interface port, right-click, and choose **Expose Driver Pin**. The Expose Driver Pin dialog box appears (as shown below).

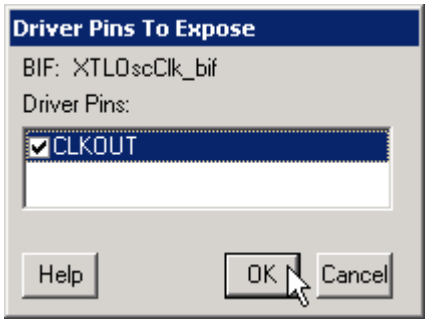


Figure 14 · Expose Driver Pin Dialog Box

2. Click the checkbox associated with the driver pin you want to expose. Once the port is exposed it appears in the Grid and is available for individual connection.

To un-expose a driver pin, right-click the exposed port and choose **Hide BIF Driver Pin**.

Instance Properties

Right-click a component instance and choose **Properties** to view the Name, Instance Name, and port information - name/direction-.

This dialog box is useful if you want to view the list of Port Names available in the instance from the Canvas view instead of the Grid.

See Also

Grid overview

Display panel

Connection panel

Rename Net

To rename a net:

1. Right-click the net on the Canvas and choose **Rename Net**. This opens the Rename Net dialog box.
2. Type in a new name for the net.

Note: The system automatically assigns net names to nets if they are not explicitly specified. Once you have specified a name for a net, that name will not be over-written by the system.

Automatic Names of Nets

Nets are automatically assigned names by the tool according to the following rules:

In order of priority

1. If user named then name = user name
2. If net is connected to top-level port then name = port name; if connected to multiple ports then pick first port
3. If the net has no driver, then name = net_[i]
4. If the net has a driver, name = instanceName_driverpinName

Slices

For slices, name = instanceName_driverpinName_sliceRange; for example u0_out1_4to6.

GND and VCC Nets

The default name for GND/VCC nets is net_GND and net_VCC.

Expanded Nets for Bus Interface Connections

Expanded nets for bus interface connections are named busInterfaceNetName_<i>_driverPinName.

Organizing Your Design on the Canvas

You may find it easier to create and navigate your SmartDesign if you organize and label the instances and busses on the Canvas.

You can show and hide nets, lock instances, rotate busses, group and ungroup pins, rename instances / groups / pins, and auto-arrange instances.

To organize your design:

1. Click the Auto-Arrange button to automatically arrange instances on the Canvas. SmartDesign's auto-arrange feature optimizes instance location according to connections and instance size.
2. Right-click any instance and choose Lock Location to fix the placement. Auto-Arrange will not move any instances that are locked.
3. Click Auto-Arrange again to further organize any unlocked instances. Continue arranging and locking your instances until you are satisfied with the layout on the Canvas.

If your design becomes too cluttered:

1. Hide the display of nets by de-selecting Canvas > Nets. This hides all the scalar and bus nets on your Canvas. You can also right-click a pin and choose Show Net (or Hide Net) to show/hide individual nets. Note that selecting a pin will make the corresponding net temporarily visible.
2. Group your pins. It may help to group pins that are functionally similar, or to group pins that are already connected or will be unused in your design.

To further customize your design's appearance:

1. Double-click the names of instances to add custom names. For example, it may be useful to rename an instance based on a value you have set in the instance: the purpose of an instance named 'array_adder_bus_width_5' is easier to remember than 'array_adder_0'.
2. Right-click any bus and choose Shape > Rotate Left or Right to change the bus orientation (horizontal or vertical). Click and drag the bus to a new location and lock, if necessary.

Grid

Grid Overview

The Grid (see image below) provides a mechanism for making manual connections between building blocks in your design. The grid displays your design in a spreadsheet for sorting and filtering, enabling you to quickly access and manipulate any subset of your design.

The Grid shows block instances vertically and horizontally on the spreadsheet, such that the port rows on the spreadsheet intersect with port columns. Each intersection of rows and ports on the spreadsheet provides a connection opportunity.

The grid is divided into two panels, the Display panel and the Connection panel.

The Grid offers two different views: the Instance-Instance view and the Net-Instance view. The behavior of the two panels is the same in both views.

The default display of the Grid shows connections between all the instances in your design in an Instance-Instance view.

Actel recommends that you work with only a subset of the instances in the current design when making manual connections. This greatly reduces the information displayed in the Grid view and makes it easier to create manual connections.

Click the Maximize Work Area button  to hide the other windows and show more of the Grid.

To create new Grids with just a subset of instances, select the instances between which you are making connections on the Canvas, then right-click and choose Edit Connections. A new Grid will be displayed, with only those instances and the top-level. When you are done making connections, right-click the grid view name tab and close the subset view.

To further simplify the data search in the grid and to make connections efficiently, use Filtering, Hierarchical sort in the instance-instance view, and the find unconnected ports (Hide All Connected Ports) features.

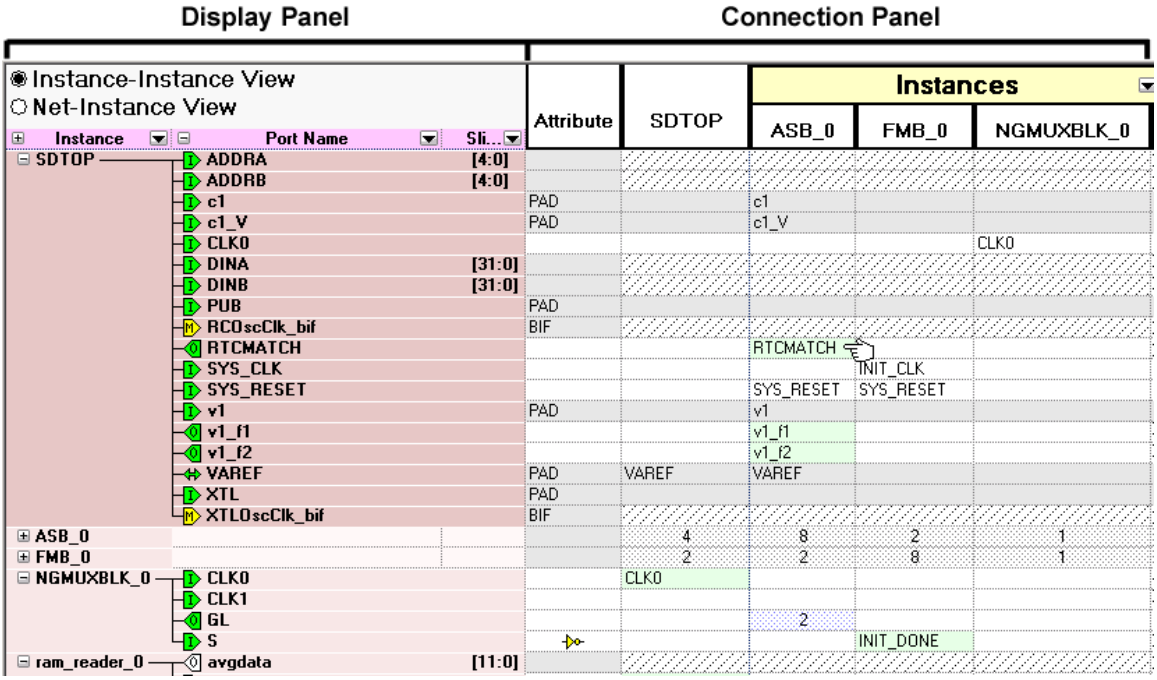


Figure 15 · Grid (Instance-Instance View)

To switch to Net-Instance view, click the Net-Instance view radio button.

To reset to the default view, from the **Grid** menu, choose **Reset Instance [Net] View to Default**.

See Also

Grid - Display panel icons

Grid - Connection panel icons

Display Panel

You can use the fields in the Display panel to manage content. To add or remove a field, right-click the field title (such as Instance in the image below) and from the right-click menu choose **Fields**. New fields appear to the right of the fields already shown. To filter the list of nets or instances in the Display panel, use the Custom Filter.

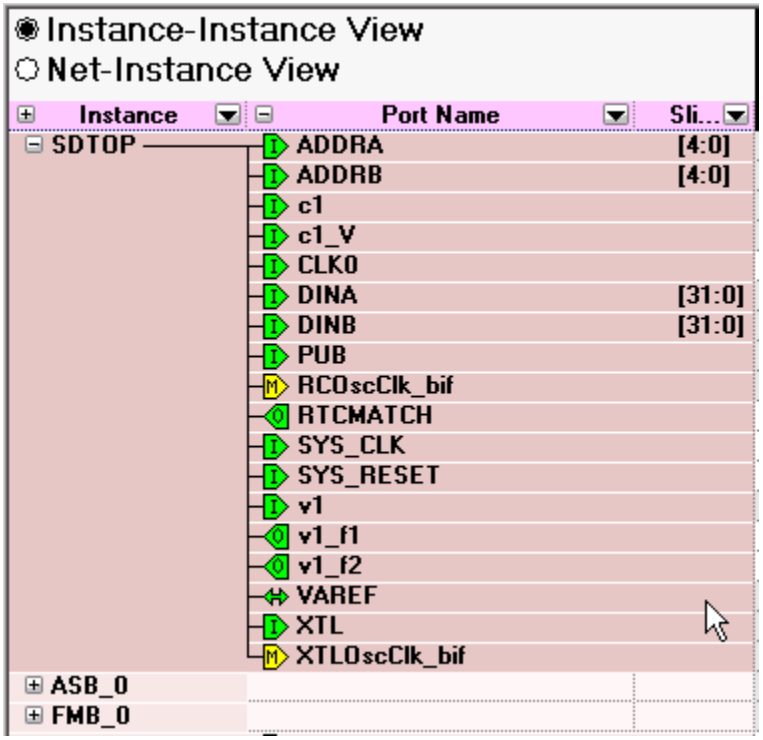


Figure 16 · Instance-Instance View Display Panel

The Display panel may list the following fields:

- **Instance:** Displays instances in the current design.
- **Direction:** Displays the port direction and bus interface type. Port directions are defined as IN, OUT and INOUT, bus interfaces are shown as MASTER, SLAVE, and SYSTEM.
- **Port Name:** Lists port names for all instances. Also displays an icon that indicates if the port is connected (green), disconnected (white), partially connected (green and white), input (I), output (O), master (yellow M), INOUT (small horizontal arrows), a system bif, or slave (S).
- **Slice:** Displays bit order (i.e. [7:0]) of busses and slices. Slice is not available for scalars and bus interfaces.
- **Width:** Displays the size of the bus for any bus port. One for a scalar and zero for a bus interface port.
- **Net**: Identifies the net for each instance connection.

Click the plus button to expand the information listed for the selected instance or direction. Click the minus button to collapse the information displayed for the selected instance or direction. You can add and remove fields to meet your needs.

Use the filter button to filter the contents of each column. To sort the content of a column, click the **Filter** button and select **Sort Ascending** or **Sort Descending**. Choose **Custom Filter** to open the Custom Filter dialog box. You can use the Custom Filter dialog box to choose the nets, instances and slices you wish to display.

Right-click the column heading and choose **Fit This Column To Data** to expand (or shrink) the column to match the column width to the size of the field name.

Promoting Ports to Top Level

To automatically promote a port to top level, select the port, right-click, and choose **Promote To Top Level**. This automatically creates top-level ports of that name and connects the selected ports to them. If a port name already exists, a choice is given to either connect to the existing ports or to create a new port with a name <port name>_<i> where i = 1…n.

Bus slices cannot be automatically promoted to top level. You must create a top level port of the bus slice width and then manually connect the bus slice to the newly created top level port.

Tying Off Input Pins

Click in the Grid Attribute column and select Invert, Tie Low, or Tie High to tie the Port.

Making Driver and Bus Interface Pins Unused

Driver or bus interface pins can be marked unused (floating/dangling) if you do not intend to use them as a driver in the design. If you mark a pin as unused the Connectivity Checker does not return Floating Driver or Unconnected Bus Interface messages on the pin.

Once a pin is explicitly marked as unused it cannot be used to drive any inputs. The unused attribute must be explicitly removed from the pin in order to connect it later. To mark a driver or bus interface pin as unused:

- Right-click the driver or bus interface pin and choose **Mark as Unused**
- In the Grid Attribute column, click the attribute and select **Mark as Unused**

Finding Unconnected and Partially Connected Ports

The grid allows you to quickly find all the unconnected ports in your design. To filter the grid to only show these ports, from the SmartDesign menu, choose Grid > Hide All Connected Ports.

Compatibility Rules

- If the port selected on the row is a top-level port with a direction IN or an instance port with direction OUT, all ports of direction IN and INOUT on the instances are compatible with it.
- If the port selected on the row is a top-level port with direction OUT or instance port with direction IN or INOUT, all ports with direction IN are compatible with it.
- Bus ports or slices are only compatible with bus ports or slices of equal size.
- If there are no compatible connections between a port in the row area and an instance in the column area, the cell is shaded and unavailable.
- The pull-down menu in the cells only lists compatible ports.

See Also

Connection panel

Making connections

Filtering views

Grid - Display panel icons

Connection Panel

The Connection panel (the area to the right side of the grid) shows the Attribute column, the "top" (top-level), and the Port Name to which the port is connected (if any).

Attribute	Top	Instances	
		Count8_0	my_block_0
PAD			AC1
PAD			AV0
PAD			AV1
PAD			PUB
		Aclr	SYS_RESET
			VRPU
PAD			XTL
PAD	VAREF		VAREF
	0	1	12
	SYS_R		
	Q[7:4]		
BIF	1	1	1
BIF			

Figure 17 · Instance-Instance Connection Panel

Use the filter  button to filter and select which columns you wish to view, or to sort the contents of the columns in ascending or descending order.

Attribute Column

The attribute column specifies additional properties of a port on the instance. These are:

PAD - Indicates that the port is a chip-level package pin. In SmartDesign, these ports are automatically promoted to the top-level and are read only.

BIF - Indicates that the port is a Bus Interface.

GND  - Tie the port to logic 0.

VCC - Tie the port to logic 1.

Invert - Invert the polarity of this port. Inverting a port automatically instantiates an inverter into the generated HDL file:

- For a driver: Inverter added after pin or port.
- For a non-driver: Inverter added before pin or port.

Unused - Indicates the pin has been assigned the float attribute and is not included in the Connectivity Check.

<design name> Column

The <design name> column represents the top-level; the name of the column depends on the name of your design.

Instances Column(s)

An instance column represents an instance that an instance-port of a row can be connected to.

See Also

Display panel

Making connections

Filtering views

Grid - Connection panel icons

Instance-Instance View

Instance-Instance View

The Instance-Instance view (see figure below) is divided into two panels: the Display panel and the Connection panel. By default, the Display panel shows Instance, Port Name, and Slice information.

By default, the Connection panel begins at the Attribute column, and lists instances in the design and their ports. You can show/hide any column in either panel; if you modify the view and wish to reset it, right-click the Instance-Instance View radio button in the Display panel and choose **Reset Instance View to Default**.

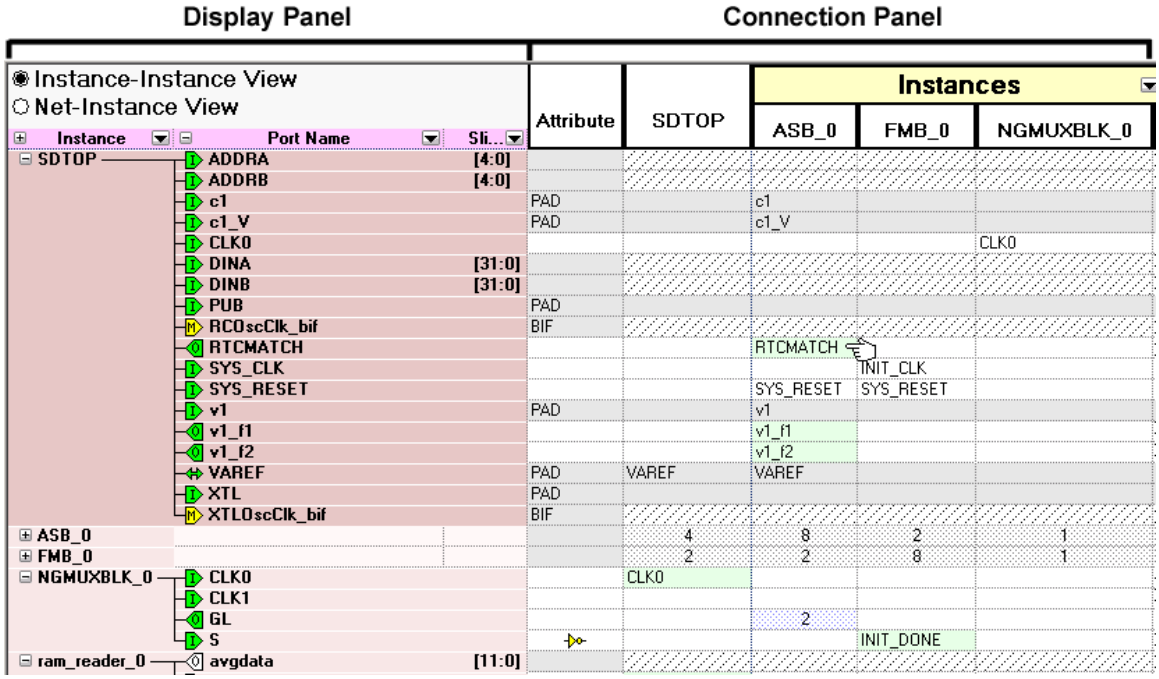


Figure 18 · Instance - Instance View

Adding and Removing Fields

To add a field in the Display panel, right-click the field title (such as Direction in the image below) and from the right-click menu choose **Field**, and select the field you wish to add or remove. Added fields appear at the end of the list of fields.

You can add fields to view additional information about a port. Also, adding the field enables you to Sort your design based on fields.

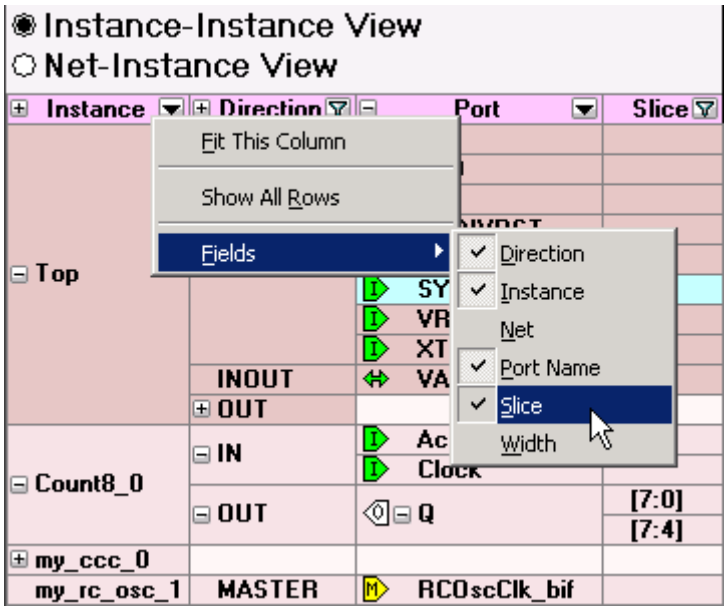


Figure 19 · Add Field Menu in Display Panel

To add an instance in the Connection panel, click the drop-down arrow in Instances (as shown in the figure below), and choose **Custom Filter**. The Custom Filter dialog box appears. Select checkbox for the instance you wish to view, or use the Find box to search for a specific instance or range of instances.

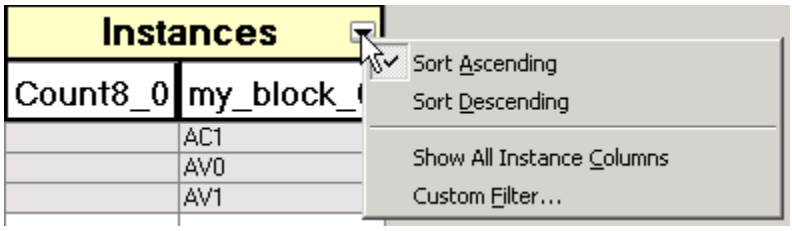


Figure 20 · Add an Instance with Custom Filter in Connection Panel

Sorting with Fields

The field columns inside the Grid can be used to sort the ports in your design.

The hierarchical order is defined by the order of the columns (left to right). The data within each field is sorted alphabetically. To change the hierarchical view, select a column and drag the column to the left or the right.

For example, this may be useful if you wish to see all of your INPUT ports together or if you want to see all of your 8-bit busses together. The image below shows the Display Panel sorted by Port Name.

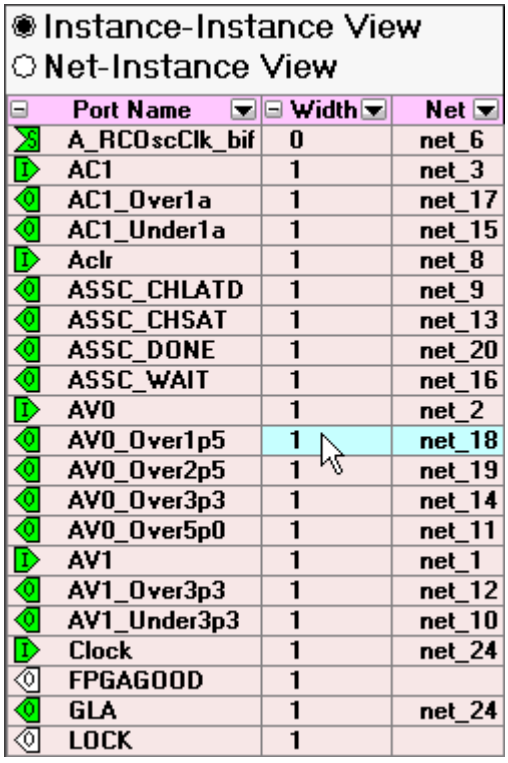


Figure 21 · Display Panel Sorted by Port Name

Making Connections Using the Grid

To make connections between ports on two instances:

1. Click in the intersection between the port (row) and the instance (column). SmartDesign displays a drop-down list of compatible ports from the instance on the column area.
2. Select the desired port to make the connection. In the figure below, the port SYS_RESET from the instance Top is being connected to port Aclr in the instance Count8_0. Note that the unconnected ports are shown in white.

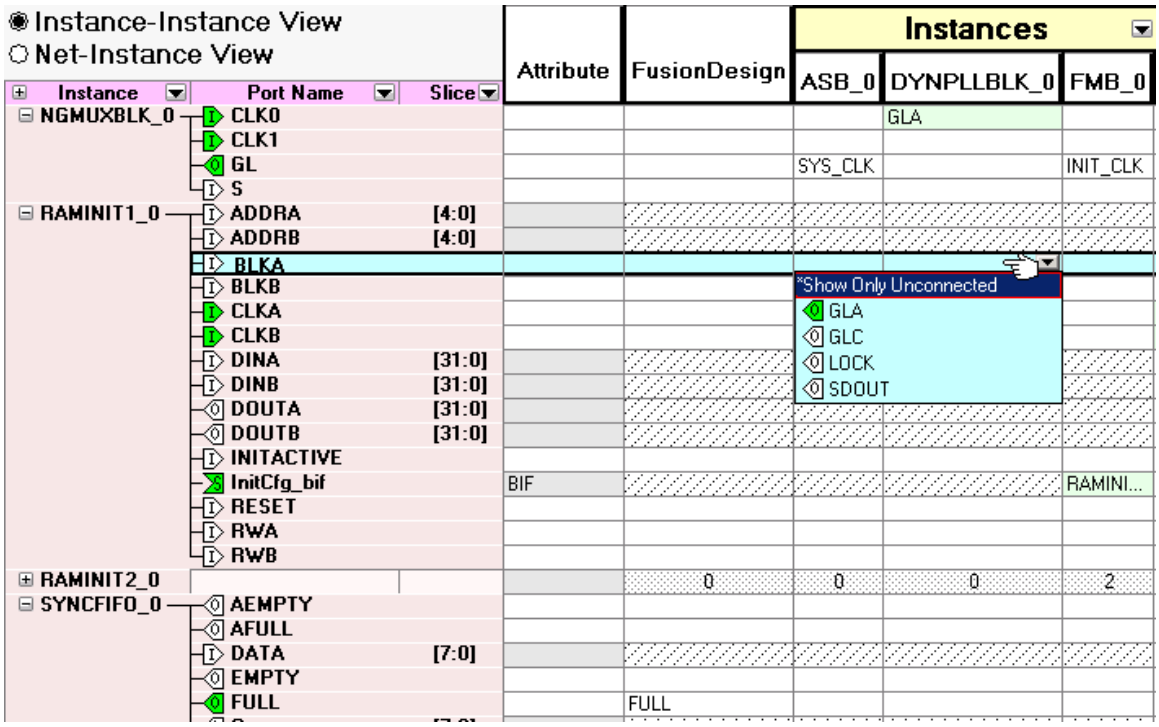


Figure 22 · Making Connections Between Two Ports on Two Instances

To disconnect an existing connection, click in the intersection between the port and the instance and choose **Disconnect**.

See Also

Connecting multiple ports (Connection panel)

Filtering views

Connecting Multiple Pins (Connection Panel)

The Connect Multiple dialog box enables you to make multiple connections to a pin or net.

In the Instance to Instance view you can easily connect multiple non-driver pins from a single instance to a driver pin. To do so:

1. Click a cell intersection of a driver pin and you will see a drop down with **Connect Multiple**. Choose **Connect Multiple** to open the dialog box below.

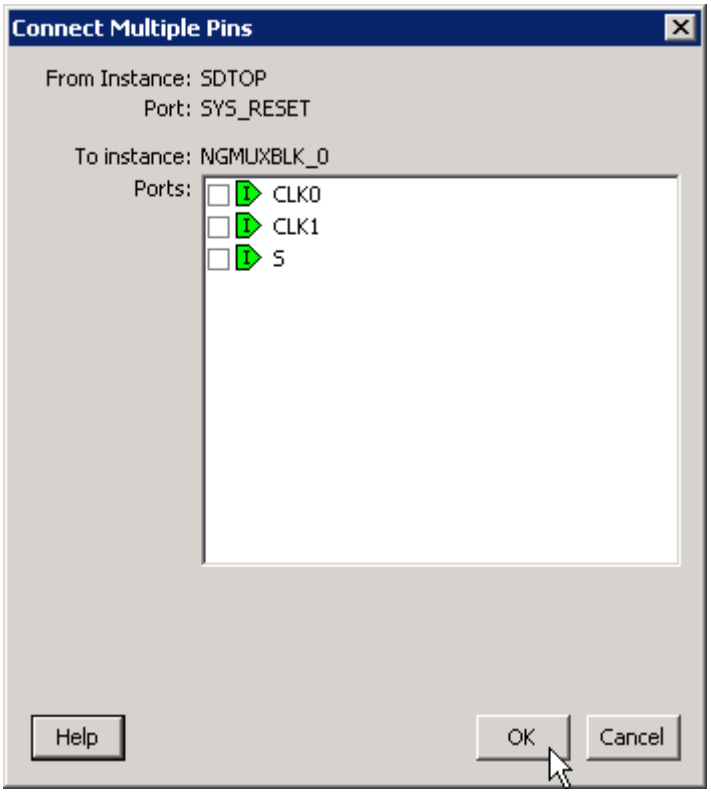


Figure 23 · Connect Multiple Pins Dialog Box - Instance to Instance

2. The dialog box lists all the compatible non-driver pins that can be connected to the selected driver pin. Click the checkbox to connect these pins to the driver pin.

In the Net to Instance view you can easily connect multiple pins from a single instance to a net. To do so:

1. Click a cell intersection of an existing net and you will see a drop down with **Connect Multiple**. Choose **Connect Multiple** to open the dialog box below. The dialog box lists all the compatible non-driver pins that can be connected to this net.

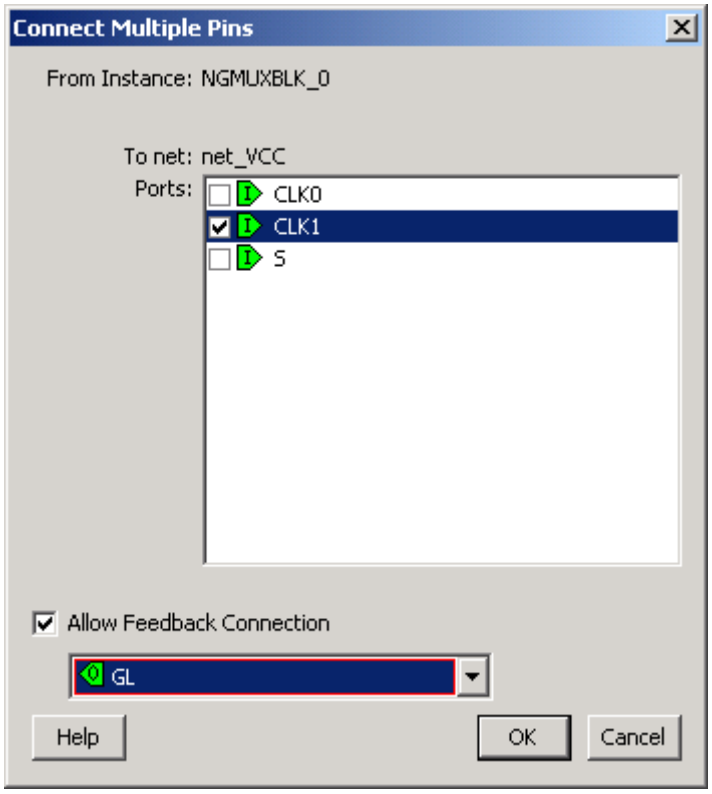


Figure 24 · Connect Multiple Pins Dialog Box - Net to Instance

2. Click the checkbox to connect these pins onto the net.
3. If the instance has driver pins available, you can click the checkbox for **Allow Feedback Connection** to select the driver pin for this net.

See Also

Filtering views

Connection panel

Net-Instance View

The Net-Instance view is a simplified version of the Instance-Instance view. Instead of an expandable list of every instance in your SmartDesign, the Display panel lists only the net names that are connected to an instance. This view is useful if you wish to see which nets are connected to an instance without changing your settings in the Instance-Instance view. The Display and Connection panels in the Net-Instance view behave the same in both views.

The default Display panel in Net-Instance view lists the nets in your design; the default Connection panel lists all instances (see figure below).

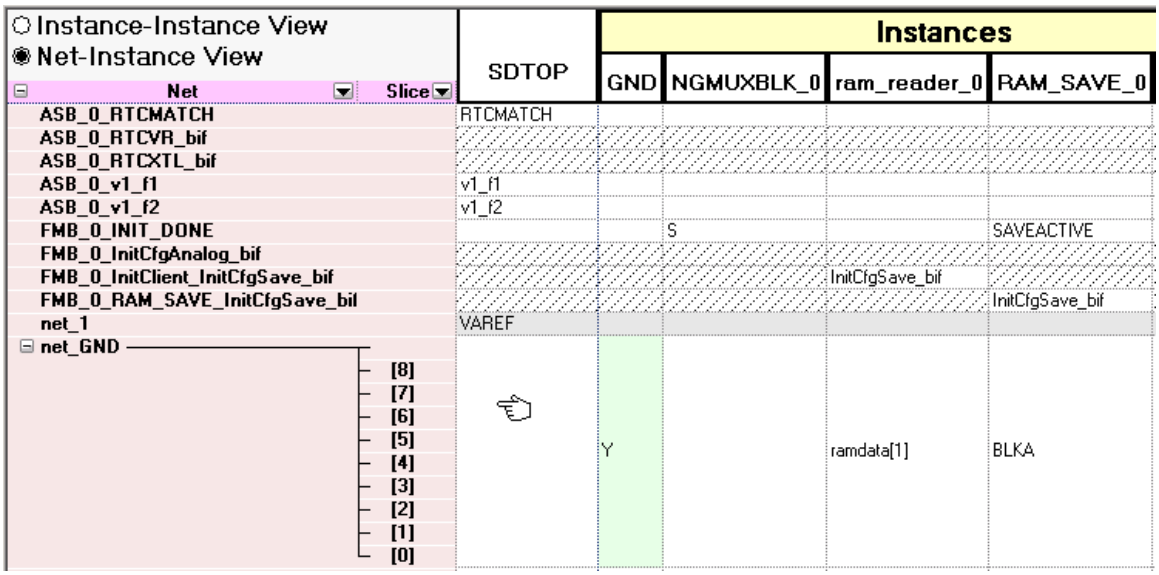


Figure 25 · Net-Instance View, Display and Connection Panels

To switch to Net-Instance view, click the **Net-Instance** radio button. To reset to the default view, from the **Grid** menu, choose **Reset Net View to Default**.

See Also

Connect to an existing net (Net-Instance view)

Connection panel

Display panel

Filtering views

Connect to an Existing Net (Net-Instance View)

To connect to an existing net, select the ports to be connected from the drop-down list by clicking in the cell at the intersection of the net and the instance (see figure below).

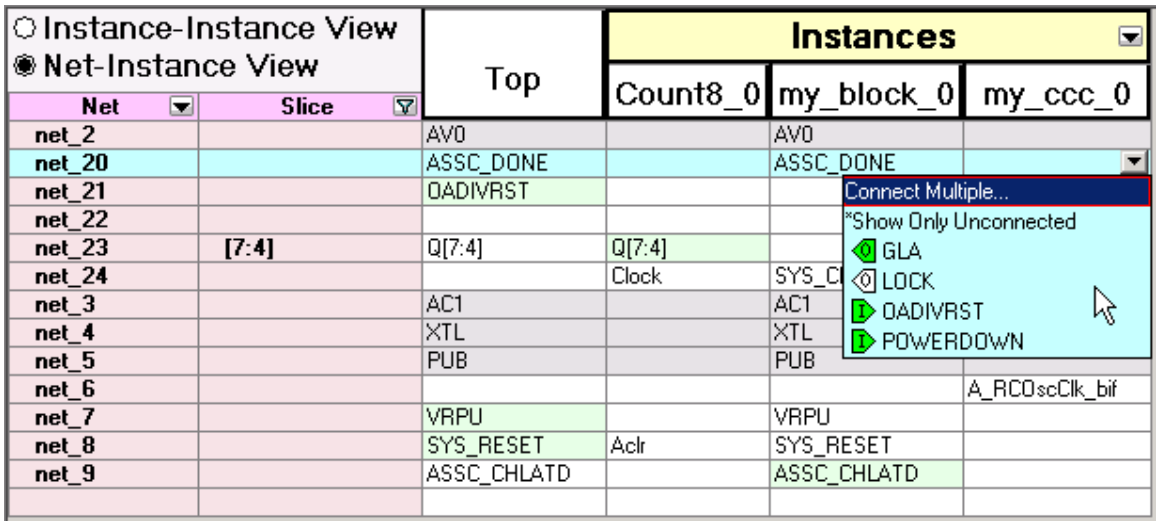


Figure 26 · Connecting to an Existing Net

Any net can have at most one driver. IN ports of the top-level or OUT ports from instances are considered drivers. If another driver is for an already driven net, the current driver will be disconnected and the new driver will be connected to the selected net.

See Also

Connection panel

Display panel

Make New Connection (Net-Instance View)

To connect to a new net, select the ports to be connected from the drop-down list. Click the cell at the intersection of the (unconnected) net row and the instance. This creates a new net (see figure below).

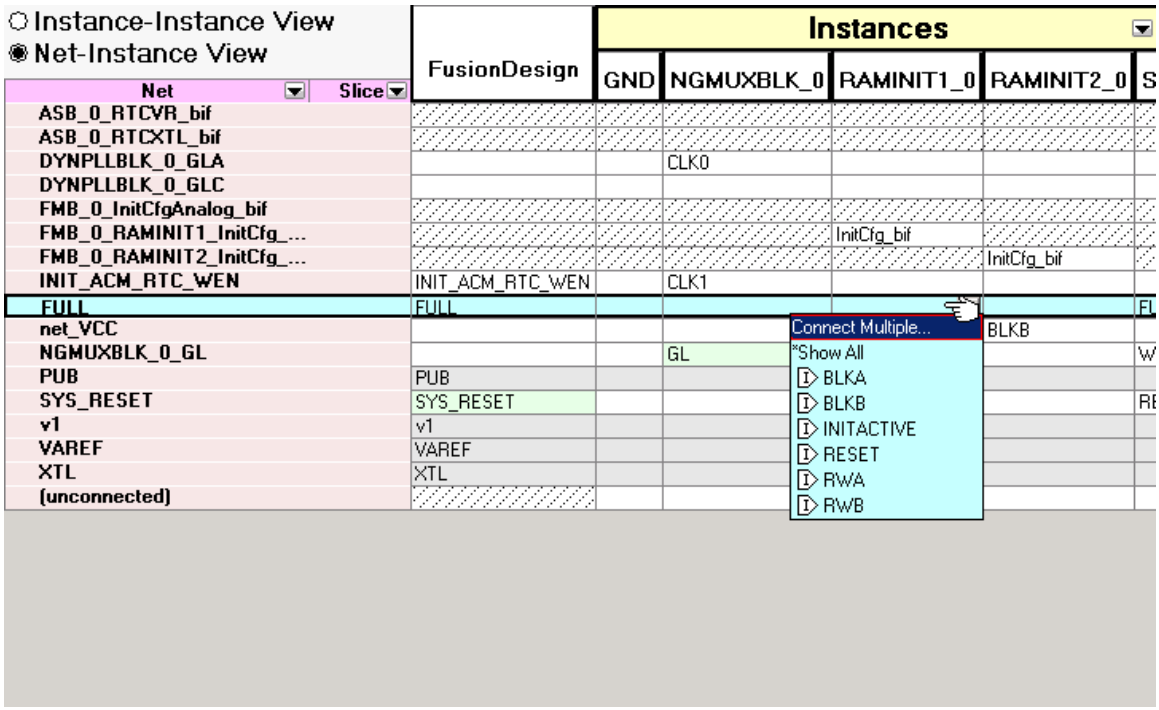


Figure 27 · Making a New Connection

See Also

Connect to an existing net (Net-Instance view)

Connection panel

Display panel

Filtering Views

To reduce the amount of data shown on the screen, you can display it selectively. The easiest way to hide an entry is to right-click the cell and choose **Hide Selection**. To show the entry again, you can right-click at the top and choose **Show All Rows**.

For more control over the data display, use the Custom Filter available from the button on the header row.

The Grid enables you to filter all instances within the design, as well as their direction, ports and slices. The example below filters by instance, but you can filter any column in the Display panel with the same procedure.

To filter the contents in the grid:

1. Use the filter button and choose **Custom Filter** to bring up the filter box (see figure below).

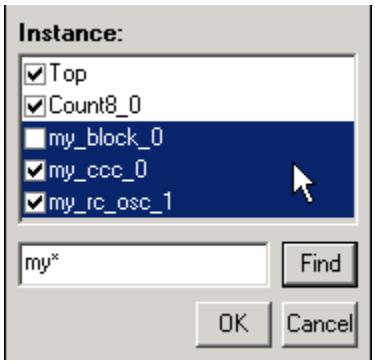


Figure 28 · Custom Filter Box in the Display Panel

2. From the filter box, you can find and select multiple values. In the image above, the Find field has highlighted all the instances that start with 'my', * is a wildcard. You must click inside the checkbox to select, or de-select, highlighted values.
3. Click OK to commit your changes.

To hide data in the grid:

Select the rows you want to hide, right-click and choose **Hide Selection**.

To restore grid data:

From the **SmartDesign** menu, choose **Connectivity View > Reset Instance View to Default**.

See Also

Connection panel

Display panel

Making connections

Schematic View

Schematic Overview

The Schematic view (see figure below) displays a detailed connection diagram for all instances, ports, and pins in the current design with lines representing nets. This view is the closest representation to the exported HDL.

You can zoom the contents in the Schematic view or split the Schematic view into multiple pages.

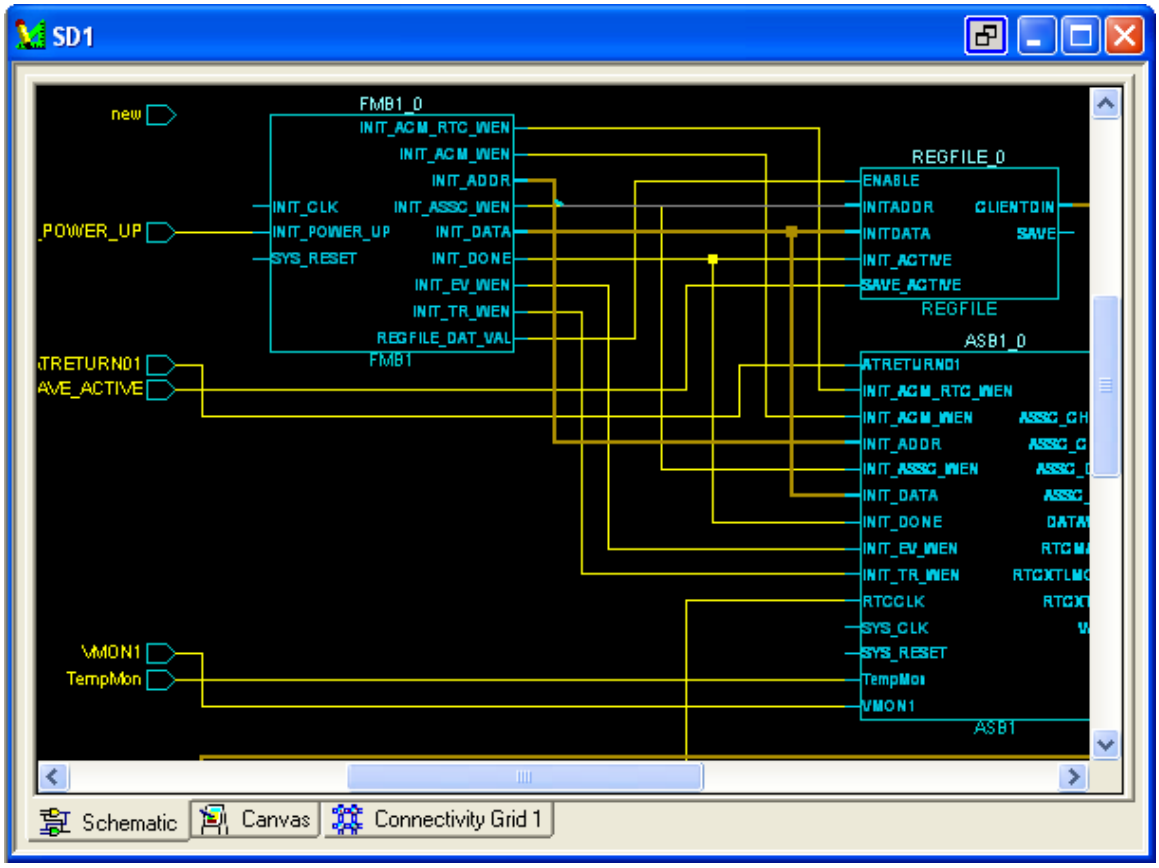


Figure 29 · Schematic View

Page Splitting

By default, the Schematic view displays large designs using multiple pages. Page splitting enables you to quickly compute and display the schematic. You can turn off page splitting to view your entire design on a single page. For larger designs, when this option is turned off, it may take SmartDesign longer to display the schematic.

To turn page splitting on or off, from the **SmartDesign** menu, choose **Schematic View > Allow Page Splitting**.

To navigate to the next page in a design, from the **SmartDesign** menu, choose **Schematic View > Go to Next Page**.

To navigate to the previous page, from the **SmartDesign** menu, choose **Schematic View> Go to Previous Page**.

To navigate to the first page, from the **SmartDesign** menu, choose **Schematic View > Go to First Page**.

To navigate to the last page, from the **SmartDesign** menu, choose **Schematic View> Go to Last Page**.

Zooming

The zoom tool in the Schematic View enables you to zoom fit the contents of your design within the window.

To zoom fit the design, click and drag to the bottom left corner of the window.

Zoom in and out of your schematic using the zoom icons on your toolbar.

Creating a SmartDesign

Adding Components and Modules (Instantiating)

SmartDesign components, SmartGen cores, IP cores, and HDL modules are displayed in the Hierarchy, Files, and Find output window.

To add a component, do either of the following:

- Select the component and drag it to the Canvas or Grid.
- Select a component, right-click, and choose **Instantiate in SmartDesign <name>.**

The component is instantiated in the design.

SmartDesign creates a default instance name. To rename the instance, double-click the instance name in the canvas.

Note: HDL modules with syntax errors cannot be instantiated in SmartDesign. However, since SmartDesign requires only the port definitions, the logic causing syntax errors can be temporarily commented out to allow instantiation of the component.

Adding a SmartDesign Component in a Higher-level Design (Instantiating)

SmartDesign components can be instantiated into another SmartDesign component.

Once a SmartDesign is generated, the exported netlist can be instantiated into HDL like any other HDL module.

Adding Top Level Ports / Renaming External Pads in a SmartDesign

You can add ports to, and/or rename ports in your SmartDesign.

To add ports:

1. From the **SmartDesign** menu, choose **Logic > Add port**. The Add Port dialog box appears (as shown below).

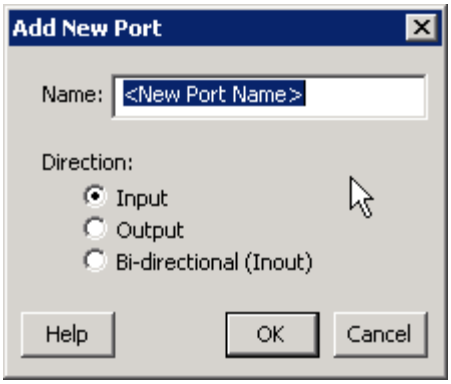


Figure 30 · Add New Port Dialog Box

2. Specify the name of the port you wish to add. You can specify a bus port by indicating the bus width directly into the name using brackets [ ], such as mybus[3:0].
3. Select the direction of the port.

To remove a port from the top level, select the port in the Grid, right-click and choose **Delete Top Level Port**.

To rename a top-level port, right-click the top-level non-pad port and choose **Modify Top Level Port**. You can rename the port, change the bus width (if the port is a bus), and change the port direction.

To rename an external pad:

1. Right-click a pad in the top-level port and select **Rename External Pad**. The Rename External Pad dialog box appears, as shown in the figure below.

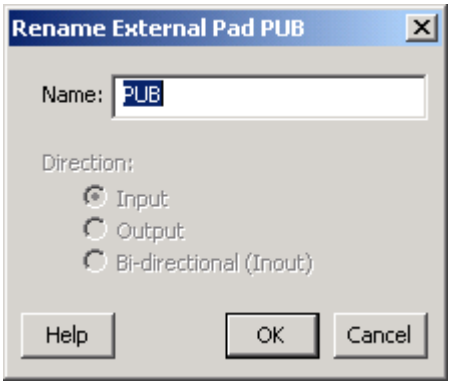


Figure 31 · Rename External Pad Dialog Box

2. Enter the new name for the external pad and click **OK**.

See Also

Top level connections

Connecting Instances

Automatic Connections

Using automatic connections (as shown in the figure below) enables the software to connect your design efficiently, reducing time required for manual connections and the possibility of introducing errors.

To auto connect the bus interfaces in your design, right-click the design Canvas and select **Auto Connect**, click the Auto Connect button ; or from the **SmartDesign** menu, choose **Auto Connect**.

You can select individual pins or groups on the Canvas to auto-connect. Select the pins, right-click and choose Auto Connect.

SmartDesign searches your design and connects all compatible bus interfaces.

SmartDesign will also form known connections for any SoC systems such as the processor CLK and RESET signals.

If there are multiple potential interfaces for a particular bus interface, Auto Connect will not attempt to make a connection; you must connect manually. You can use the Canvas, Grid or the Find Compatible Bus Interface dialog box to make the manual connection.

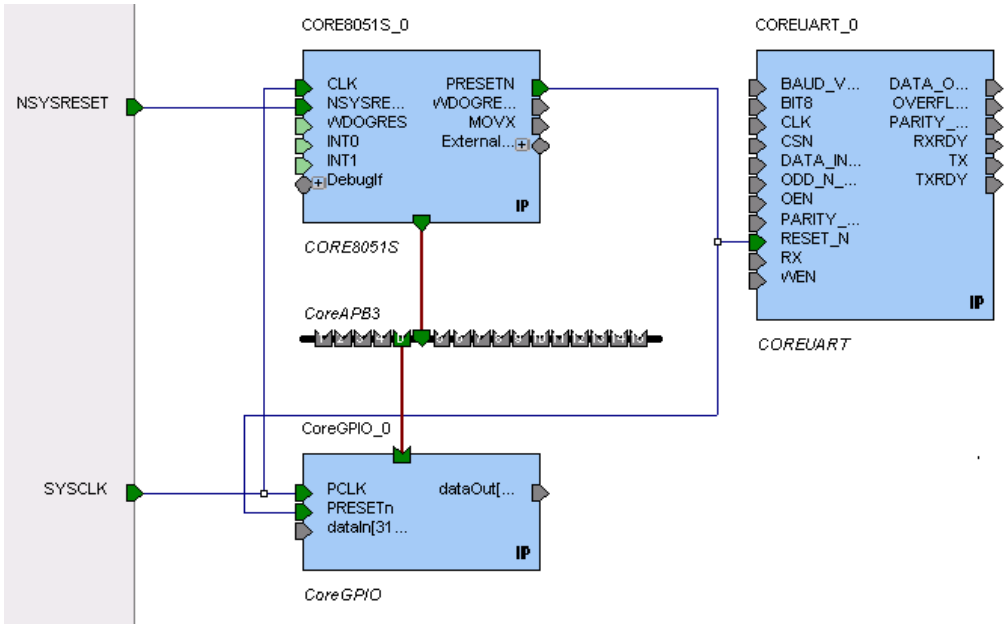


Figure 32 · Auto-Connected IP Cores

Manual Connections

To make manual connections between to pins on the Canvas, select both pins (use CTRL + click), right-click either pin and choose **Connect**. If the pins cannot be legally connected the connection will fail.

Deleting Connections

To delete a net connection on the Canvas, click to select the net and press the Delete key, or right-click and choose **Delete**.

To remove all connections from one or more instances on the Canvas, select the instances on the Canvas, right-click and choose **Clear all Connections**. This disconnects all connections that can be disconnected legally.

You can also select one or more rows in the Grid and choose **Remove Connections from Selected Ports** from the right-click menu to remove the connects for a group of Ports.

If you click in a cell displaying a connection, selecting **Disconnect** from the drop down removes just that connection.

Certain connections to ports with PAD properties cannot be disconnected. PAD ports must be connected to a design's top level port. PAD ports will eventually be assigned to a package pin. In SmartDesign, these ports are automatically promoted to the top level and cannot be modified or disconnected.

Top-Level Connections

Connections between instances of your design normally require an OUTPUT (Driver Pin) on one instance to one or more INPUT(s) on other instances. This is the basic connection rule that is applied when connecting.

However, directions of ports at the top level are specified from an external viewpoint of that module. For example, an INPUT on the top level is actually sending ('driving') signals to instances of components in your design. An OUTPUT on the top level is receiving ('sinking') data from a Driver Pin on an internal component instance in your SmartDesign design.

The implied direction is essentially reversed at the top-level. Making connections from an OUTPUT of a component instance to an OUTPUT of top-level is legal.

This same concept applies for bus interfaces; with normal instance to instance connections, a MASTER drives a SLAVE interface. However, they go through a similar reversal on the top-level.

Bus Interfaces

About Bus Interfaces

A bus interface is a standard mechanism for specifying the interconnect rules between components or instances in a design. A bus definition consists of the roles, signals, and rules that define that bus type. A bus interface is the instantiation of that bus definition onto a component or instance.

The available roles of a bus definition are master, slave, and system.

A master is the bus interface that initiates a transaction (such as read or write) on a bus.

A slave is the bus interface that terminates/consumes a transaction initiated by a master interface.

A system is the bus interface that does not have a simple input/output relationship on both master/slave. This could include signals that only drive the master interface, or only drive the slave interface, or drive both the master and slave interfaces. A bus definition can have zero or more system roles. Each system role is further defined by a group name. For example, you may have a system role for your arbitration logic, and another for your clock and reset signals.

Mirror roles are for bus interfaces that are on a bus core, such as CoreAHB or CoreAPB. They are equivalent in signal definition to their respective non-mirror version except that the signal directions are reversed.

The diagram below is a conceptual view of a bus definition.

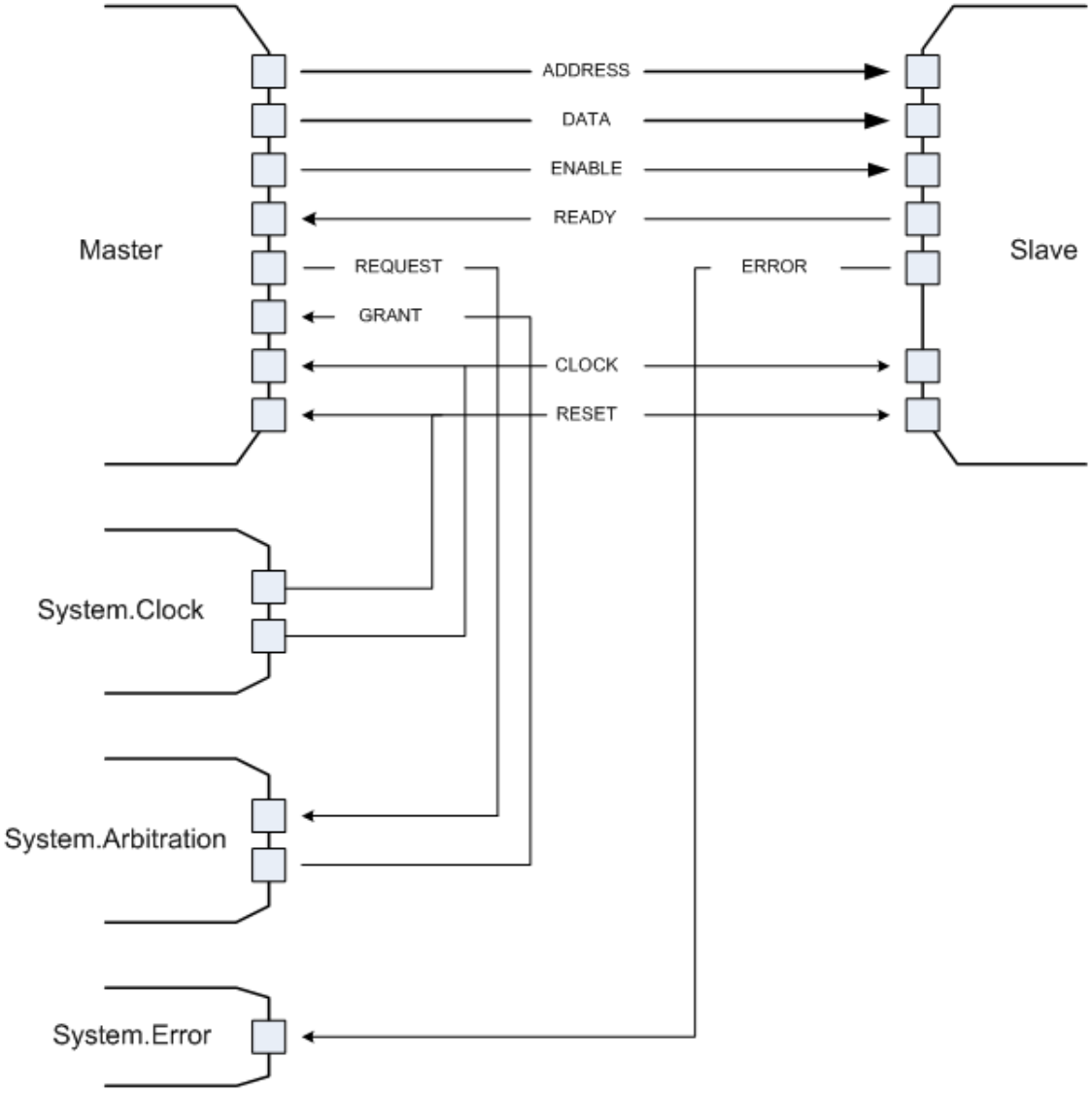


Figure 33 · Bus Definition

See Also:

Using bus interfaces in SmartDesign

Using Bus Interfaces in SmartDesign

Adding bus interfaces to your design enables SmartDesign to do the following:

- Auto connect compatible interfaces
- Enforce DRC rules between instances in your design
- Search for compatible components in the project

The Catalog in the Project Manager contains a list of Actel-specific and industry standard bus definitions, such as AMBA.

You can add bus interfaces to your design by dragging the bus definitions from the Bus Definitions tab in the Catalog onto your instances inside SmartDesign.

Some Actel SmartGen cores have bus interfaces that are instantiated during generation.

Certain bus definitions cannot be instantiated by a user. Typically these are the bus definitions that define a hardwired connection and are specifically tied to a core/macro. They are still available in the catalog for you to view their properties, but you will not be able to add them onto your own instances or components. These bus definitions are grayed out in the Catalog.

A hardwired connection is a required silicon interconnect that must be present and specifically tied to a core/macro. For example, when using the Real Time Counter in a Fusion design you must also connect it to a Crystal Oscillator core.

Maximum masters allowed - Indicates how many masters are allowed on the bus.

Maximum slaves allowed - Indicates how many slaves are allowed on the bus.

Default value - indicates the value that the input signal will be tied to if unused. See Default tie-offs with bus interfaces.

Required connection - Indicates if this bus interface must be connected for a legal design.

Hover your mouse over a bus definition in the Project Manager Bus Definition Catalog to view the masters/slave/default/required connection information.

Adding Bus Interfaces to SmartDesign Components

To add a bus interface to a component:

1. Select a bus definition from the Bus Definitions tab in the catalog and drag it onto your top-level. The Add Bus Interface dialog box opens (see figure below). A default name is assigned to your bus interface; you can specify your own if you wish.

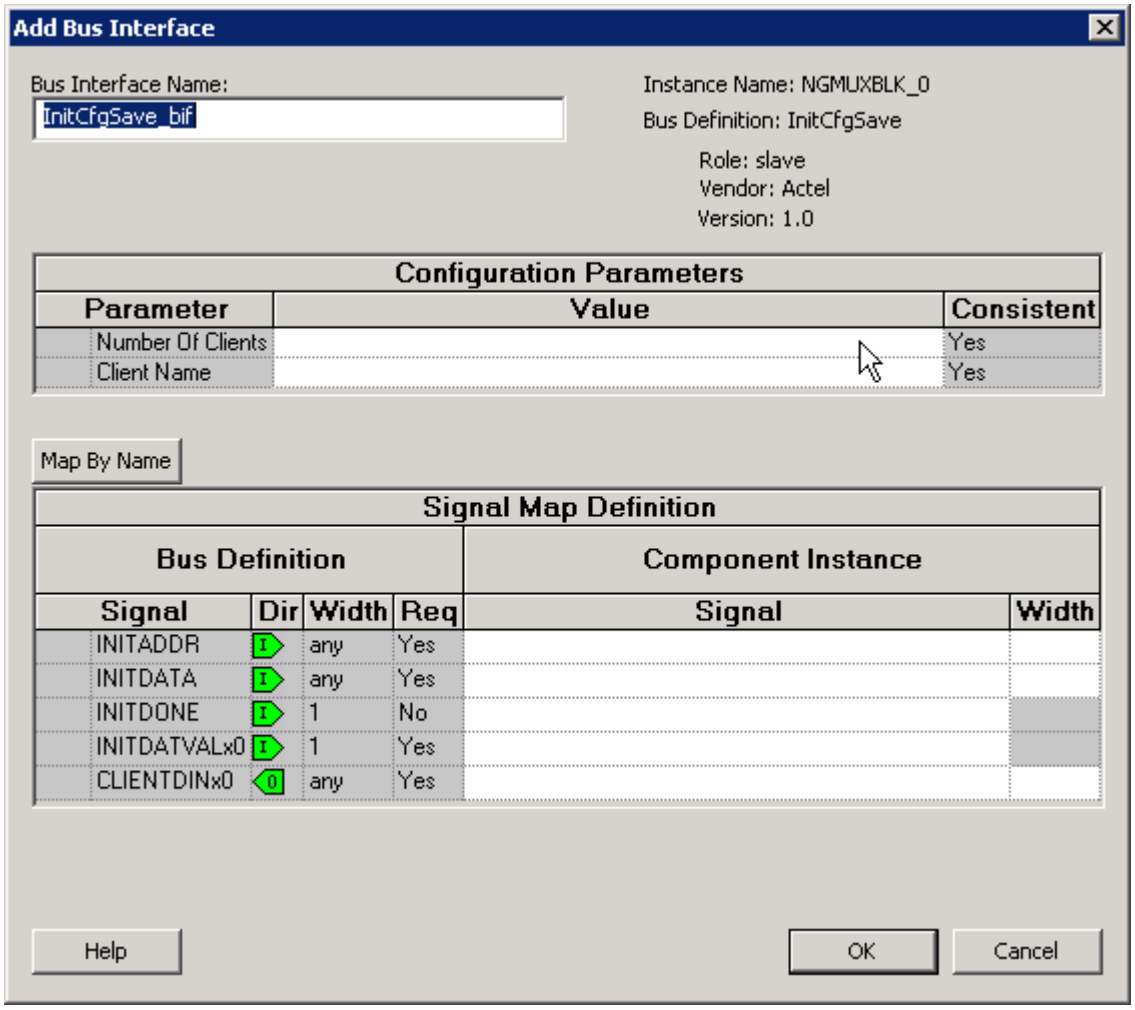


Figure 34 · Add Bus Interface Dialog Box

2. Click **Map by Name** to map the signals automatically. Map By Name attempts to map any similar signal names between the bus definition and pin names on the instance.
3. (Optional) Click the **Add Port** checkbox to add ports to the top-level. If you choose to add ports, the Signal row becomes a text editable field.

Adding Bus Interfaces to SmartDesign Instances

To add a bus interface to your instance:

1. Select a bus definition from the Bus Definition tab in the Catalog and drag it onto your instance. The Add Bus Interface dialog box opens (see figure below). A default name is assigned to your bus interface; you can specify your own if you wish.

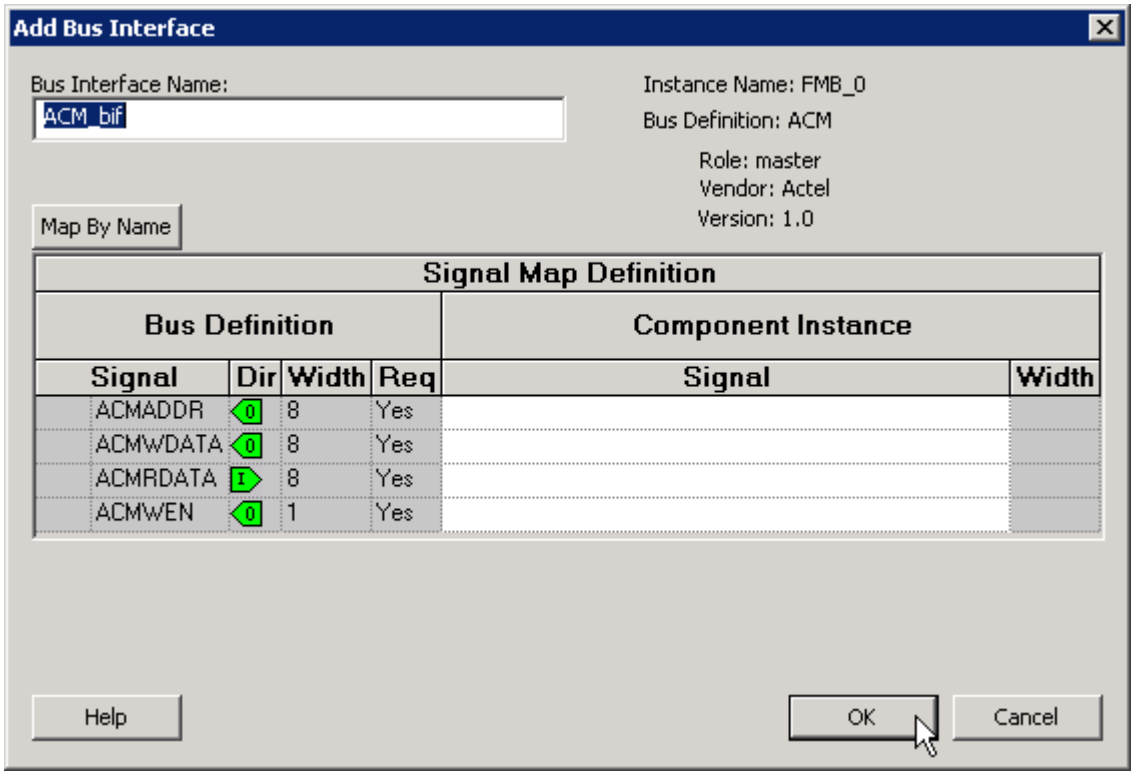


Figure 35 · Add Bus Interface Dialog Box

2. If necessary, enter the configuration parameters.
3. Click **Map by Name** to map the signals automatically. Map By Name attempts to map any similar signal names between the bus definition and pin names on the instance.

Removing Bus Interfaces from Instances

Only bus interfaces that you explicitly added to an instance can be removed or deleted. Bus interfaces that were instantiated as part of core generation cannot be deleted.

To delete user added bus interfaces, on the Canvas, select the bus interface pin object, right-click, and choose **Delete Bus Interface**; or, in the Grid, select the **Port Name** field, right-click, and choose **Delete Bus Interface**.

Viewing Bus Interface Properties

To view the properties of a bus interface:

In the Canvas, select the bus interface pin object, right-click, and choose **Properties.** This opens the View Bus Interface dialog box (see figure below).

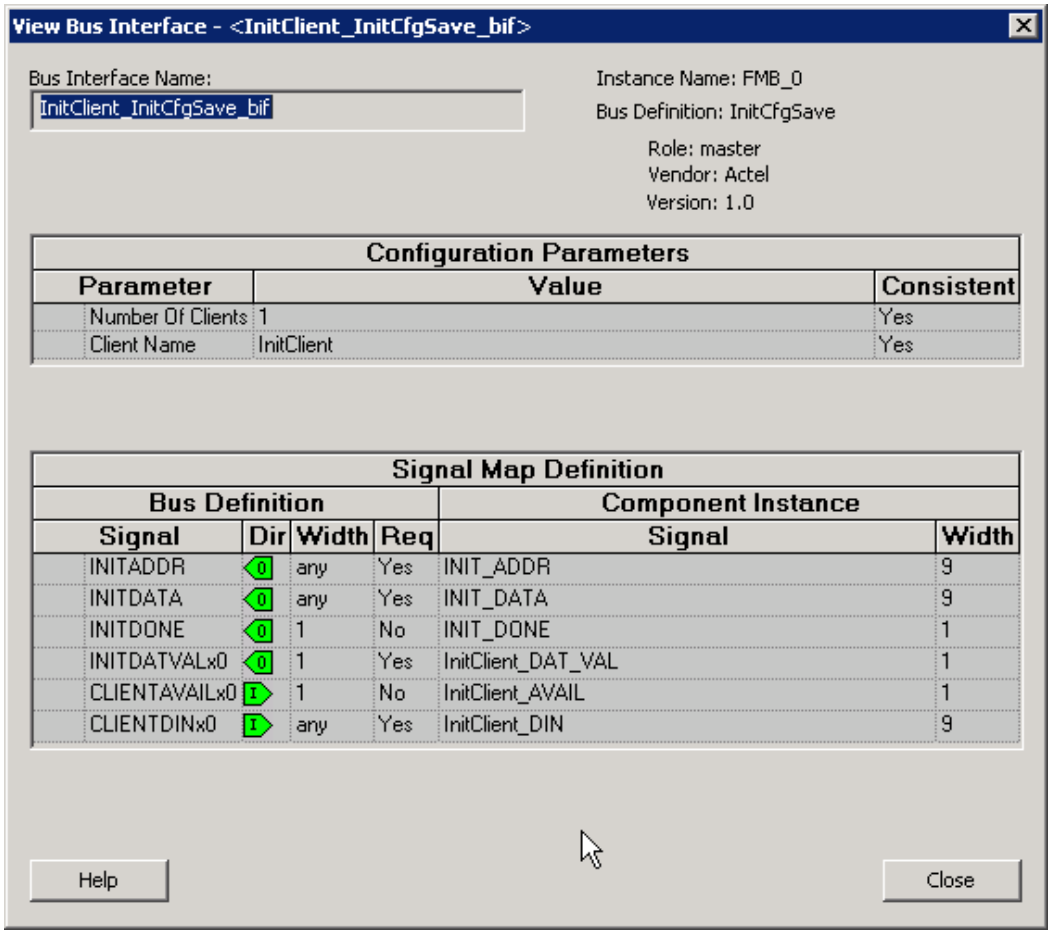


Figure 36 · View Bus Interface Properties Dialog Box

Bus Interface Details

Bus Interface Name: Name of bus interface.

Instance Name: Specifies the name of the instance.

Bus Definition: Specifies the name of the bus interface.

Role: Specifies the bus role (master or slave).

Vendor: Specifies the vendor for the bus interface.

Version: Specifies the version for the bus interface.

Configuration Parameters

Certain bus definitions contain user configurable parameters.

Parameter: Specifies the parameter name.

Value: Specifies the value you define for the parameter.

Consistent: Specifies whether a compatible bus interface must have the same value for this bus parameter. If the bus interface has a different value for any parameters that are marked with consistent set to **yes**, this bus interface will not be connectable.

Signal Map Definition

The signal map of the bus interface specifies the pins on the instance that correspond to the bus definition signals. The bus definition signals are shown on the left, under the **Bus Interface Definition**. This information includes the name, direction, width, and required properties of the signal.

The pins for your instance are shown in the columns under the Component Instance. The signal element is a drop-down list of the pins that can be mapped for that definition signal. Only pins that have the same direction and width requirements will be shown.

If the Req field of the signal definition is Yes, you must map it to a pin on your instance for this bus interface to be considered legal. If it is No, you can leave it unmapped.

If the Width field is *Any* there is no restriction on the width for this definition signal. That means a pin of any width on your instance can be mapped to this signal. During bus interface connection, if the instance pins are of differing widths, the bit connections will start from right to left. For example, if a 16-bit bus is connected to an 8-bit bus, the 8-bit bus will be connected to bits 7 down to 0 of the 16-bit bus. The higher bits will be unmapped and tied off at generation time.

Modifying Bus Interface Details

Only bus interfaces that you explicitly added to an instance can be modified. Bus interfaces that were instantiated as part of SmartGen core generation cannot be modified.

To modify the properties of a bus interface:

1. In the Canvas, select the bus interface pin object, right-click, and choose **Modify Bus Interface** (see figure below).

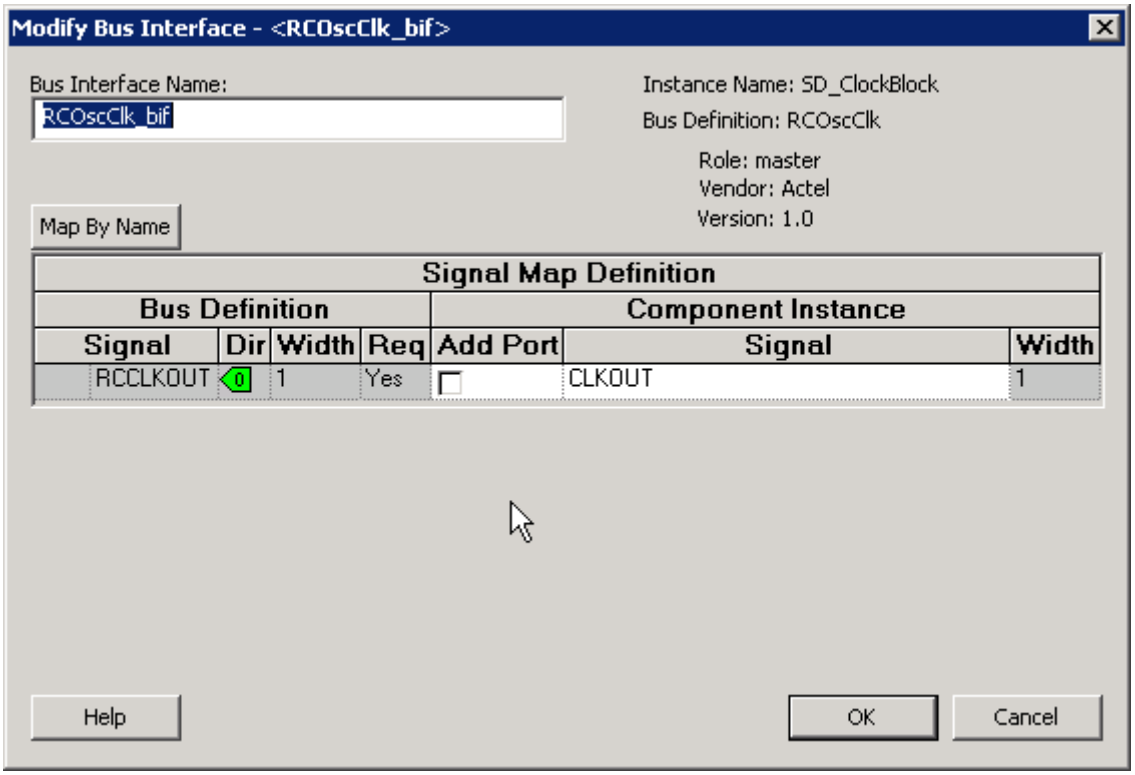


Figure 37 · Modify Bus Interface Dialog Box

2. Modify the bus interface details, configuration parameters, or signal map definition and click **OK**.

Map By Name attempts to map any similar signal names between the bus definition and pin names on the instance.

Finding Compatible Bus Interfaces

The SmartGuide feature helps you complete your design; when you have a specific bus interface on an instance, you can find a compatible instance, component, or core to connect.

To find a compatible bus interface:

1. In the Canvas, select the bus interface pin object, right-click, and choose **Find Compatible Bus Interface**. This brings up the Find Compatible Bus Interface dialog box, showing the compatible instances, components, or cores that have the bus interface.

SmartGuide searches all the instances in the current SmartDesign for any compatible bus interfaces. SmartGuide also searches through all the configured components in the Libero IDE project for any compatible bus interfaces, then searches through the Cores Catalog for any cores that may potentially contain a compatible bus interface when generated.

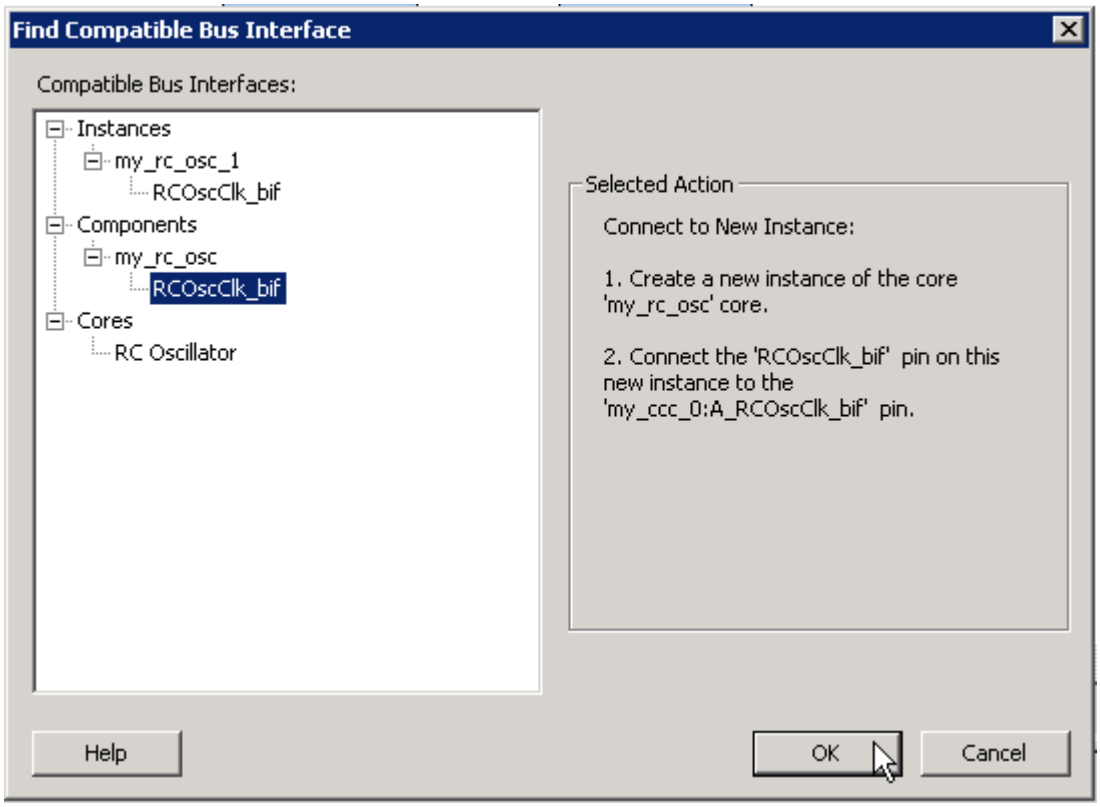


Figure 38 · Find Compatible Bus Interface Dialog Box

2. Select a compatible instance, component or core and click **OK**.

- Selecting an instance from this list automatically connects that instance to the selected bus interface.
- Selecting a component from this list automatically instantiates that component into the design and connects it to the selected bus interface.
- Selecting a core from this list automatically brings up the configurator for that core and enables you to generate a new core. It will then be added to the design and connected. Note that it is possible to configure a core such that no compatible bus interface is generated; you will be given the opportunity to reconfigure the core in this scenario.

Actel Bus Interfaces

The Catalog provides the following Actel-specific bus interfaces:

ExtSeqCtrl

This bus interface defines the set of signals required to interface to the Analog System External Sequence Control. If the Analog System is configured with more than a single procedure, it will export this bus interface. Your own logic would need to connect to this bus interface to properly communicate and control the sequencer.

RTCXTL

This bus interface represents the hardwired connection needed between the Real Time Counter and the Crystal Oscillator.

RTCVR

This bus interface represents the hardwired connection needed between the Real Time Counter and the Voltage Regulator Power Supply Monitor.

InitCfg

This is the initialization and configuration interface that is generated as part of the Flash Memory Builder. Any clients can be initialized from the Flash Memory as long as it can connect to this bus interface. This is for pure initialization clients that do not require save-back to the Flash Memory.

InitCfgSave

This is the initialization and configuration interface that is generated as part of the Flash Memory Builder. Any client can be initialized or saved-back to the Flash Memory as long as it can connect to this bus interface. This is for clients that require initialization and save-back capabilities to the Flash Memory.

InitCfgCtrl

This interface is used to initiate the save-back procedure of the Flash Memory.

InitCfgAnalog

This interface is required between the Flash Memory System and the Analog System core.

FlashDirect

This bus interface defines the set of signals that are required to interface directly to the Flash Memory. From the Flash Memory, if you add a data storage client, this interface will be exported. Interfacing to this interface enables direct access to the Flash Memory.

XTLOscClk

This interface represents the Crystal Oscillator clock.

RCOscClk

This interface represents the RC Oscillator clock.

DirectCore Bus Interfaces

The Catalog provides the following DirectCore bus interfaces.

AHB

The AMBA AHB defines the set of signals for a component to connect to an AMBA AHB bus.

APB

The AMBA APB defines the set of signals for a component to connect to an AMBA Peripheral Bus.

SysInterface

The SysInterface is the interface used between the CoreMP7 and CoreMP7Bridge cores.

DBGInterface

This is the set of debug ports on the CoreMP7 core.

CPInterface

This is the co-processor interface on the CoreMP7 core.

Default Tie-Offs with Bus Interfaces

Bus definitions can contain default values for each of the defined signals. These default values specify what the signal should be tied to if it is mapped to an unconnected input pin on the instance.

Bus definitions are specified as required connection vs optional connection that defines the behavior of tie-offs during SmartDesign generation.

Required bus interfaces - The signals that are not required to be mapped will be tied off if they are mapped to an unconnected input pin.

Optional bus interfaces - All signals will be tied off if they are mapped to an unconnected input pin.

Tying Off (Disabling) Unused Bus Interfaces

Tying off (disabling) a bus interface sets all the input signals of the bus interface to the default value.

To tie off a bus interface, right-click the bus interface and select Tie Off.

This is useful if your core includes a bus interface you plan to use at a later time. You can tie off the bus interface and it will be disabled in your design until you manually set one of the inputs.

Some bus interfaces are required; you cannot tie off a bus interface that is required. For example, the Crystal Oscillator to RTC (RTCXTL) bus interface is a silicon interface and must be connected.

To enable your pin, right-click the pin and choose **Clear Attribute**.

Required vs. Optional Bus Interfaces

A required bus interface means that it must be connected for the design to be considered legal. These are typically used to designate the silicon interconnects that must be present between certain cores. For example, when using the Real Time Counter in a Fusion design you must also connect it up to a Crystal Oscillator core.

An optional bus interface means that your design is still considered legal if it is left unconnected. However, it may not functionally behave correctly.

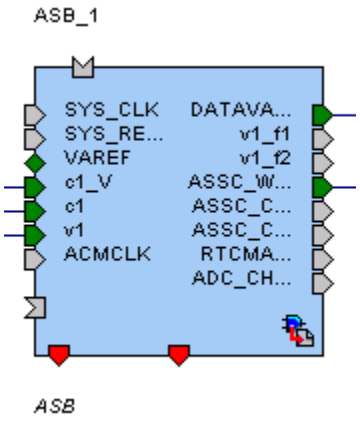


Figure 39 · Required Unconnected, Optional Unconnected, and Connected Bus Interfaces

See Also

Canvas icons

Promoting Bus Interfaces to Top-Level

To automatically connect a bus interface to a top-level port, select the bus interface, right-click, and choose **Promote To Top Level**.

This automatically creates a top-level bus interface port of that name and connects the selected port to it. If a bus interface port name already exists, a choice is given to either connect to the existing bus interface port or to create a new bus interface port with a name <port name>_<i> where i = 1...n.

The signals that comprise the bus interface are also promoted.

Promoting a bus interface is a shortcut for creating a top-level port and connecting it to an instance pin.

Incremental Design

Reconfiguring a Component

To reconfigure a component used in a SmartDesign:

- In the Canvas, select the instance and double-click the instance to bring up the appropriate configurator, such as SmartGen, or the HDL editor; or select the instance, right-click it, and choose **Configure Component**.
- Select the component in the Hierarchy tab, Files tab or Find output window, and from the right-click menu select **Open Component**.

When the configurator is launched from the canvas, you cannot change the name of the component.

See Also

Design state management

Replacing components

Fixing an Out-of-Date Instance

Any changes made to the component will be reflected in the instance with an exclamation mark  when you update the definition for the instance. An instance may be out-of-date with respect to its component for the following reasons:

- If the component interface (ports) is different – after reconfiguration - from that of the instance
- If the component has been removed from the project
- If the component has been moved to a different VHDL library
- If the SmartDesign has just been imported

You can fix an out-of-date instance by:

- Replacing the component with a new component (as shown in the figure below)
- Updating with the latest component

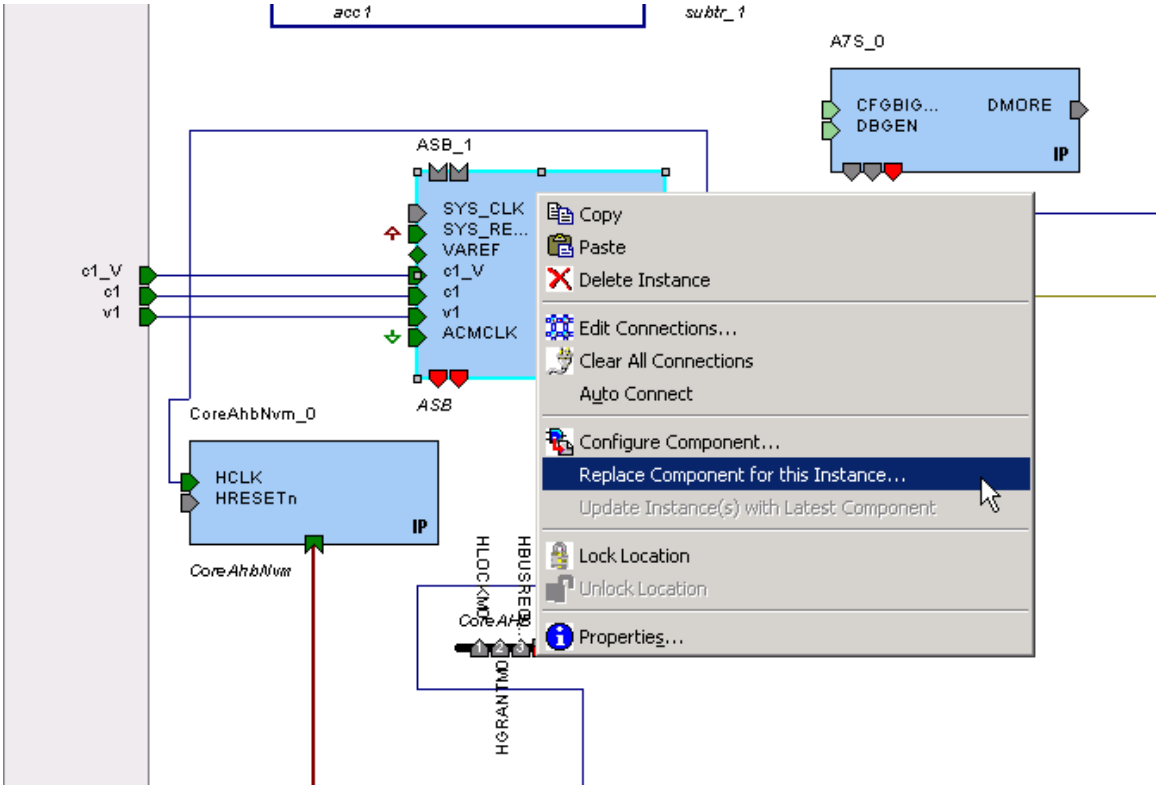


Figure 40 · Right-Click Menu - Replace Component for this Instance

See Also

Design state management

Reconfiguring components

Replacing components

Replacing Components

Components of an instance on the Canvas can be replaced with another component and maintain connections to all ports with the same name.

To replace a component in your design:

1. Select the component on the Canvas, right-click, and choose **Replace component for this Instance**. The Replace Component dialog box appears (see figure below).

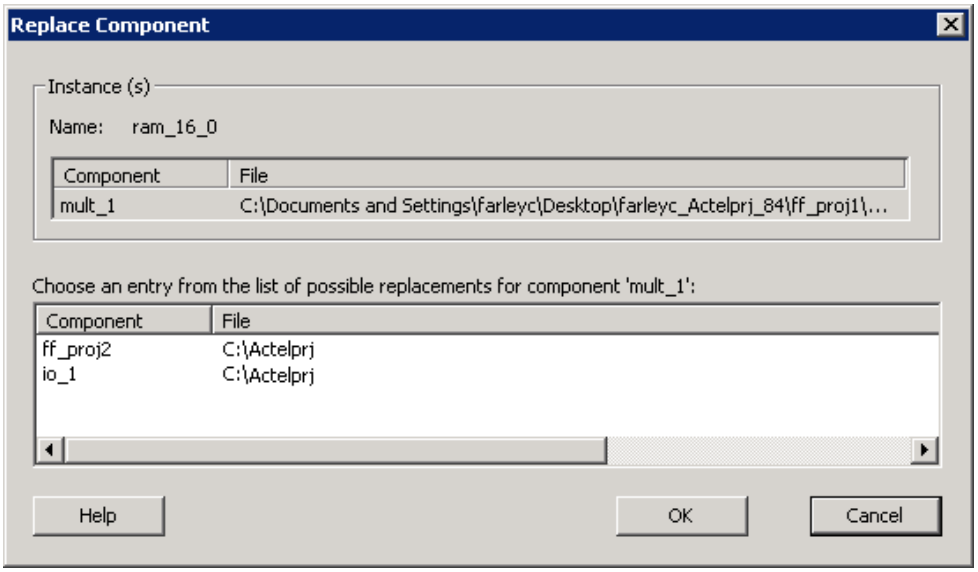


Figure 41 · Replace Component Dialog Box

2. Select the component you want to replace it with and click **OK**.

Design State Management

When any component with instances in a SmartDesign design is changed, all instances of that component detect the change.

If the change only affects the memory content, then your changes do not affect the component's behavior or port interface and your SmartDesign design does not need to be updated.

If the change affects the behavior of the instantiated component, but the change does not affect the component's port interface, then your design must be resynthesized, but the SmartDesign design does not need to be updated.

If the port interface of the instantiated component is changed, then you must reconcile the new definition for all instances of the component and resolve any mismatches. If a port is deleted, SmartDesign will remove that port and clear all the connections to that port when you reconcile all instances. If a new port is added to the component, instances of that component will contain the new port when you reconcile all instances.

The affected instances are identified in your SmartDesign design in the Grid and the Canvas with an exclamation point. Right-click the instance and choose **Update With Latest Component.**

Note: For HDL modules that are instantiated into a SmartDesign design, if the modification causes syntax errors, SmartDesign does not detect the port changes. The changes will be recognized when the syntax errors are resolved.

Changing Memory Content

For certain cores such as Analog System Builder, Flash Memory, or FlexRAM it is possible to change the configuration such that only the memory content used for programming is altered. In this case Project Manager (IDE) will only invalidate your programming file, but your synthesis, compile, and place-and-route results will remain valid.

When you modify the memory content of a core such as Analog System Builder or RAM with Initialization that is used by a Flash Memory core, the Flash Memory core indicates that one of its dependent components has changed and that it needs to be regenerated. This indication will be shown in the Hierarchy or Files Tab  .

In these cases, the Project Manager indicates that your programming file is out of date but your synthesis and place-and-route remain valid. You only need to regenerate your programming file in FlashPoint.

If any SmartGen core is regenerated where the HDL file is not modified, the Project Manager design state will not invalidate your Synthesis and/or Place and Route results. Some specific cores are listed below.

RAM with Initialization core - You can modify the memory content without invalidating synthesis.

Analog System Builder core - You can modify the following without invalidating synthesis:

- Existing flag settings: threshold levels, assertion/de-assertion counts, OVER/UNDER type
- Modifying sequence order or adding sequence operations
- Changing acquisition times
- Resistor Value for the Current Monitor
- RTC time settings
- Gate Driver source current

Flash Memory System Builder core - You can modify the following without invalidating synthesis:

- Modifying memory file or memory content for clients
- JTAG protection for Init Clients

Connectivity Checker

To run the Connectivity Checker, from the **SmartDesign** menu, choose **Connectivity Check**.

SmartDesign displays your connectivity violations in the Connectivity Checker grid (similar to the Grid), but with two additional fields available: Message and Type.

The Message field describes the error/warning, and the Type field displays an icon to indicate if the message is an error or a warning. The default display moves the Type icon into the Message field (as shown in the figure below).

Error messages are shown with a small red octagon and warning messages with a yellow exclamation point.

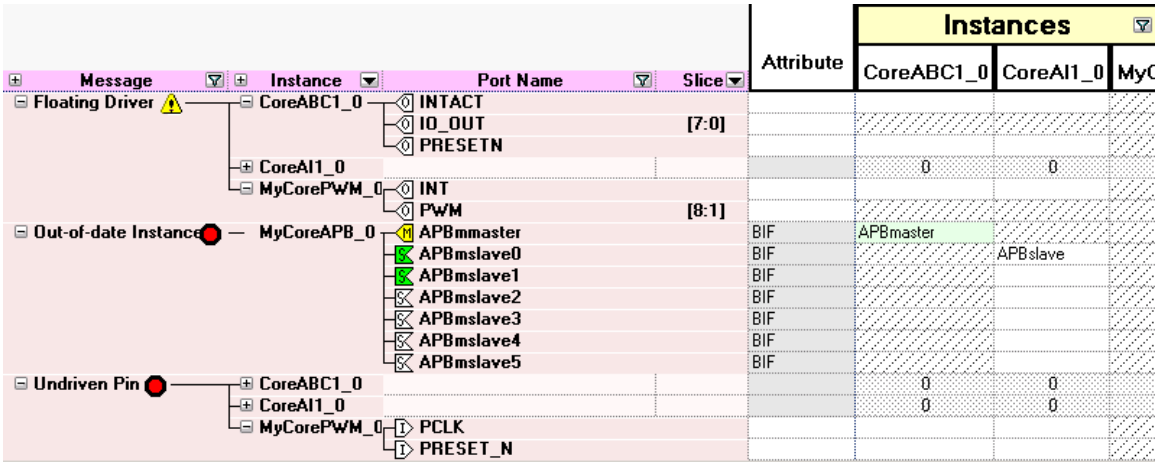


Figure 42 · Connectivity Check Results Grid

Unused Instance - You must remove this instance or connect at least one output pin to the rest of the design.

Out-of-date Instance - You must update the instance to reflect a change in the component referenced by this instance; see Fixing an out-of-date instance.

Undriven Pin - You must connect the pin to a driver, change the state and tie low (GND) or tie high (VCC).

Floating Driver - You can float the pin if it is not going to be used in the current design. Pins marked float are ignored by the Connectivity Check.

Unconnected Bus Interface - You must connect this bus interface to a compatible port because it is required connection.

Required Bus Interface Connection – You must connect this bus interface before you can generate the design. These are typically silicon connection rules.

Required Bus Interface Connection – You must connect this bus interface before you can generate the design. These are typically silicon connection rules.

Multiplicity Rule Violation – Some IP cores can only be instantiated a certain number of times for legal design. For example, there can only be one CortexM1 or CoreMP7 in a design because of silicon rules. You must remove the extra instances.

Incompatible Family Configuration – The instance is not configured to work with this project's Family setting. Either it is not supported by this family or you need to re-instantiate the core.

Incompatible Die Configuration – The instance is not configured to work with this project's Die setting. Either it is not supported or you need to reconfigure the Die configuration.

Incompatible 'Debug' Configuration – You must ensure your CoreMP7 and CoreMP7Bridge have the same 'Debug' configuration. Reconfigure your instances so they are the same.

No RTL License, No Obfuscated License, No Evaluation License – You do not have the proper license to generate this core. Contact Actel to obtain the necessary license.

Generating a SmartDesign Component

Before your SmartDesign component can be used by downstream processes, such as synthesis and simulation, you must generate it.

To generate a SmartDesign component, from the **SmartDesign** menu, choose **Generate** or click  .

This will generate a HDL file in the directory <libero_project>/components/<library>/<yourdesign>.

Note: The generated HDL file will be deleted when your SmartDesign design is modified and saved to ensure synchronization between your SmartDesign component and its generated HDL file.

Generating a SmartDesign component may fail if there are any DRC errors. DRC errors must be corrected before you generate your SmartDesign design.

Synthesizing the SmartDesign Component

Synthesizing a SmartDesign component using the Project Manager is the same as any other design component. See the Synthesis help for more information on using the Project Manager to synthesize your design.

A SmartDesign component must be generated before it can be synthesized.

Note: Once a component is set as root in the Project Manger Hierarchy, it can be synthesized.

Simulating the SmartDesign Component

Simulating a SmartDesign component is identical to simulating any other element in the Libero IDE Project Manager Hierarchy (in the project using Model*SIM* AE). See the ModelSIM AE with Libero IDE help and the Model*SIM* help for more information.

Simulating IPs

Some IPs are packaged with their own testbenches and verification suites. You can run these tests if you want to ensure the IP is working properly.

To simulate an individual DirectCore IP:

1. Generate your design.
2. In the Hierarchy, change the Show drop-down menu to Modules. This switches all the components to their module representation.
3. Select the IP that you wish to simulate, right-click and choose **Set As Root**. You may have to expand the Hierarchy to view the IP module you wish to simulate.
4. Click the Simulation icon in the Project Flow window to run simulation.

Reference

SmartDesign Menu

Command	Icon	Function
Show Canvas View		Displays the Canvas
Show Grid View		Displays the Grid
Show Schematic View		Displays the Schematic Viewer
Show Memory Map / Data Sheet		Displays the datasheet for the design
Check Connectivity		Runs the Connectivity Checker
Generate Design		Generates your SmartDesign component
Auto Connect		Auto-connects instances
Add Port		Adds a port to the top of the SmartDesign component

Canvas Menu

Command	Icon	Function
Auto-Arrange Instances		Auto-arranges the Canvas location of the instances on your Canvas; note that the Canvas location of the instances is a representation and not the actual layout.
Auto-Arrange Connections		Auto-arranges the Canvas location of the connections on your Canvas; note that the Canvas location of the instances is a representation and not the actual layout
Nets		Shows/hides the nets on the Canvas
Ruler		Shows/hides the ruler at the edges of your Canvas
Grid Points		Shows/hides grid points on your Canvas
Page Bounds		Shows/hides the page boundaries on your Canvas

Grid Menu

Command	Function
Hide All Connected Ports	Hides all connected ports in the current grid
Fit All Columns to Data	Fits the column size to the data in the column
Reset Instance [or Net] View to Default	Resets the grid layout for the current grid
Show All Rows	Shows all rows in the Display Panel
Show All Instance Columns	Shows all instance columns in the Connection Panel
Show All Rows and Columns	Shows all rows and columns in the Display Panel
Attribute Column	Shows/hides the Attribute column in the Connection Panel
Top Level Column	Shows/hides the Top Level column in the Connection Panel
Fields	Shows/hides the selected field in the Display Panel

Schematic Menu

Command	Icon	Function
Go To First Page		Goes to first page in Schematic View (when using page splitting)
Go To Previous Page		Goes to previous page in Schematic View (when using page splitting)
Go To Next Page		Goes to next page in Schematic View (when using page splitting)
Go To Last Page		Goes to last page in Schematic View (when using page splitting)
Allow Page Splitting		Allows page splitting; useful when you have a large schematic
Fit to Page		Fits the content to a single page

SmartDesign Glossary

Term	Description
BIF	Abbreviation for bus interface.
bus	An array of scalar ports or pins, where all scalars have a common base name and have unique indexes in the bus.
Bus Definition	Defines the signals that comprise a bus interface. Includes which signals are present on a master, slave, or system interface, signal direction, width, default value, etc. A bus definition is not specific to a logic or design component but is a type or protocol.
Bus Interface	Logical grouping of ports or pins that represent a single functional purpose. May contain both input and output, scalars or busses. A bus interface is a specific mapping of a bus definition onto a component instance.
Bus Interface Net	A connection between 2 or more compatible bus interfaces.
Canvas	Block diagram, connections represent data flow; enables you to connect instances of components in your design.

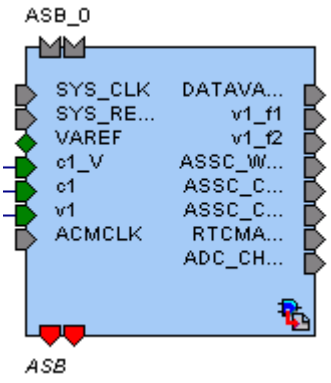
Term	Description
Component	Design element with a specific functionality that is used as a building block to create a SmartDesign core. A component can be an HDL module, SmartGen core, SmartDesign core, Designer Block, CoreConsole core, or IP core. When you add a component to your design, SmartDesign creates a specific instance of that component.
Component Declaration	VHDL construct that refers to a specific component.
Component Port	An individual port on a component definition.
Grid	Manual connection tool in SmartDesign.
Driver	A driver is the origin of a signal on a net. The input and slave BIF ports of the top-level or the output and Master BIF ports from instances are drivers.
Instance	A specific reference to a component/module that you have added to your design. You may have multiple instances of a single component in your design. For each specific instance, you usually will have custom connections that differ from other instances of the same component.
Master Bus Interface	The bus interface that initiates a transaction (such as a read or write) on a bus.
Net	Connection between individual pins. Each net contains a single output pin and one or more input pins, or one or more bi-directional pins. Pins on the net must have the same width.
PAD	The property of a port that must be connected to a design's top level port. PAD ports will eventually be assigned to a package pin. In SmartDesign, these ports are automatically promoted to the top-level and cannot be modified.
Pin	An individual port on a specific instance of a component.
Port	An individual connection point on a component or instance that allows for an electrical signal to be received or sent. A port has a direction (input, output,

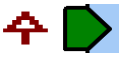
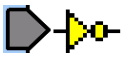
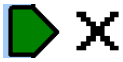
Term	Description
	bi-directional) and may be referred to as a 'scalar port' to indicate that only a single unit-level signal is involved. In contrast, a bus interface on an instance may be considered as a non-scalar, composite port. A component port is defined on a component and an instance port (also known as a 'pin') is part of a component instance.
Signal	A net or the electrical message carried on a net.
Slave Bus Interface	Bus interface that terminates a transaction initiated by a master interface.
System Bus Interface	Interface that is neither master nor slave; enables specialized connections to a bus.
Top Level Port	An external interface connection to a component/module. Scalar if a 1-bit port, bus if a multiple-bit port.

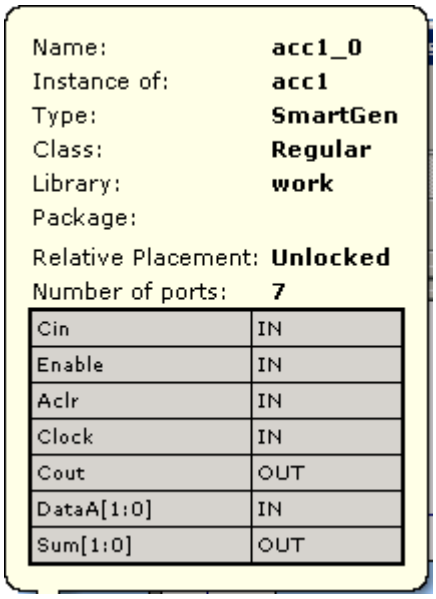
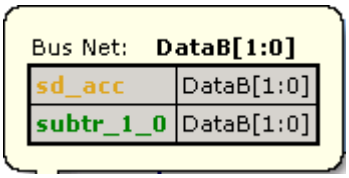
Canvas Icons

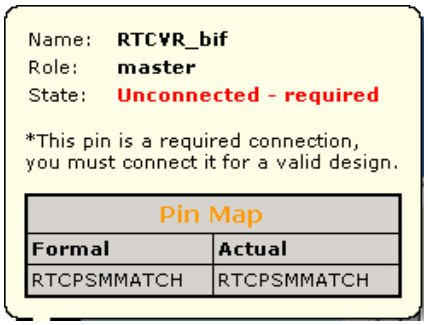
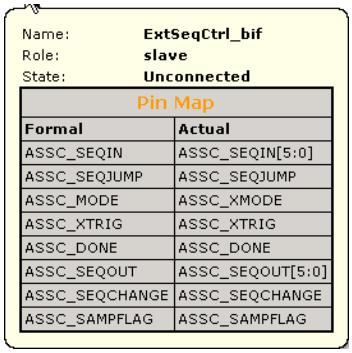
Canvas icons are listed below.

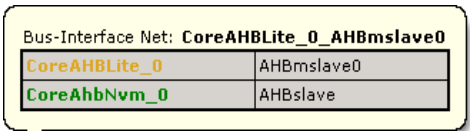
Hover your pointer over any icon in the SmartDesign Canvas view to display details.

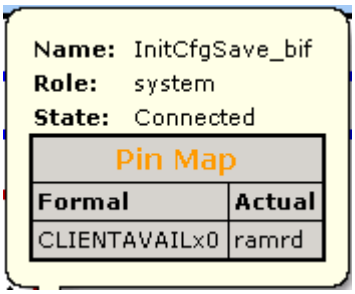
Icon	Description
	Representation of an instance in your design. An instance is a component that has been added to your SmartDesign component. The name of the instance appears at the top and the name of the generic component at the bottom. The instance type is indicated by an icon inside the instance. There are specific icons for instances

Icon	Description
	from SmartDesign, SmartGen, CoreConsole, HDL, and ViewDraw. The instance icon at left indicates a SmartGen core.
	Bus instance; you can click and drag the end of a bus instance to resize it; also, the bus instance will resize based on the number of instances that you connect to it.
	Optional unconnected pin. Required pins are red.
	Connected pin
	Pin with default Tie Off
	Pin tied low
	Pin tied high
	Pin inverted
	Pin marked as unused
	Pin tied to constant

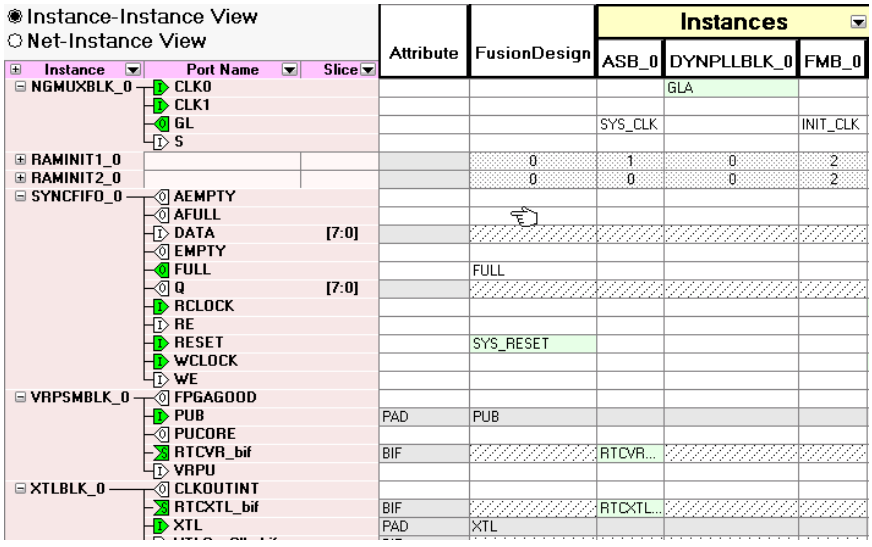
Icon	Description
	Instance details. If there are less than twenty ports, they are listed in the details.
	Bus Net details.
	Master bus interface icon. A master is a bus interface that initiates a transaction on a bus interface net. An unconnected master BIF with REQUIRED connection is red (shown at left). A master BIF with unconnected OPTIONAL connection is gray.

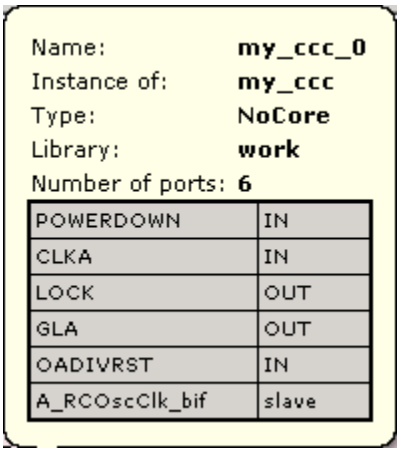
Icon	Description
	Master BIF details, showing name, role, and state. The Pin Map shows the Formal name of the pin assigned by the component (in this example, RCCLKOUT) and the Actual, or representative name assigned by the user (CLKOUT).
	Slave BIF (shown at left). Unconnected slave icons with REQUIRED connections are red. Unconnected slave icons with OPTIONAL connections are gray.
	Slave BIF details, showing name, role, and state. The Pin Map shows the Formal name of the pin assigned by the component (in this example, RCCLKOUT) and the Actual, or representative name assigned by the user (CLKA).
	Master-slave bus interface connection

Icon	Description
	Master-slave bus interface connection details.
	Groups of pins in an instance. Fully connected groups are solid green. Partially connected groups are gray with a green outline. Unconnected groups (no connections) are gray with a black outline.
	A system BIF is the bus interface that does not have a simple input/output relationship on both master/slave. This could include signals that only drive the master interface, or only drive the slave interface, or drive both the master and slave interfaces.

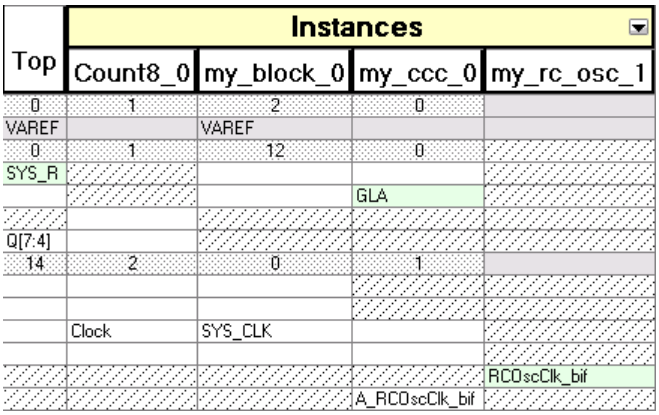
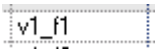
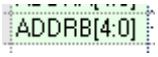
Icon	Description
	System BIF details, showing name, role, and state. The Pin Map shows the Formal name of the pin assigned by the component (in this example, CLIENTAVAILx0), and the Actual name assigned by the user (in this example: ramrd).

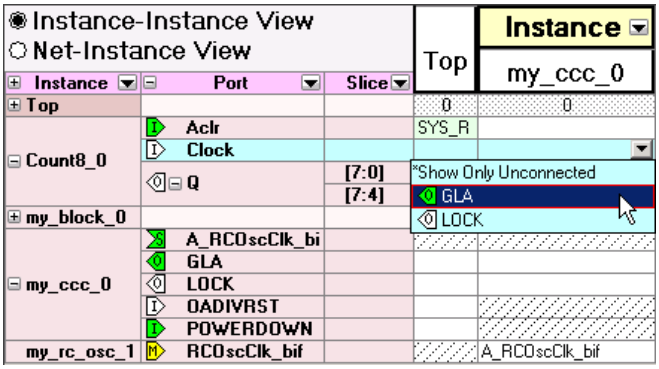
Grid - Display Panel Icons

Icon	Description
	Display panel (default Instance-Instance view). Note the +/- next to the instances to expand and contract the lists. You can click and drag an edge to resize the columns in the Display panel. Click and drag the column headings (Instance, Port Name, Slice, etc.) to change the order of the columns. Right-click the column headings to modify the fields (show/hide Instance, Port, etc.)
	Filter button
	Output icon (Port field). Shows that the port is a connected (green)

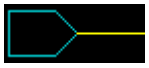
Icon	Description
	output (letter O).
	Input icon (Port field). Shows that the port is a connected (green) input (letter I).
	INOUT icon (Port field). Shows that the port is a connected INOUT port. Unconnected INOUT ports are white.
	Disconnected (white) output icon
	Disconnected input icon
	Master icon, connected
	Master icon, unconnected
	Slave icon, connected
	Slave icon, unconnected
	Display panel instance details. **Name** is the name of your component; the default name for components is <instance>_0. **Instance of** specifies the component that was used to create the instance. **Type** shows the origin of the component, such as SmartGen if the component was created in SmartGen, or IP if the core was created by CoreConsole. **Library** is the library location of the core.

Grid - Connection Panel Icons

Icon	Description
	Connection panel (Instance-Instance view). This default view of this panel shows your top level, all instances, and their corresponding connections to instances in the Display panel. Use the filter button  to show/hide your instances. Intersections between identical instances are grayed out. Also, inputs may only be connected to outputs, outputs only connected to inputs. INOUT ports may be connected to inputs or outputs.
	White, empty cells indicate that a connection is possible, but not active.
	White cells with text indicate that the cell is connected and a non-driver.
	Light green cells indicate that the cell is connected and is a driver.
	Gray cells are read-only and indicate that the connection is exclusively reserved for pads.
	Blue dotted cells indicate that there are multiple connections at that intersection - the number in the cell shows how many connections there are; click the cell to view the connections.
	Black dotted cells indicate that multiple connections are possible - the number in the cell indicates how many connections are available; expand the instance in the Display panel to show more connections.

Icon	Description
	Diagonal hatch cells indicate no legal connections are possible
	List of ports available to connect. The intersection of an instance in the Display panel and an instance in the Connection panel enables a drop-down menu. Select the pin you want to use to connect the two instances from the drop-down menu. Icons in the drop-down menu represent whether the connection is a connected input, output, master, or slave. See the Display panel icon list for more information.

Schematic Symbols

Icon	Description
	Schematic input icon
	Schematic output icon
	Schematic inout icon
	Schematic input icon (multiple addresses)
	Schematic connection icon
	Schematic connection icon (multiple connections)
	Schematic inverter icon; hover your mouse over the inverter symbol in the schematic view for more information on the state of your inverter. An inverter symbol does not necessarily indicate that all your pins are inverted.

Using the HDL Editor

The HDL Editor is a text editor designed for editing HDL source files. In addition to regular editing features, the editor provides a syntax checker.

You can have multiple files open at one time in the HDL Editor workspace. Click the tabs to move between files.

CoreConsole only: If you use the template created by CoreConsole to instantiate the top level of the CoreConsole project, you must create a new HDL source file and copy the content of the template. If you do not, Libero IDE overwrites the file if you re-import a CoreConsole project.

Editing

Editing functions are available in the **Edit** menu. Available functions include cut, copy, paste, find, and replace. These features are also available in the toolbar.

Saving

You must save your file to add it to your Libero IDE project. Select **Save** in the **File** menu, or click the **Save** icon in the toolbar.

Printing

Print and **Print Preview** functions are available from the **File** menu and the toolbar.

Note: To avoid conflicts between changes made in your HDL files, Actel recommends that you use one editor for all of your HDL edits.

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (http://www.actel.com/custsup/search.html) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at http://www.actel.com/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

For more information about Actel's products, visit our website at

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