
Silicon Explorer II

User's Guide

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked.

View the online help included with software to enable all linked content.



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Getting Started

About Silicon Explorer (SE)

The Silicon Explorer™ Logic Analysis software is designed to support logic instruments such as a timing analyzer, a state analyzer, and a probe pilot. Each of these instruments provides specific capabilities for acquiring and/or viewing data.

Microsemi has previously offered Silicon Explorer (SE) II Lite, SE Lite and SE I (all now discontinued).

SE full-version has a built in logic analyzer functionality. SE has a 22-pin (18 channels, a clock, VCC, GND, and clock GND) and a 16-pin connector for controlling the Action Probe circuitry and reading the design checksum. It also has a 26-pin connector for programming ProASIC devices. The Silicon Explorer II logic-analysis system is enhanced to support an external power supply, which permits internal probing of 5.0V, 3.3V, and 2.5V FPGAs. Other features include four-levels of triggering, decompression on download to speed up response time and system acquisition rates up to 100MHz.

Silicon Explorer II enables control of the Action Probe circuitry, a patented architectural feature built into all of Actel's antifuse devices that allows access to any internal node from selected external pins. SE II integrates two diagnostic tools, the Command module and the Analyze module, into a single diagnostic and logic analysis device that attaches to a PC's standard COM port. The [Command module](#) of the Explore software lists all the observable nets in the FPGA. Select the desired net in the list and click the PRA or PRB button to display the signal on the Analyze module. The Command module also reads back the design's checksum. Also, it is possible to read back the CHECKSUM of a device after it has been secured. You can use the design's checksum to verify that you programmed the correct design in the FPGA. The Analyze module is an 18-channel logic analyzer that automatically displays the signals for both probe outputs (and up to 16 additional signals) on the target system. You may sample data asynchronously at 66 MHz. Channel 1 and 2 of the logic analyzer connect to the PRA and PRB signals on the FPGA automatically. Silicon Explorer II uses the remaining 16 channels of the logic analyzer to examine other signals on the board.

Silicon Explorer has no memory devices. File data cannot be stored on any of the non-volatile memory components.

Device Support

Silicon Explorer supports all antifuse devices.

System Requirements

For information about supported platforms, see the [Microsemi website](#).

Kit Contents

The Silicon Explorer kit contains the following:

Table 1 · Silicon Explorer Kit Contents

Hardware/Software	Part Number
Silicon Explorer II	SILICON-EXPLORER II
Silicon Explorer User's Guide	5029134

Hardware/Software	Part Number
Ribbon Cable Assembly	RIBBON & BREAKOUT CABLES
Quick Pro Clips	1630073
Accessory Bag	1630078
Power Supply	SE II PWR SUPPLY
Flying Lead Cable Assembly	SI-EX-TCA
CD Containing Silicon Explorer Software	LIB-CD-PACK-PC

Connecting to the PC

Silicon Explorer II connects to a standard serial port using an 8250 or 16550 UART. Establish communication via the 9-Pin D-Sub connector.

Connecting Silicon Explorer

Powering Silicon Explorer II

SE II supports probing of anti-fuse FPGAs with 5.0V, 3.3V, or 2.5V I/O supplies. SE II draws power from the external power adapter (included with SE II unit). Optionally, SE II may be powered without the external supply by connecting the VIO pin to an existing power source within the PCB, but only for I/O supply of 3.3V or 5.0V. If I/O supply is 2.5V, the external power adapter must be used.

Note: You must use the external power adapter in all situations if the target system cannot supply enough current to run SE II.

When you apply power, the yellow “heartbeat” LED on Silicon Explorer II begins to blink. Microsemi designed Silicon Explorer II hardware to withstand abuse normally found in a lab environment. However, long term exposure to out-of-range conditions can cause failure. Long-term connection to reverse or over-voltage power conditions can cause thermal failure.

Current Consumption

Silicon Explorer II is a CMOS device and exhibits very low current consumption when idle. Current consumption rises rapidly to several hundred milliamps during acquisition. If your power supply is unable to supply the necessary current, SE II or your target may reset. The table below is a guide to typical current consumption based on an acquisition rate at 5V — current will be proportionately higher at 3V.

Table 2 · Typical Current Consumption

Acquisition Rate	Current @5V
IDLE	75 mA
10 MHZ	300 mA
20 MHz	400 mA
50 MHz	500 mA
100 MHz	700 mA

Connector Types

Silicon Explorer II has a 22-pin (18 channels, a clock, VIO, GND, and clock GND), a 26-pin, and a 16-pin connector for controlling the Action Probe circuitry and reading the design checksum.

Table 3 · Connector Types

Connector Type	Mode
22-pin	Logic Analysis
16-pin	Action Probe Control
26-pin	Not Used

The pins are assigned according to the table below.

Source	Pin
PRC	Pin 6
PRD	Pin 7
GND	Pin 1, 21
VIO	Pin 2

Logic Analysis

Microsemi Silicon Explorer II ships with a replaceable target cable assembly (SI-EX-TCA) that interfaces Silicon Explorer II with your target system. To connect Silicon Explorer II, align the short red wire on the SI-EX-TCA with no dot on the case and fully insert the 2 mm header (Digi-Key MHD16K-ND). The contacts on the SI-EX-TCA accept standard 0.025" round or square test accessories.

Connect any of Silicon Explorer II's 18-channel leads to the desired target signals using standard test accessories.

The Silicon Explorer units come with cables that are terminated with a connector so you can insert a post on the board. A bag of clips that attach to these connectors to clip onto a post or pin of the device, or another cable is also included.

Probe Leads

Connect the probe leads by attaching one of two supplied cable assemblies. One 16-pin cable assembly terminates in individual 0.025 connectors that connect to 0.025 headers or microclips according to the labels on the wires. The other assembly interfaces directly to the target board with a 16-pin header when you install the target according to the pin-out shown in the figure and listed in the table below.

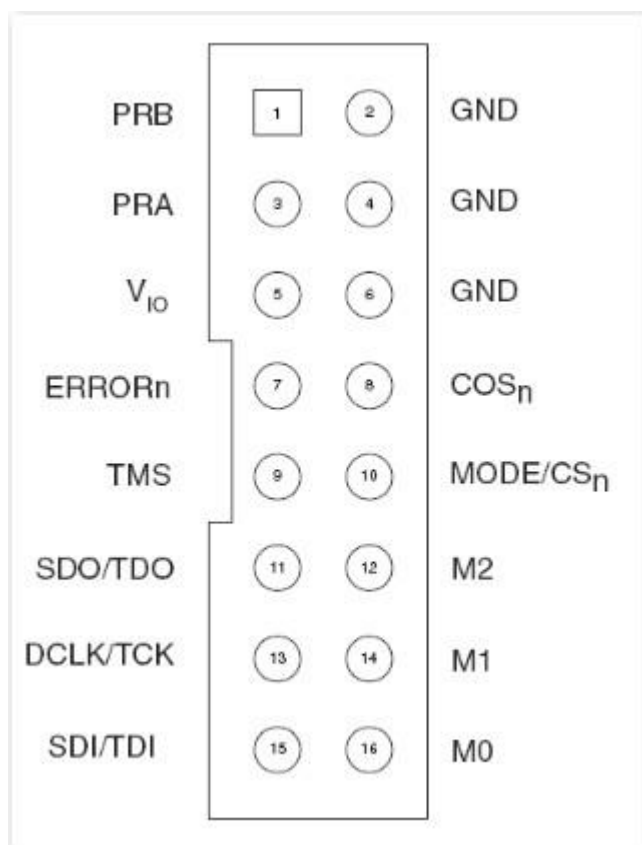


Figure 1 · Silicon Explorer II Probe Connector Pin-Out

Table 4 · Matching Probe Pins to Device Pins ¹

Probe	ACT1,40MX	ACT2, 42MX, 3200DX	SX/SX-A/eX
Mode	Mode	Mode	Not Used
GND ²	GND	GND	GND
SDI/TDI	SDI	SDI	TDO
DCLK/TCK	DCLK	DCLK	TCK
SDO/TDO	PRA	SDO	TDO
TMS	Not Used	Not Used	TMS
V _{IO}	V _{CCI}	V _{CCI}	V _{CCI}
PRA	PRA	PRA	PRA
PRB	PRB	PRB	PRB
Ch3 ³	-	-	PRC
Ch4 ³	-	-	PRD

¹ ERRORn, CONn, M2, M1, M0 pins are not required for use with Silicon Explorer II.

²You can connect any or all GND pins. For best results, connect all GND pins.

³These are used with [AX/RTAXS](#) devices.

Note: Note: Chan 16/QO, Chan 17/Q2, and Chan 0/CH0/TRIG refers to a feature in a previous product and is not available in Silicon Explorer.

Silicon Explorer Target Connections

Signal Connections

Silicon Explorer includes a replaceable [TCA](#) cable which interfaces to your target system. The TCA contains flying leads for input signals, clock, power and ground. Each wire is identified by a printed label.

To connect Silicon Explorer to the target signals:

1. Insert the TCA 2 mm header into Silicon Explorer. The connector is keyed and will only go in one way.
2. Connect the leads to the circuit under test using the .025" contacts, or test accessories such as probe clips, or clip-over adapters.

To avoid difficulty:

- Be sure the TCA is firmly seated in the mating connector.
- Remember that the ground lead is also the signal return. Make a good connection directly to the ground plane or a ground point near the highest frequency signal that you will be acquiring. If possible connect all of the ground leads to the target board for best signal quality.

External Clock

Synchronous acquisitions are made by connecting the Clock input leads of the target cable assembly (TCA) to the clock signal on the circuit under test. Silicon Explorer is specified to sample using an external clock to 66 MHz.

To connect to an external clock:

1. Insert the TCA 2 mm header into Silicon Explorer. The connector is keyed and will only go in one way.
2. Connect the external clock input lead of the target cable assembly, labeled CKLIN, to the clock signal on the target board.
3. Connect the clock ground wire to the ground plane or a ground point physically close to the clock signal.

To avoid difficulty:

- The clock ground wire should be connected for best signal integrity.
- Be sure the TCA is firmly seated in the Silicon Explorer mating connector.

See Also

[Sampling](#)

[Understanding Synchronous Sampling](#)

Power

Silicon Explorer is powered by +3V to +5V, which is supplied by the target board, the supplied power adapter (Silicon Explorer II only), or an external power supply. To determine if a power adapter or external supply is needed, see the current consumption section.

Caution: Although Silicon Explorer is designed to withstand the abuse normally found in a lab environment, long term exposure to out of range conditions can cause failure. In particular long term connection to reverse or over-voltage power conditions can cause thermal failure.

Target Power

Power and ground leads are provided on the target cable assembly (TCA) for connection to a +3V to +5V source. Two micro-grabber test clips are used for connection to power test points on the target board.

1. Insert the target cable assembly (TCA) 2 mm header into Silicon Explorer. The connector is keyed and will only go in one way.
2. With power removed from the target circuit, connect the TCA power and ground leads to the power (+3V to +5V) and ground test points on the target board. The TCA power lead is labeled +5V but can be connected to any voltage between +3V and +5V on the target.
3. Apply power to the target circuit.

Note: Note: The amount of current drawn by Silicon Explorer depends on the sample rate selected and number of active input channels and ranges from 125mA to 750mA with a 5V supply.

Power Adapter

The supplied power adapter (Silicon Explorer II) is a compact switching power supply that provides +5V at 1 A for applications where target power is not available or insufficient. The power supply is plugged into the power jack located on the Silicon Explorer II next to the serial cable.

1. With the power adaptor disconnected from any wall outlet, insert the power adaptor's plug into the power jack on the Silicon Explorer II.
2. Connect the Silicon Explorer II ground leads to the target.
3. Plug the power adaptor into a wall outlet.

External Power Supply

An external +5V power supply may be used to power Silicon Explorer when target power is insufficient. Power and ground leads are provided on the target cable assembly (TCA) for connection to the +5V source. Two micro-grabber test clips can be used for connection to ground test points on the target board.

1. Insert the target cable assembly (TCA) 2mm header into Silicon Explorer. The connector is keyed and will only go in one way.
2. With the external power supply turned off, connect the Silicon Explorer and external power supply ground leads to the ground plane of the circuit under test.
3. Connect the Silicon Explorer and external power supply +5V leads together.
4. Switch on the external supply.

Current Consumption

Silicon Explorer is a CMOS device and exhibits very low current consumption at idle, rising rapidly to several hundred milliamps during acquisition. The amount of current required depends on the sample rate and number of active channels. If your power supply is unable to supply the inrush current, Silicon Explorer or your target may reset. The following lists the minimum and maximum current requirements at 5V. Current will be proportionately higher at 3V:

Idle	125 mA
Minimum Acquisition	350 mA
Maximum Acquisition	750 mA

Debug Port

You can connect the probe leads by attaching one of two supplied cable assemblies. One cable assembly terminates in individual 0.025 receptacles that can connect to 0.025 headers or micro-clips according to the labels on the wires - the other assembly interfaces directly to the target board when a 16-pin header is installed on the target according to the pin-out shown on the bottom of the Silicon Explorer.

The Probe A and B pins on the probe connector may be selected as the source for logic analyzer channels 1 and 2 respectively, by clicking on the # field in the Waveform window and selecting PRA or PRB as the source. Selecting the probe pins as the source disables the CH1 and/or CH2 inputs from the target cable assembly.

See Also

- [Probing](#)

Silicon Explorer PC Connection

[Device Settings](#)

[Hardware Connection](#)

See Also

[Target Connections](#)

[Troubleshooting](#)

Connecting Silicon Explorer

The Silicon Explorer POD is connected to your PC with a 9 pin Serial Port cable that is permanently attached to the POD. The Silicon Explorer POD is connected to the target by two cables. The first cable is a 16-pin ribbon cable that contains the control signals for addressing the PRA, PRB, PRC*, and PRD* Action Probes (tm) within the Microsemi FPGAs. The second cable is a 22 pin flying-lead cable for connecting the logic analyzer channels to the target and optionally an external clock. (*Action Probes (tm) PRC and PRD are only available for Axcelerator devices and need be connected to the Channel 3 and Channel 4 leads by the user.)

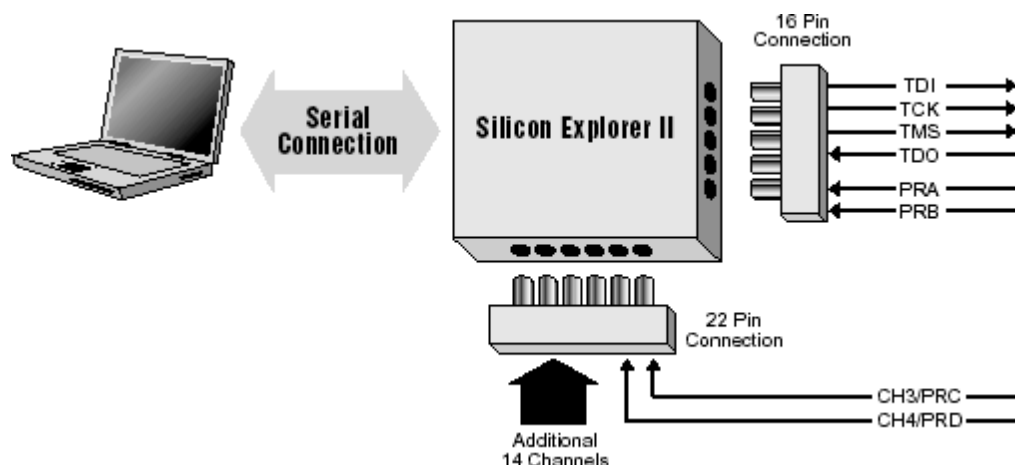


Figure 2 - Connecting Explorer POD to PC

Note: Note: The Silicon Explorer units come with cables that are terminated with a connector into which a post on the board can be inserted. Clips which can be attached to these connectors and used to clip onto a post or pin of the device, or another cable are also included.

Device Settings

The Silicon Explorer connects to a standard RS-232 serial port using either an 8250 or 16550 UART. Although 16550 UARTs are not required for hi-speed operations some serial ports do not use driver/receivers that are rated for the full 115,200 baud data rate used by the Pod and may not work with extension cables.

To attach Silicon Explorer to your PC, connect the Silicon Explorer 9-Pin D-Sub connector to a serial port (COM 1 through 4) on your PC

Note: Note: If you wish to use a serial extension cable with your Silicon Explorer choose a shielded cable of good quality. RTS and CTS are required as well as Transmit, Receive, and Ground. DSR is connected to DTR but is not required for operation.

You can select a serial port (COM1 through 4) from the menu bar. The Silicon Explorer application polls the Silicon Explorer continuously for activity. Setting the port to Demo mode prevents the application from opening any COMports on your system.

To select the COM port:

On the Device menu, click **Port**, then click the appropriate COM port.

Select **Demo** to view data files without Silicon Explorer connected.

The Silicon Explorer software defaults to 115,200 baud at this speed data transfer will be less than 20 seconds for the entire buffer. On some slow systems (486-33 or less) particularly those with 8250 UARTs, better performance may occur at 57,600 baud due to the need to retry blocks at high speed.

To change the baud rate:

On the Device menu, click **Baud**.

Click the appropriate baud rate.

Verify Communication

The Silicon Explorer software reports communication status on the status bar. When the Silicon Explorer has been properly connected, configured and powered, the status will show IDLE. If the status bar reports POLL or N/C (not connected) then the link has not been established. See the [troubleshooting](#) page for assistance.

Act1 and A40MX Connection

The figure below shows the connection of Silicon Explorer II to the Act1 and A40MX families of devices. The Act1 and A40MX families of devices have two probe outputs, PRA & PRB, that connect to the Silicon Explorer's 16 pin connector.

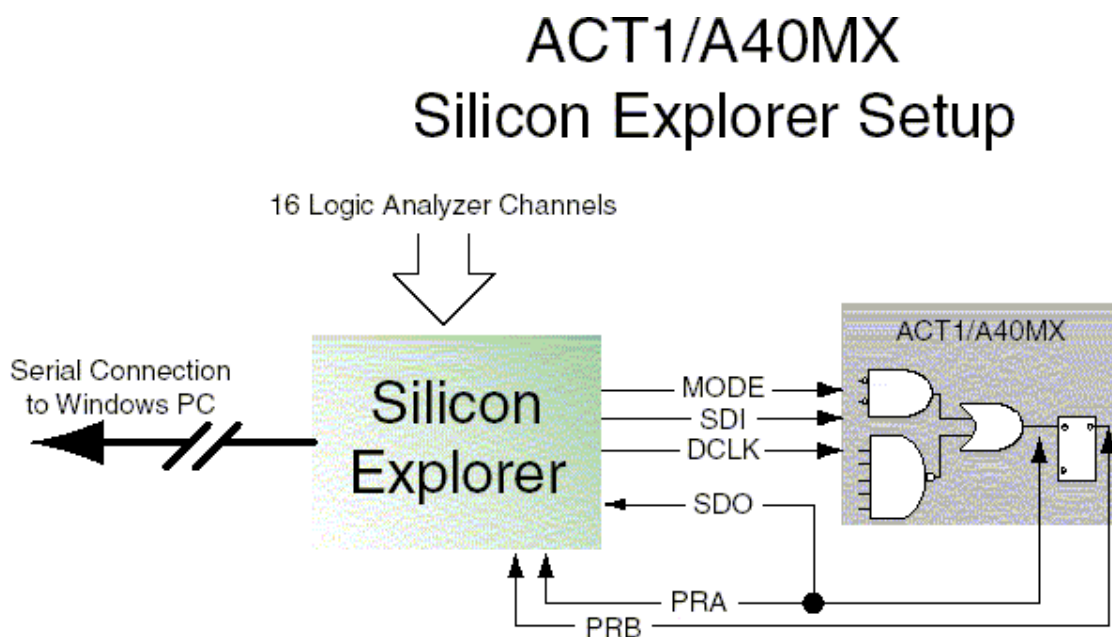


Figure 3 · Silicon Explorer II Connection to Act1 and A40MX Devices

Act2/XL/Act3/DX/A42MX Connections

The figure below shows the connection of Silicon Explorer II to the Act2, Act3, XL, DX, and A42MX families of devices. All of these families of devices have two probe outputs, PRA & PRB, that connect to the Silicon Explorer's 16 pin connector.

ACT2/XL/ACT3/DX/A42MX Silicon Explorer Setup

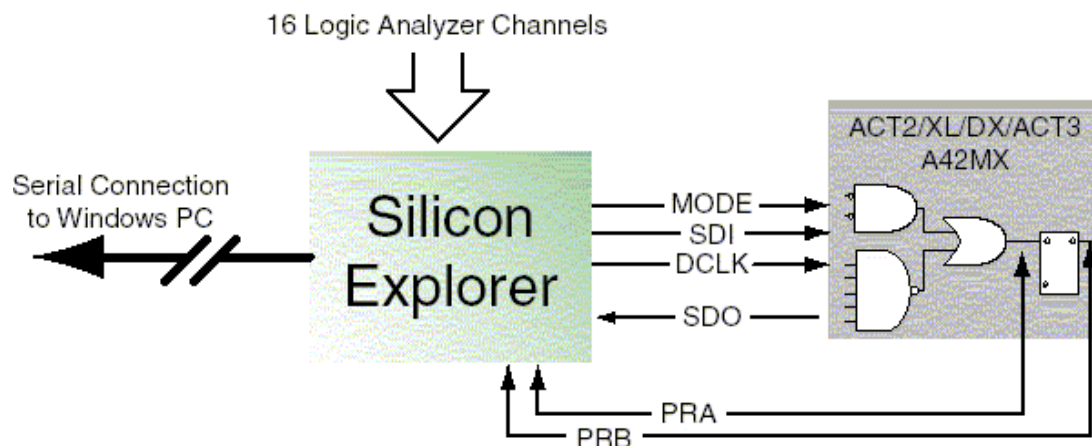


Figure 4 · Silicon Explorer II connection to Act, XL, DX, and A42MX Devices

Note: Note: Designer R398 or later is required for probe file creation.

SX/SX-A/eX/RTSX/RTSX-S Connections

The figure below shows the connection of Silicon Explorer II to the SX, SX-A, RTSX, RTSX-S, and eX families of devices. All of these families of devices have two probe outputs, PRA & PRB, that connect to the Silicon Explorer's 16 pin connector.

The probing of an SX-A, RTSX-S, or eX device may require special setup. Microsemi recommends that you use a series 70 ohm termination on all the probe connectors (TDI, TDO, TCK, TMS, PRA, PRB). The 70 ohm series termination prevents data transmission corruption during probing and reading checksum.

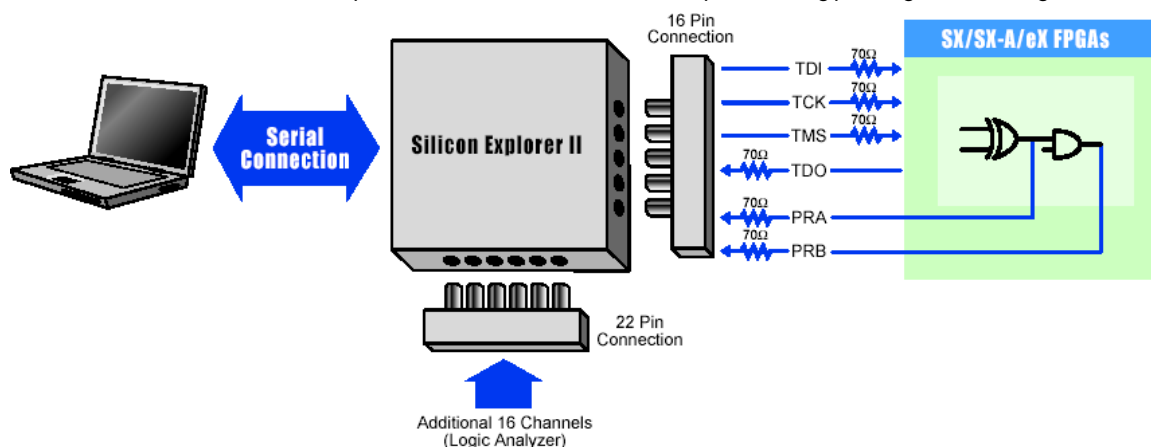


Figure 5 · Silicon Explorer Connection

Note: Note: Designer R398

Axcelerator Connection

The figure below shows the connection of Silicon Explorer II to the Axcelerator family of devices. The Axcelerator family of devices has four probe outputs unlike earlier device families. Each member of the

Axcelerator family has four external pads: PRA, PRB, PRC, and PRD. These can be used to bring out four probe signals from the Axcelerator device (note that the AX125 only has two probe signals that can be observed: PRA and PRB). Each core tile has up to two probe signals.

Shown in this figure are the 70-ohm series termination resistors needed on TDI, TCK, TMS, TDO, PRA and PRB. Probe outputs PRC and PRD do not need termination resistors on the board because resistors are built into the CH3 and CH4 leads. The 70-ohm series termination prevents data transmission corruption during probing and reading checksum.

Note: Note: Signals in Axcelerator devices can only be probed for speeds of 28 MHz or less.

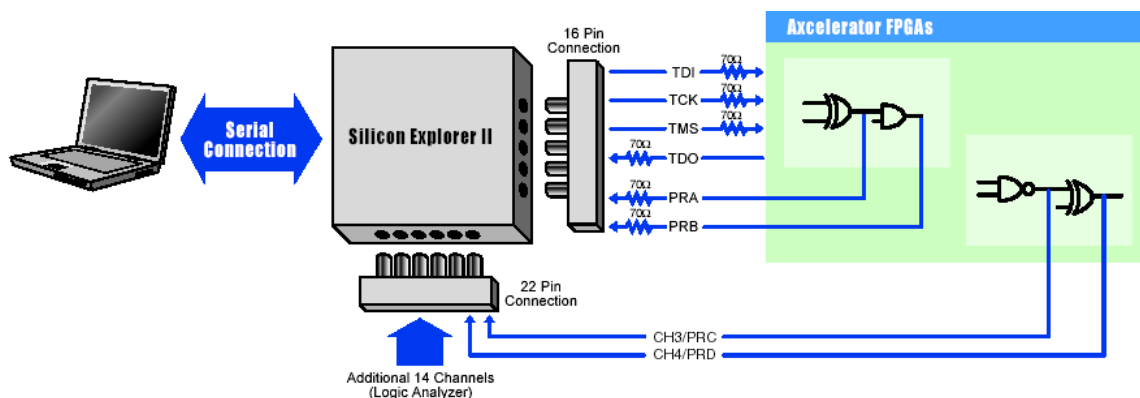


Figure 6 · Silicon Explorer II Connection to Axcelerator Device

Note: Note: Designer R1-2003 SP3 or later is required for Axcelerator probe file creation.

External Logic Analyzer Pinout Table

Table 5 · External Logic Analyzer Pinout Table

Pin Number	Function
1	GND
2	+V5
3	CH0/TRIG
4	CH1
5	CH2
6	CH3
7	CH4
8	CH5
9	CH6
10	CH7
11	CH8
12	CH9
13	CH10

Pin Number	Function
14	CH11
15	CH12
16	CH13
17	CH14
18	CH15
19	CH16/Q0
20	CH17/Q1
21	GND (CLK ground)
22	CLKIN (for synchronous sampling)

Using the Software

Software Settings

Silicon Explorer II sets itself to **Demo** mode on installation. From the Device menu, choose **Silicon Explorer II** or **Silicon Explorer**, depending on your version of the hardware.

Choose the desired port (COM1 through COM4) from the **Port** drop-down list in the **Device** menu. The software continuously polls the hardware for activity. Setting the port to the Demo mode prevents the application from opening any COM ports on your system. The serial port saves information in the analyze.ini file found in your Windows directory. The default data transfer speed is 115,200 baud. At this speed data transfer for the entire buffer is less than 15 seconds.

Note: Note: Many notebook computers share the external COM port with a built-in infrared (IR) port. You may have to enter your CMOS setup menu to enable the external COM port.

Silicon Explorer Software

The Explorer software consists of two components, the Command module and the Analyze module. The Command module of the Explore software lists all the observable nets in the FPGA. Use the Command module to verify that you programmed the correct design in the FPGA. The Analyze module is an 18-channel logic analyzer that automatically displays the signals for both probe outputs (and up to 16 additional signals) on the target system. PRC and PRD are not displayed for other device families. The figure below shows the Silicon Explorer with an Axcelerator probe file loaded.

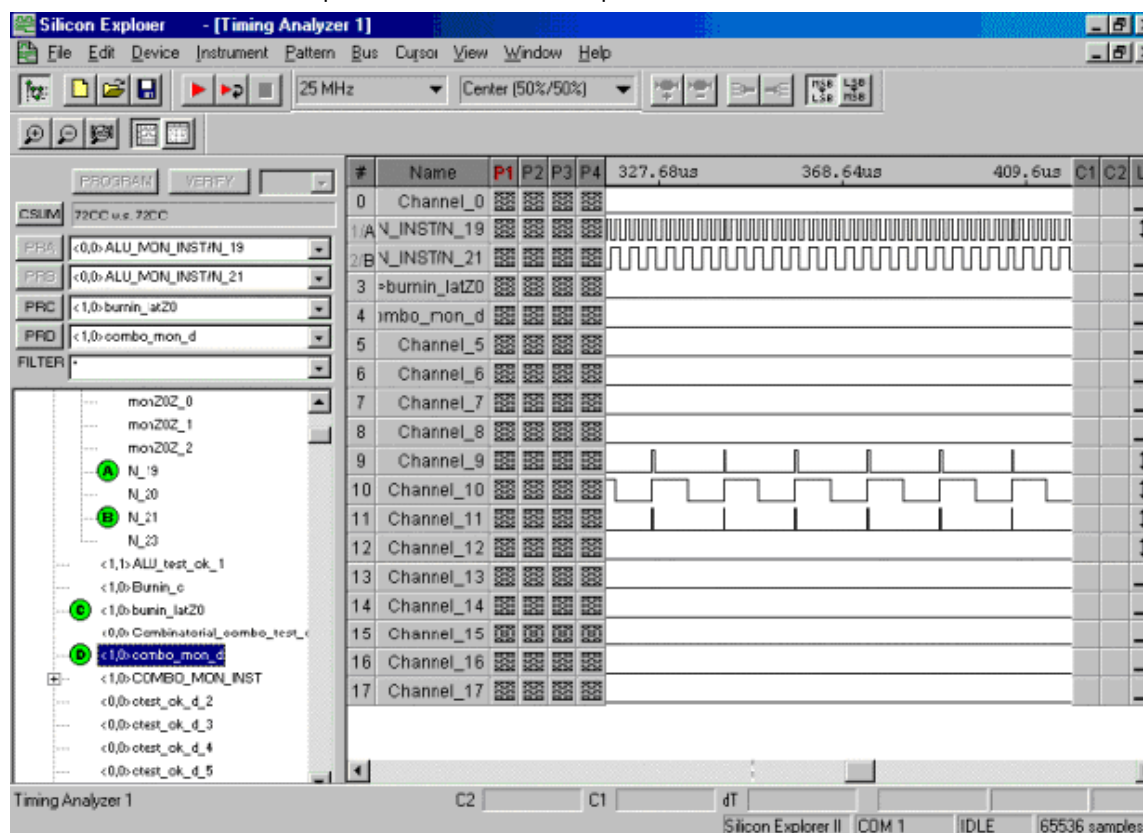


Figure 7 · Silicon Explorer Window with an AX Probe File

Using the Command Mode

The **Command** module is the interface used to select internal nodes in the Microsemi FPGA family. The Command module lists all the observable nets in the FPGA. You can select the desired net in the list and click the PRA or PRB button to display the signal on the Analyze module. The Command module also reads back the design's checksum. You can still read back the CHECKSUM of a device after it has been secured and you can use the design's checksum to verify that you programmed the correct design in the FPGA.

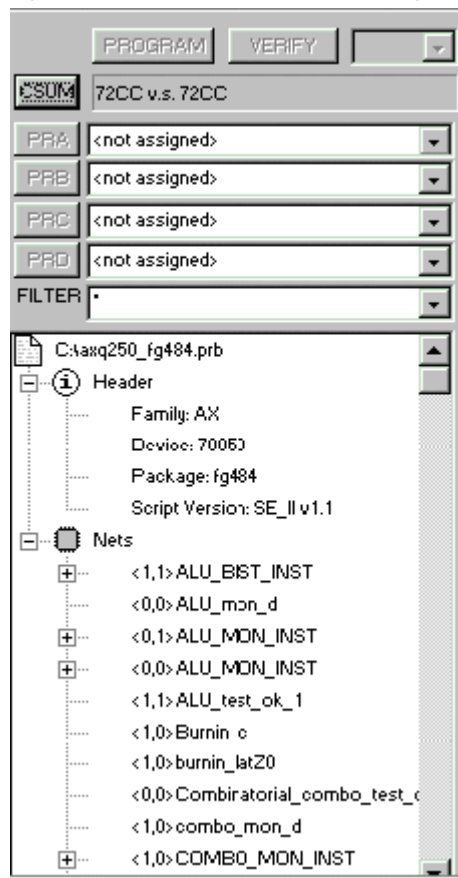


Figure 8 - Command Module

To open a probe file:

1. From the Start menu, choose **Programs > Designer > Silicon Explorer** to launch Silicon Explorer.
2. From the File menu choose **Open**. Choose (*.prb) as the File type and double-click the desired probe file. You can also open a probe file in Silicon Explorer by double-clicking the **Open Actel Probe File** icon.

Explore uses a PRB file exported from Designer during analysis. The exported file contains device information, net names, and node location information. After the PRB file opens, verify the information displayed in the tree structure in the Analyze window.

To export a probe file from Designer:

1. Launch Designer.
2. Open your design file
3. Go to **File > Export** to view the Export dialog box.

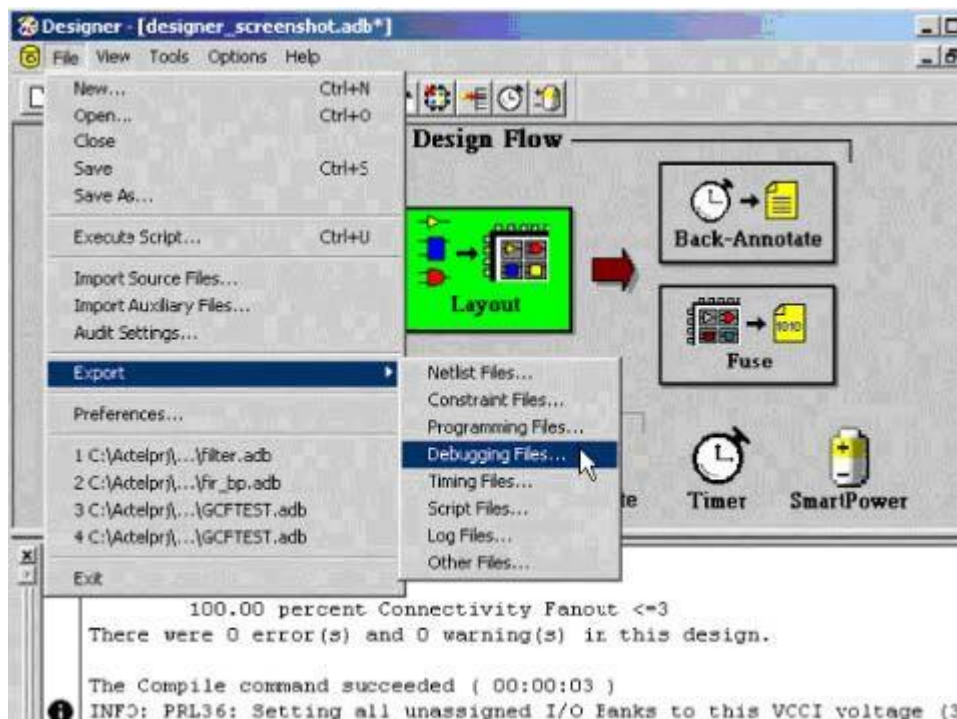


Figure 9 • Opening the Export Debugging Dialog Box

4. Select **Auxiliary File** from the **File Type** pull-down menu.
5. Select **Probe** from the **Type** pull-down menu.
6. Select **OK** to continue and then save the Probe file.

You can also generate a AFM or probe file using the Generate Programming Files: Fuse Files dialog box. See the figure below. Note that the **Generate Probe File Also** box is checked.

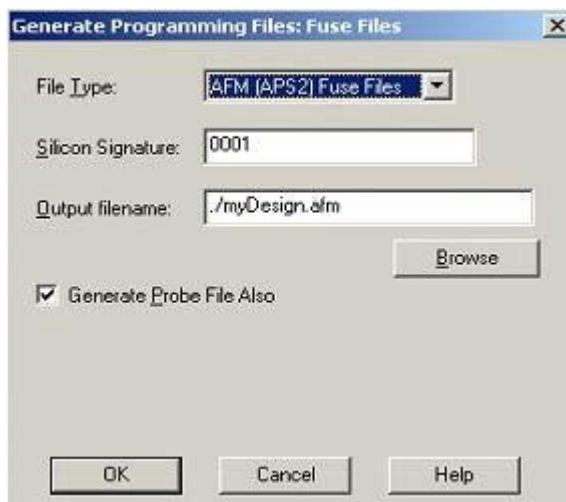


Figure 10 • Generate Programming Files Dialog Box

To verify checksum:

1. Make sure that the SDO/TDO is connected.
2. Click the **Checksum** button.
3. Once you open a Probe file and make a device connection, read the checksum of the target device and compare it to the checksum in the Probe file by double-clicking the Checksum button. The table below lists and explains the error messages.

Note: Note: When reading an FPGA checksum with Silicon Explorer, the Acquire/AutoRun button and the Stop button may randomly toggle. If this happens, click the Acquire button and then the Stop button. This returns the software to normal state.

Table 6 · Checksum Error Messages

Error Message	Explanation
Checksum: 383A vs ????	Checksum is not readable because the probe is disconnected or not powered.
Checksum: 383A vs 0000	Checksum does not match the file or The SDO/TDO probe-side pin is not properly connected to the device. Connector Types contains a listing of the proper connections.

To probe a node:

1. Select the designed signal from the tree by clicking the net name. Use the filter box to search nets quickly, and use the multiple wildcard characters ("*") to restrict your search.
2. Click the PRA or PRB button. Silicon Explorer II routes the selected node to the probe pin and switches the corresponding analyzer input to the probe connector.

Using the Analyze Module

To use the Analyze Module:

1. Open Silicon Explorer II and check the status in the lower right corner of the display. If you have properly selected the COM port and powered up Silicon Explorer II, then the status is IDLE. The Analyze module captures 64K samples of each channel and uploads them to the host over the serial port.

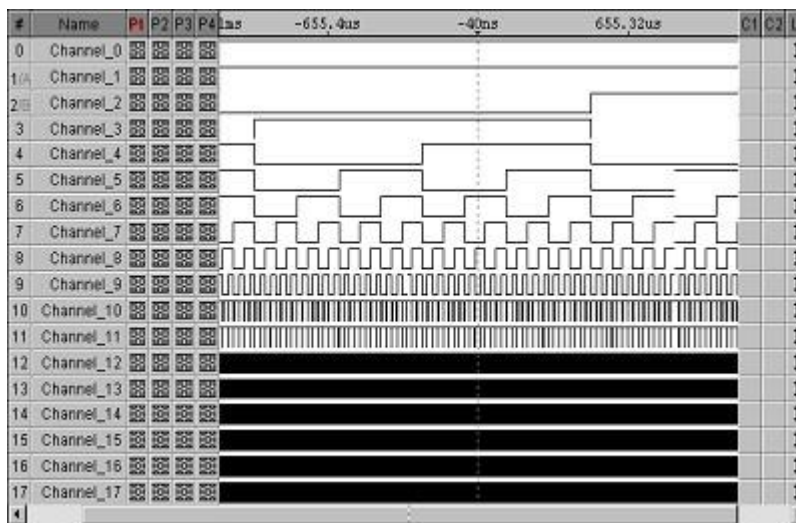


Figure 11 · Analyze Module

2. Set acquisition parameters from the tool bar or the pull-down menus.

Figure 12 · Acquisition Parameters

Acquisition Speed	10 Khz to 100 MHz asynchronous
Trigger Position	25% 50%

	75%
Trigger Pattern	Click on individual signals in the Px Column to specify don't care, low, high, rising, falling, or either edge. The trigger patterns is the logical AND of the 18 patterns.

3. Once you set the acquisition parameters, click the Run button (red triangle) to begin acquisition. The analyzer begins capturing data until Silicon Explorer II recognizes the trigger pattern or you press the stop button (black square). During the capture period, the status window displays "PRE" for the pre-trigger state (although you may not see it if the trigger pattern matches quickly).

Next, Silicon Explorer II enters the POST state and samples data after the trigger pattern (or stop button) until it fulfills the post trigger requirement. Then, it uploads the data to the host (READ State with progress indicator). The entire upload process takes less than 15 seconds, although you may zoom in and view data immediately because the buffer uploads as a background task.

Main GUI

Menu Bar

The Menu Bar provides pull-down menu access to all Silicon Explorer settings, controls and display functions.

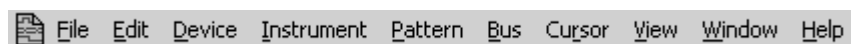


Figure 13 · Menu Bar

[Keyboard shortcuts](#) are also indicated in the menu choice.

Silicon Explorer Tool Bar

The Tools Bars contain button-style controls which are grouped together into individual tool bars. The grouped tool bars can be viewed, hidden or rearranged.

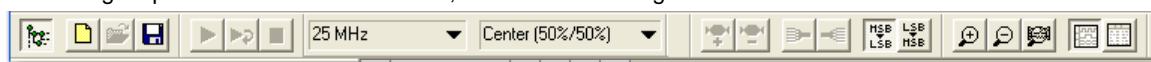



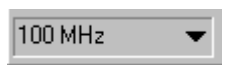
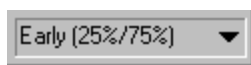





Figure 14 · Tool Bar

Table 7 · Tool Bar Icons and Description

Icon	Group Description
	Show/Hide Probe window.
	Create new project, open created project, and save project.
	These are run control icons used with the analyzer instrument. Use them to acquire, autorun/auto trigger, and halt an acquisition. The auto-trigger mode will continually trigger, capture, and re-arm for the next run capture.
	Use this pull down menu to choose synchronous or asynchronous clocks. See Synchronous and Asynchronous .
	Select the trigger position from the pull-down menu
	Use these icons to create or undefine signal busses.
	Change the resolution of the timing analyzer display by zooming in or out.
	Displays acquisition data as a timing view or a state list. Timing view is displayed horizontally as a graph

Icon	Group Description
	and the state list is displayed vertically as a table.

Main Window

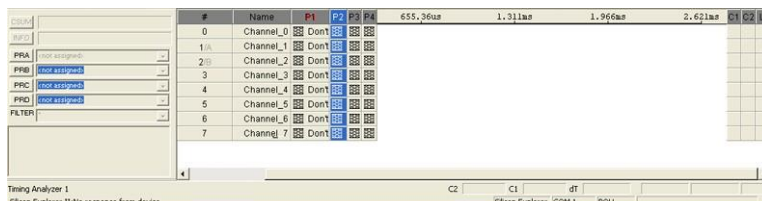


Figure 15 · Silicon Explorer Main Window

The Silicon Explorer software presents information in rows and columns just like a spreadsheet. In the Timing Analyzer each row represents a channel or, in the case of bussed signals, group of channels. Each column contains specific information about that channel, such as the acquired data, trigger condition, signal activity indicator, etc. These columns may be moved and resized as desired.

Pattern Column

The Pattern column contains logic levels and or edge conditions for each channel and can be named. These logic conditions are logically added together composing a pattern which can be used to [trigger the analyzer](#), [locate \(find\) similar patterns within the data](#), or [highlight similar \(or dissimilar\) patterns](#)

See [Pattern](#) for information on creating or renaming a pattern.

Wire Number



The Wire Number column provides a reference between the signal name and the physical target cable assembly wire. In the case of bussed signals, this column contains the list (in order) of all channels included in the bus. This column can be moved or resized as needed.

C1 and C2 (Level at cursor n)

The C1 and C2 columns display the logic levels of all visible channels at the time sample beginning with cursor 1 and cursor 2 respectively. For example, if you place cursor 1 on a logic transition, the C1 column will display the logic level immediately to the right of cursor 1. This column can be moved or resized as needed.



Activity Indicator

The Activity Indicator column provides a real time indication of the state of each channel. The states displayed are Constant HIGH level, Constant LOW level, and TOGGING. In the case of bussed signals, the state of the last channel in the bus is displayed. This column can be moved or resized as needed.

Note: Note: Resizing this column is done by dragging the right edge of the column to the right and can only be done when it is not the last column on the right.

Readout Bar

Cursor measurements are displayed in the Readout Bar located near the bottom of the screen.

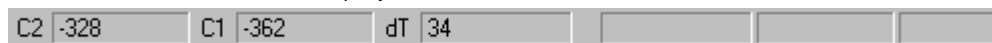


Figure 16 · Readout Bar

C1 - Time (or number of clocks) from the trigger to cursor 1
C2 - Time (or number of clocks) from the trigger to cursor 2
dT - Time (or number of clocks) between cursor 1 and cursor 2

Time measurements appear on the readout bar automatically after cursors are placed in the data.

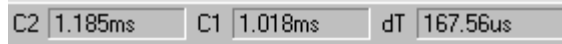


Figure 17 - C2 to trigger / C1 to trigger / C2 to C1

Shortcuts

Keyboard Shortcuts

Table 8 - Keyboard Shortcuts

Menu	Action	Shortcut Key
Run Control	Run	R
	Auto Trigger	A
	Stop	S
Zoom (timing display)	Zoom in	Up arrow
	Zoom out	Down arrow
	Full screen	Spacebar
Pan Controls	Next Screen	Page down
	Previous Screen	Page up
Timing	Forward	Right arrow
	Backward	Left arrow
Goto	Trigger	Home
	Cursor 1	1
	Cursor 2	2
	Find cursor	F
	Beginning or end	End
Find	Next	Ctrl+F
	Previous	Ctrl+Shift+F
Cursors	Nudge cursor 1 forward	Ctrl+right arrow
	Nudge cursor 1 backward	Ctrl+ left arrow
	Nudge Cursor 2 forward	Ctrl+Shift+right arrow

Menu	Action	Shortcut Key
	Set cursor 1	Ctrl+1
	Set cursor 2	Ctrl+2
Edit Controls	Undo	Ctrl+Z
	Cut	Ctrl+X
	Copy	Ctrl+C
	Paste	Ctrl+V
	Delete	Del
	Select all	Ctrl+A
	Deselect all	Esc
	Rename	Enter
Wiggle Sticks: Place cursor in data area	Course Control	Alt (move mouse)
	Fine Control	Shift+Alt (move mouse)

Context Menu Shortcut

Context-sensitive menus are provided via the right mouse button. They are available for the rows and columns of the logic analyzer window.

Data Display

The Silicon Explorer software contains an array of tools to format and view acquired data. These topics explain what the tools are, and how to use them.

- [Bussed Signals](#)
- [Multiple Document Interface](#)
- [Timeline](#)
- [Rearrange Channels](#)

Bussed Signals

Channels may be grouped together as a bus, with their combined numeric value displayed in hex, decimal, ASCII or analog radix.

Creating a Bus

Channels can be grouped together as a bus, with their combined numeric value displayed in hex, decimal, ASCII or analog radix.

Signal busses can be created by grouping similar channels together (such as data lines, address lines, etc.). Once created they can be undefined and viewed as individual channels again.

To create a bus:

1. Click in the channel's wire number column to highlight the bus.
2. Click and drag the cursor to highlight the remaining channels.
3. Click the **MAKE BUS** icon on the tool bar.



Undefined a Bus

To undefine a bus:

1. Click the buses wire number column to highlight it
2. Click the **Undefine Bus** icon.



Collapsing a Bus

Expanding a bus shows the individual channels without losing the bus structure that happens when the bus is Undefined. Collapsing the bus has the opposite affect, displaying the signals as a single bus once more.

To Expand a bus:

1. Highlight the bus by clicking on the bus' wire number column.
2. Click the **Expand Bus** icon.

Expanding a Bus

To Collapse an Expanded bus:

1. Highlight the bus by clicking on the bus' wire number column.
2. Click the **Collapse Bus** icon.

See Also

[Radix](#)

[Bus Ordering](#)

Radix

The combined numeric values of bussed signals can be displayed in one of several radices such as hexadecimal, binary, decimal, ASCII, analog and user mnemonics.

To select a radix:

1. Highlight the bus by clicking in the bus' wire number column.
2. Select **Bus** from the menu bar.
3. Click on the desired radix.

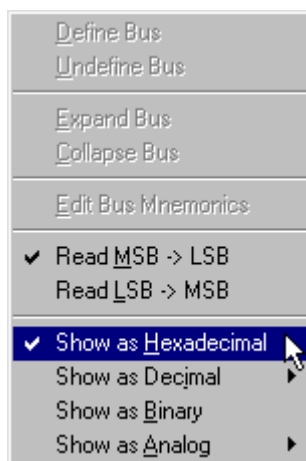


Figure 18 · Selecting Radix

Note: Note: The bus values will be incorrect if the order of the channels is backwards (MSB is in the LSB position). See [Bus Ordering](#) to correct the problem.

Bus Ordering

Bus ordering refers to the order in which channels are selected when a bus is defined.

Problems with bus ordering become apparent after a bus is created and data is captured. If the bus order is backwards, the data will also be backwards and may be unintelligible. Silicon Explorer software provides a way to specify the bit order, even after the bus has been defined.

To set the bus order:

1. Highlight the bus by clicking on the bus' wire number column.
2. Click the appropriate bus order icon.

See Also

[Radix](#)

Multiple Document Interface

The Multiple Document Interface lets users open several logic analyzer windows within the Silicon Explorer application. Each window is a unique analyzer session, containing its own trigger settings, channel labels,

data, etc. A window can also be a clone of another, containing the same data and settings, but with a different view (pan, zoom, etc.) of the data.

The active window has access to the logic analyzer hardware and is the only one that can capture acquisition data.

To create a copy of the current window, from the menu bar, select **Window > New Window**.

To create a new analyzer instrument, from the menu bar, select **File > New**, then click on the instrument desired.

To arrange the analyzer windows, from the menu bar, select **Window**, then **Cascade** or **Tile**.

To switch between analyzer windows:

Click within the desired analyzer window

or

From the menu bar, select **Window**, then click on the desired window name.

Timeline

A timeline is displayed along the top of the data display providing a time reference for acquired data. This reference can be presented in time units (seconds) or in samples. Additionally, vertical reference dots can be turned on (or off) providing a grid in the data display making time relationships between channels much easier to see.

To display the timeline in seconds:

1. From the menu bar, select **View > Timeline**.
2. Click **Time Units** to place a check next to it.

To display the timeline in samples:

1. From the menu bar, select **View > Timeline**.
2. Click **Samples (Hex)** or **Samples (Decimal)** to place a check next to the desired setting.

To enable or disable the reference dots:

1. From the menu bar, select **View**.
2. Click **Sample Dots** to place a check next to it.

Rearrange Channels

Channels can be rearranged so that related signals are displayed next to one another. Channel rearrange is also useful before grouping channels together as a bus.

To move a channel:

1. Press and hold the **Alt** key.
2. Position the cursor over the channel to be moved. A hand displays.
3. Click and drag the channel to the desired location.

Pattern

Pattern is a generic name describing a user defined template of logic conditions used for comparison with real data. Patterns may include any or all input channels, and are used for triggering, locating data and highlighting occurrences of data patterns.

To create a new pattern:

- From the **Pattern** menu choose **New Pattern**.
or
- Press the letter **P** on the keyboard.

To modify the logic conditions:

1. Place the mouse cursor over the Pattern column for the input channel(s) of interest.
2. Click the mouse button to cycle through the list of choices.
or

Right-click to display a list of choices and select an option from the drop-down menu.

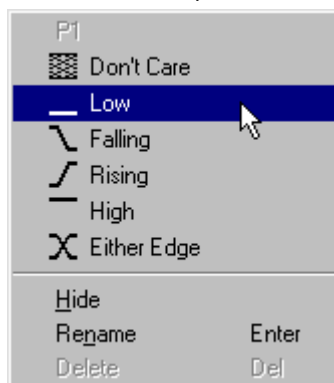


Figure 19 ·

Figure 20 · Pattern Column

To rename a pattern:

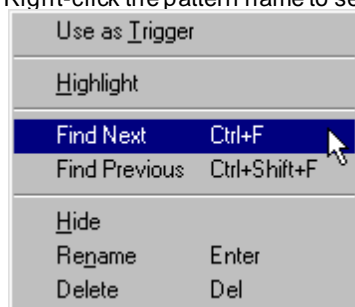
1. Click the pattern to highlight the pattern of interest.
2. Press **Enter**.
3. Type the new name and press **Enter**.

Find

Patterns can be used as to locate occurrences of specific logic conditions within the acquisition data. Once the logic conditions of interest are entered into the pattern, the find operation can take place.

Locating data using patterns:

1. [Create a pattern](#) containing the data conditions of interest.
2. Right-click the pattern name to select it.



3. Click Find Next or Find Previous. (You can also use the keyboard shortcuts Ctrl+F to Find and Ctrl+Shift+F to Find Previous.)

See Also

[Pattern](#)

[Trigger](#)

[Highlight](#)

[Keyboard Shortcuts](#)

Highlight

Silicon Explorer Patterns can be used to visually highlight the occurrence(s) of specified data patterns within acquisition memory.

To highlight data that matches a pattern:

1. [Create a pattern](#) containing the data conditions of interest.
2. Click the pattern heading (name) to highlight it.
3. From the **Pattern** choose **Highlight**.
4. Acquisition samples that match the data pattern are highlighted.

See Also

[Find](#)

[Trigger](#)

[Keyboard Shortcuts](#)

Data Files

Previously acquired data files can be opened for viewing and analysis. When saved, the files are given a ".bce" extension.

To open a file:

- From the **File** choose **Open**.
- Select Pod-A-Lyzer Files (*.bce) in the Files of Type box
- Click the desired file
- Click **File Open** icon

To close a file, from the **File** choose **Close**.

Acquisition data and setup information, such as the trigger condition, channel labels, etc., are stored together when saved to a file. This way, the analyzer display always looks the same as when it was last used.

To save a data file, from the **File** menu choose **Save** or click the **Save** icon.

Use the **Print** command to print an active window in Silicon Explorer.

Copy Display Data

State list display data may be copied, then pasted into an ASCII file in a tab-delimited format.

To copy state list data:

1. Place the mouse cursor over the wire number of the first column of data to be selected.
2. Click and drag the mouse to highlight all the data columns.
3. From the **Edit** choose **Copy**.

Readback Data

Data captured by an analyzer device is automatically transferred to the PC. It is sometimes useful to read that data again.

To readback data:

From the **Instrument** menu choose **Readback Data**.`Instrument` and then choose **Readback Data**.

See Also

- [Run Controls](#)

- [Multiple Document Interface](#)

Logic Analyzer Concepts

Synchronous Sampling

Synchronous sampling is supported only on Silicon Explorer I. Silicon Explorer II does not support synchronous sampling. Synchronous sampling uses a sample clock that is external to the logic analyzer - usually the clock from the system under test. This mode of operation is often referred to as State acquisition since the analyzer is capturing the state of all signals on every clock. The target clock must be connected to the wire labeled **CLKIN**. The clock ground wire must be connected for best signal integrity at high clock rates (> 20MHz). The Silicon Explorer does not require the clock to be an oscillator. However, it does require a continuous series of edges for operation.

State Display is a tabular display of logic activity, usually captured synchronously to an external clock. The data displayed on each horizontal line represents one recorded sample. The analyzer can display the recorded data in a variety of [radixes](#) (numerical formats) including binary, decimal, hexadecimal, analog, etc.

Clock Qualifier

State#	Signal Names						
	#	0	1	2:9	10	11	12:17
	Name	Vblank-	Vsync-	Video Address	Hblank-	Hsync-	Horiz Data
4C93		1	1	DD	0	0	30
4C94		1	1	DD	0	0	20
4C95		1	1	DD	0	0	01
4C96		1	1	DD	0	0	02
4C97		1	1	DD	0	0	05
4C98		1	1	DE	0	1	0B
4C99		1	1	DE	0	1	17
4C9A		1	1	DE	0	1	2E
4C9B		1	1	DE	0	1	1D
4C9C		1	1	DE	0	1	3A
4C9D		1	1	DE	0	1	35
4C9E		1	1	DE	0	1	2A
4C9F		1	1	DE	0	1	14
4CA0		1	1	DE	0	1	29

The Clock Qualifier is an external signal that acts as a gate for the acquisition clock. When the external signal is false, the acquisition clock is not allowed to load acquired data into acquisition memory.

The Clock Qualifier is useful when you want to observe signal activity taking place only when a particular chip is selected. For example, if the system under test has three devices of the same type connected to a common bus, one of which appears to be defective, you might want to record signal activity on the bus only when the suspect device is selected.

If the logic analyzer's Clock Qualifier input were connected to the chip select line of the device we were interested in, the analyzer would record data only when the chip's select line was active. The Clock Qualifier allows us to filter out irrelevant data by only clocking data of interest into the sample buffer.

To set up for Synchronous acquisition:

1. Connect the clock leads of the Target Cable Assembly to the target circuit clock signal.
2. From the Instrument menu, choose **Clock > Clock Edge** and click either **Rising** or **Falling** depending on which edge is appropriate.

Asynchronous Sampling

An acquisition that is made using a clock signal generated internally by the analyzer. This clock is unrelated to the clock in the target system, and can be set by you.

Timing Display

Timing display is a graphic representation of the timing relationships between input signals, displaying the recorded signal activity in timing diagram format. The screen fragment below shows a typical timing display in which multiple signals are displayed one on top of another. This type of display is ideal for understanding the "logic level vs. time" relationships between multiple channels at a single glance. Measuring the time between signal events is usually accomplished with the use of cursors.

Table 9 · Timing Display

Signal Name	Time > >																																								
<table border="1"> <thead> <tr> <th>Name</th><th>20480</th><th>2457</th></tr> </thead> <tbody> <tr><td>Vblank-</td><td></td><td></td></tr> <tr><td>Vsync-</td><td></td><td></td></tr> <tr><td>VQ7</td><td></td><td></td></tr> <tr><td>VQ6</td><td></td><td></td></tr> <tr><td>VQ5</td><td></td><td></td></tr> <tr><td>VQ4</td><td></td><td></td></tr> <tr><td>VQ3</td><td></td><td></td></tr> <tr><td>VQ2</td><td></td><td></td></tr> <tr><td>VQ1</td><td></td><td></td></tr> <tr><td>VQ0</td><td></td><td></td></tr> <tr><td>Hblank-</td><td></td><td></td></tr> <tr><td>Hsync-</td><td></td><td></td></tr> </tbody> </table>	Name	20480	2457	Vblank-			Vsync-			VQ7			VQ6			VQ5			VQ4			VQ3			VQ2			VQ1			VQ0			Hblank-			Hsync-				Waveforms (low vs. high)
Name	20480	2457																																							
Vblank-																																									
Vsync-																																									
VQ7																																									
VQ6																																									
VQ5																																									
VQ4																																									
VQ3																																									
VQ2																																									
VQ1																																									
VQ0																																									
Hblank-																																									
Hsync-																																									

Sample Rate

Sample rate is the speed at which the input signals are sampled, often expressed in mega-samples per second (MSa/s). Selecting the proper sample rate is important to ensure that signals are displayed accurately, and completely.

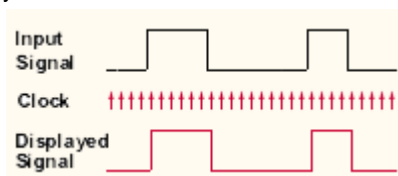


Figure 21 · Signal with Narrow Pulse

The example above shows a signal containing a narrow pulse at the end. In the case above, it is being sampled fast enough to capture the pulse. If the sample rate were slowed down, however, it would be possible to miss the narrow pulse entirely, as shown below.

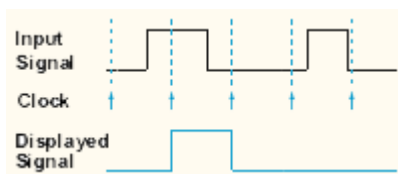


Figure 22 · Signal with Slowed Rate

To get adequate sample resolution, a good "rule of thumb" is to make sure the analyzer samples 4 to 10 times faster than the fastest signal being captured.

For example, if you wanted to capture a 40 nanosecond (ns) pulse, you would want the analyzer to sample at least 4 times faster ($40\text{ns}/4 = 10\text{ns}$). Sampling 10 times faster may not be practical since it would require an analyzer that samples every .4ns, or 2.5 giga-samples per second (GSa/s).

Capturing the entire signal

Logic analyzer sample buffers usually have a "fixed" size. This means that the faster memory is filled (the faster the sample rate), the shorter the overall acquisition time will be.

If you need to capture a burst of data that lasts 5 ms. Let's also assume the sample buffer can store 64K samples (actually 65536 samples since 64K is really 2^{16}). Simply divide 5ms by 65536 which results in 76.3 ns. In other words, with a 64K sample buffer and the analyzer sampling at 76 ns, it will capture 5 ms worth of signal activity.

In reality the analyzer probably has fixed sample rate steps (such as 200 ns, 100 ns, 50 ns, 20 ns, etc.). To comply with the requirements in the example above, we would not be able to sample faster than 76.3 ns and still capture 5 ms worth of data. The closest alternative would be 100 ns, which would result in 6.6 ms worth of data (65536 samples x 100 ns). Assuming 100 ns is fast enough to sample the input 4 times faster than the fastest signal ($100\text{ ns} * 4 = 400\text{ ns}$ pulse), we will meet our objectives for sample resolution and acquisition length.

Sample Resolution

Sampling Resolution is the interval (in seconds) between samples, determined by the frequency of the sample clock. Suppose, for example, that the sample clock was running at 100 MHz, and we were sampling on the rising edge as shown below. The sample resolution would be $1/100\text{ MHz}$, or 10 ns.

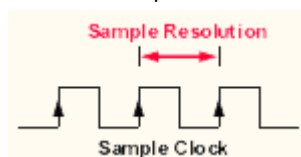


Figure 23 · Sample Resolution

When the timing analyzer samples an input line, it is either high or low. If the line is at one state (high or low) on one sample and the opposite state on the next sample, the analyzer "knows" that the input signal transitioned sometime in between the two samples. It doesn't know when, so it places the transition point at the last sample, as shown below.

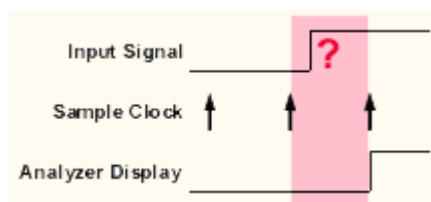


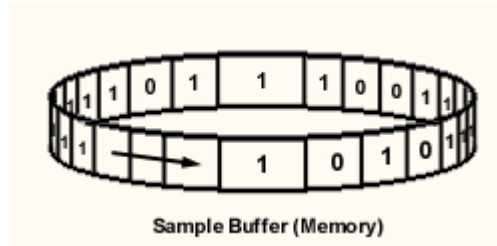
Figure 24 · Sample Uncertainty

This presents some uncertainty as to when the transition actually occurred and when it is displayed by the analyzer. Worst case for this uncertainty is one sample period, assuming that the transition occurred immediately after the previous sample point.

Understanding Triggering

Triggering is the process of halting the logic analyzer after a specific event has occurred. The event is typically called a trigger pattern and is the logical and of logic conditions on one or more channels. In multi-level triggering, several logic events may be required to occur before the analyzer triggers.

It is helpful to understand how acquisition memory applies to the trigger process:



Conceptually, the acquisition memory acts as a circular buffer. Once the analyzer is started, samples are stored in sequence. If the analyzer fills memory before a trigger occurs, it will continue to acquire data with the newest data over-writing the oldest. Once a trigger occurs, the analyzer will either:

1. Stop immediately - acquisition memory contains waveform data of signal activity leading up to the trigger only (also called pre-trigger data).
2. Fill the entire memory once more - acquisition memory contains waveform data of signal activity that occurred after the trigger (also called post-trigger data).
3. Fill only a portion of memory - acquisition memory contains both pre-trigger and post trigger information.

Trigger

By default, the Silicon Explorer software contains a trigger pattern, identified by a red font. Other patterns, however, can be selected for use as the trigger pattern.

Selecting a pattern to trigger the analyzer:

1. Click the pattern of interest to highlight it.
2. From the **Pattern** choose **Use as Trigger**. The pattern name is displayed in a red font signifying that this is now the trigger pattern.

See Also

[Pattern](#)

[Find](#)

[Highlight](#)

Auto-Trigger

Auto-trigger lets you view the captured data dynamically. Acquisitions are made, the display updated and the analyzer started for the next capture automatically. The rate at which the display is updated depends upon the amount of data being viewed and the frequency of the trigger event. The fastest update is about once every second.

To start auto-trigger:

- Toolbar: Click the **AUTO TRIGGER** icon.
- From the **Instrument** menu choose **Run Auto Trigger**.
- Keyboard: Press the letter **A**.

To halt auto-trigger:

- Toolbar: Click the **HALT** icon.
- From the **Instrument** menu choose **Stop**.
- Keyboard: Press the letter **S**.

See Also

[Understanding Triggering](#)

Triggering

The Silicon Explorer software supports both single-level and multi-level triggering depending on whether you are connected to a Silicon Explorer or a Silicon Explorer II. Select the device you are using from the list in the device menu.

Triggering Silicon Explorer

The Silicon Explorer has a single-level trigger sequence with a selectable trigger position. Silicon Explorer II has up to four-levels in its trigger sequence.

Trigger Pattern

A trigger pattern is the logical AND of the trigger conditions set on all 18 channels. Each channel may be set to one of the following trigger conditions:

- Don't Care
- High
- Low
- Rising Edge
- Falling Edge
- Either Edge

To set the trigger condition for a single channel:

Right-click the trigger pattern column of the desired channel and choose the trigger condition.

To set the trigger pattern for a group of bussed signals:

1. Click the Trigger Pattern column of the channel bus.
2. Enter the pattern using the keyboard, using the same radix as the bus.

To select a pattern to trigger the analyzer:

1. Click to select the pattern of interest.
2. From the **Pattern** menu choose **Use as Trigger**. The pattern name is displayed in a red font, indicating that this is now the trigger pattern.

Trigger Position

The Trigger Position controls determines how much of the captured data came before the trigger and how much came after. There are three possible settings:

- Early (25% pre, 75% post)
- Center (50% pre, 50% post)
- Late (75% pre, 25% post)

To set the trigger position from the menu bar:

1. On the Instrument menu select Trigger Position
2. Click on the desired position (Early, Center, or Late)

See Also

[Understanding Triggering](#)

Analyzer Controls

Probe Instrument

Probe files are generated from Designer software and contain device information, net names, and node location information. This information is displayed in a tree structure for verification. For Axcelerator devices, the net name is prefixed by the tile number the module is on. e.g. net <0,1>ALU_test_mod_d is .on tile 0,1.

Once a *.prb file is opened and a device connection has been made then the checksum of the target device can be read and compared against the checksum in the file. This ensures that the selected probe file matches the target device.

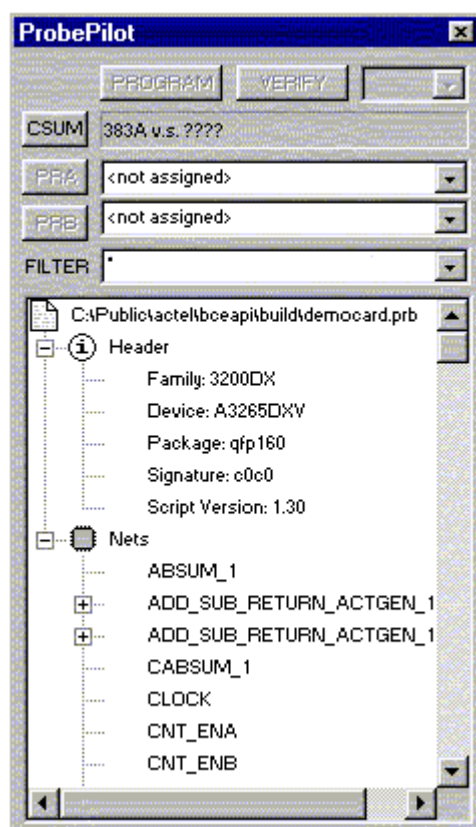


Figure 25 · Display for non-Axcelerator Devices

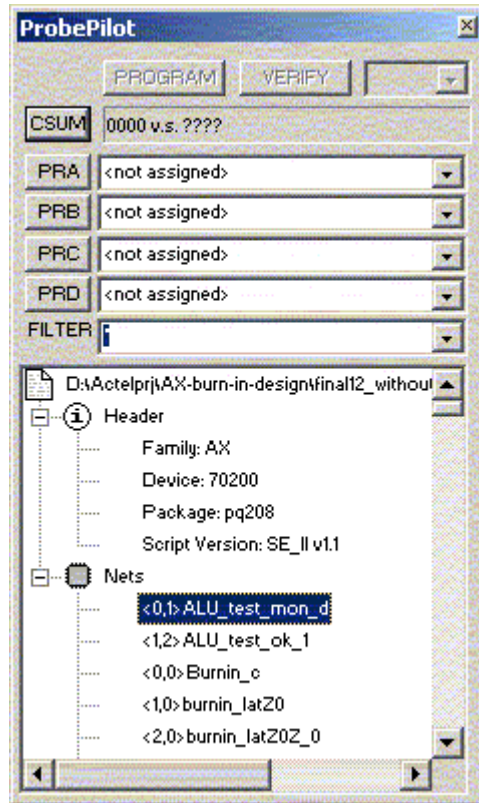


Figure 26 · Display for Axcelerator devices

Open a Probe File

Note: Note: Designer R398 or later is required. (Designer R1-2002 SP2 or later is required for Axcelerator)

To open a file:

1. From the **File** menu choose **Open > Files of type (*.prb)**.
2. Double click the desired probe file.

Assign a Probe

To assign a node to a probe:

1. Click the node to select it.
2. Click the **PRA** or **PRB** button. (PRA, PRB, PRC, or PRD for Axcelerator devices)

The selected node is routed to the probe pin and the corresponding analyzer input switched to the debug connector. The net name will also appear in the waveform window.

Note: Note: For Axcelerator devices, only the Probe A and Probe B pins will be automatically switched to the corresponding analyzer input. You must connect the Probe C and Probe D pins to CH3 and CH4 respectively. The net names for Probe C and Probe D automatically appear in the current waveform window for CH3 and CH4 unless you have already typed a name for the channel.

Display Features

The tree control lists the nets or pins in the design. To format the display, right-click the Nets branch. Use the FILTER field to filter the list. Wildcards (* ?) are supported.

A history is maintained on the probe and filter lists (PRA, PRB, PRC, PRD, and FILTER) accessible from the pull-down button.

Run Controls

Several controls are provided to start and stop the analyzer instrument, including an auto-trigger mode which continually triggers, captures and re-arms for the next capture. Facility is also provided to readback data from the instrument which is very useful when using [multiple analyzer windows](#).

To start an acquisition:

- Tool bar: Click the **RUN** icon
- From the **Instrument** choose **Run**
- Keyboard: Press the letter **R**

To halt an acquisition:

- Tool bar: Click the **HALT** icon
- From the **Instrument** menu choose **Stop**
- Keyboard: Press the letter **S**

See Also

[Auto-Trigger](#)

[Readback Data](#)

Sampling

Signals may be sampled synchronously, using an external clock, or asynchronously, using the logic analyzer's internal clock. Sample rate specifications are listed in the [specifications](#) section of the online help.

To set up for synchronous acquisition:

1. Connect the clock leads of the Target Cable Assembly to the target circuit clock signal.
2. From the Instrument menu, choose **Clock > Clock Edge** and click either **Rising** or **Falling** depending on which edge is appropriate.

To set the asynchronous sample rate from the tool bar:

1. From the **Instrument** menu, choose **Clock**.
2. Scroll down the list of sample rates until the desired rate is selected, then click the left mouse button.

To set the asynchronous sample rate from the menu bar:

1. From the **Instrument** menu, choose **Clock**.
2. Scroll down the list of sample rates until the desired rate is selected, then click select it.

See Also

[Understanding Synchronous Sampling](#)

[Understanding Asynchronous Sampling](#)

Troubleshooting Silicon Explorer

Troubleshooting Errors

Q&A

Q1	I've connected Silicon Explorer and the waveform window display reads POLL.
A1	Look on the top of the Silicon Explorer for the flashing yellow "heartbeat", if it is not flashing then make sure you have properly connected an adequate power supply.

Q2	It's flashing but still POLL.
A2	<p>There are a number of things that can prevent communication from being established. The following are the most common:</p> <p>Wrong COM port. Try all four COM ports even though you are sure that your mouse is on COM 1.</p> <p>No power to the analyzer.</p> <p>Desktop systems external COM connector not connected to the COM port internally.</p> <p>Laptop systems external COM connector disabled (IR Port Override?). Use your PC's CMOS setup program to enable the COM port.</p> <p>COM port IRQ reassigned for DOS program, control panel not updated.</p> <p>Multiple mouse drivers in <code>system.ini</code>.</p> <p>Third-party serial port "enhancers" not conforming to windows API.</p>

Q3	I've got the IDLE message but when I click RUN, the Waveform window flashes an error message and returns to IDLE.
A3	If the target power is incapable of supplying the necessary current, then the Waveform window resets and returns to IDLE. Many current-limiting supplies will trip when set too close to the operating current.

Q4	The Waveform window acquires data and then indicates errors on readback.
A4	<p>The Waveform window bursts data back in blocks at high speed, with built-in retry for a bad block (both checksum and byte count are used). Some third-party serial programs block all interrupts forcing the analyzer into a retry loop.</p> <p>Some laptops power down the UART and drop a few characters. Try disabling "Power Saving" in the CMOS setup menu.</p>

Q5	When the Waveform window is open, my other Windows programs run slowly.
----	---

A5	If the Waveform window is open but it is not connected or powered up, then the system is constantly timing out looking for a response. Either close the Waveform window or change the COM port to DEMO.
----	---

Q1	The Analyze module acquires data and then indicates errors on read-back. Why?
A1	The Analyze module bursts data back in blocks at high speeds, with built-in retry for a bad block (it uses both checksum and byte count). Some third-party serial programs block all interrupts, forcing the analyzer into a retry loop. Some laptops power down the UART and drop a few characters. Try disabling "Power Saving" in the CMOS setup menu.

Q	When the Explore window is open, my other Windows programs run slowly. Why?
A	If the Explore window is open but not connected or powered up, then the system is constantly timing out looking for a response. Either close the SE II window or change the COM port to DEMO.

Q	I get a message "Device Timed out" when I try to assign a particular signal to the Probe pins. Why?
A	This message gives us an indication that the power is not sufficient for the Silicon Explorer and as a solution you would have to add a separate power source for the Silicon Explorer. Refer to Powering Silicon Explorer II for more information.

Q	I have assigned an internal signal to PRA and PRB but the PRA and PRB light is not blinking on the Probe Pilot. Is this normal?
A	The PRA and the PRB light on the Probe Pilot are just an indication of the logic level of that assigned internal signal. If the assigned internal net is at permanent logic 0, the light on the Probe Pilot for the corresponding probe will not glow.

Q	Where are my TMS and SDO pins?
A	Your cable will not have the TMS and the SDO pins if it was bought before the SX probing capability was introduced. To order a new cable (Si-Ex-Ribbons), contact Actel customer service at Customer.Service@actel.com .

Q	Is the Silicon Explorer displaying an incorrect signal?
A	Make sure that the signal is sampled at a sufficiently high frequency. The sampling rate should be at least twice the frequency of the fastest changing signal. The maximum frequency at which the signal can be sampled is 100 MHz which limits the frequency of the device to 50 MHz. If a higher sampling frequency is required than the PRA and the PRB pins can be connected to a logic analyzer to view the signals.

Q	Why can't I find the net I wish to probe?
A	Silicon Explorer lists only the signals that are actually present on the device. There is a possibility that the net which you wish to probe has been optimized in Designer. Please check the list of the nets combined in the combiner file (*.cob) which is exported from Designer File > Export > Auxillary File with file type *.cob

Q	What are the limitations in probing devices using Silicon Explorer?
A	Probing limitations are described in the table below. Note that -- indicates that the feature is unavailable, and * indicates that the feature only applies to devices that have Qclock.

Figure 27 · Probing Limitations

Family	Probe Capable			
	Input	Clock	Hclock	Qclock
ACT1/40MX	Y	Y		
ACT2/XL/42MX	Y	Y		
ACT3	Y	Y	Y	
DX/42MX	Y	Y		Y*
SX/SX-A/eX	N	Y	N	N*

Troubleshooting General

The following is a list of frequently asked questions.

Q	Does Silicon Explorer support ProASIC programming and debugging?
A	No. As of today Silicon Explorer does not support either ProASIC programming or debugging.

Q	Can we use Silicon Explorer to debug devices which have their security fuses programmed?
A	As a part of the FPGA security feature the Silicon Explorer cannot be used on devices which have their security fuse programmed.

Troubleshooting Software

Q	How do I set up triggering?
---	-----------------------------

A	You have an option of setting trigger either EARLY that displays the values in the ratio of (25% 75%), where the first % represents the % of data sampled before the trigger point and the later % represent % sampled after the trigger point. The other options available are CENTER(50% 50%) and LATE(75% 25%). You can select the trigger position from Instrument -> Trigger Position and then selecting the required Trigger position.
---	--

Q	What is the recommended sampling rate?
A	For an accurate reading, the sampling rate for a particular signal should be at least twice the rate at which the signal is changing (According to the Nyquist theorem). For example, a clock operating at 25 MHz should be sampled at least 50 MHz frequency. Be aware that sampling at higher frequencies causes the Silicon Explorer to consume more power.

Q	What is the best way to find nets?
A	The best way to find the nets in the Silicon Explorer is to use the Filter option available in the software. You can search for the net you require by using the *partial_name* in the filter, which would return all the signals having that partial_name of the net. If you are using an HDL flow, it may be difficult to recognize the net names you need to observe. Microsemi recommends that you use a synthesis tool that can generate a gate-level schematic of your synthesized netlist so that during probing, you can easily trace through the schematic and obtain the net names from it.

Troubleshooting Hardware

Q	How do I probe an SX-A device?
A	The probing of an SX-A device requires special setup because it requires a 70 ohm termination on all the probe connectors (TDI, TDO, TCK, TMS, PRA, PRB). The 70 ohm series termination is used to prevent data transmission corruption during probing.

Q	How do I tie the TRST pin during the probing using Silicon Explorer?
A	<p>TRST is an active low input. During JTAG mode and Silicon Explorer debugging mode, JTAG state machine's reset must not be active, otherwise probe circuitry is disabled. The recommendation for TRST pin in JTAG and Silicon Explorer is listed below:</p> <p>RTSX Rev0 - No TRST pin RTSX Rev1 - You must tie TRST pin high when doing JTAG and Silicon Explorer.</p> <p>RTSX Rev2 - You can leave the TRST pin floating (or drive it high - it must not be driven low) when running JTAG or Silicon Explorer if "Reserve JTAG TRST" was selected in Designer.</p> <p>SXA - You can leave the TRST pin floating when running JTAG or Silicon Explorer</p>

Q	What are the different options that I have to connect a device to Silicon Explorer Probe Pilot?
A	You can connect the Silicon Explorer to the device by either implementing a probe connector on the board for use with the ribbon connector or by connecting the device to the Probe-Pilot using the flying lead connector. If you choose the second alternative, you can either use posts on your board or the clips provided with the Si Explorer to connect directly to the probe pins.

Q	Where can I find the pin layout of the Silicon Explorer?
A	The pin layout for the Silicon Explorer is found on the back of the Silicon Explorer case. There is a notch on one side of the pin connector that determines the position of Pin 1.

Q	How is the checksum of the device read?
A	The checksum of most devices is read through the TDO/SDO pin. Refer to the SDO pin locations sections for information about the location of SDO pins in all Microsemi Devices. ACT1 and the 40MX pins do not have an SDO pin. In order to read the checksum from ACT1/40MX devices the PRA on the device must be connected to the SDO pin of the Silicon Explorer.

Q	What are the power requirements for Silicon Explorer II?
A	Silicon Explorer II must be connected to a power supply of 5V for 5V tolerant devices, 3.3V for 3.3V tolerant devices, and 2.5V for 2.5V tolerant devices.

Debugging AX/eX/SX/SX-A Devices Using Silicon Explorer II

AX, eX, SX, and SX-A devices may require additional attention when debugging. You must control probing on AX, eX, SX and SX-A devices through the IEEE 1149.1 pins. You may configure the IEEE 1149.1 pins as dedicated (JTAG only) or flexible (JTAG or I/O). This section assists you with these and other considerations when debugging SX, SX-A, or eX devices.

Probe Circuit Control Pins

The Silicon Explorer II tool uses the IEEE 1149.1 pins (TDI, TCK, TMS and TDO) to select the desired nets for debugging. Assign the selected internal nets to the PRA/PRB pins for observation. The figures below show the connections between Silicon Explorer II and the SX/SX-A/eX FPGA required for you to perform in-circuit debugging and the Axcelerator Silicon Explorer II Setup.

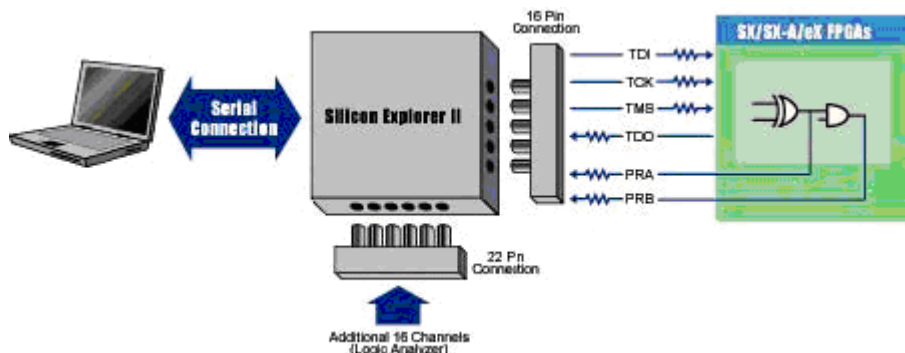


Figure 28 · eX/SX/SX-A Setup

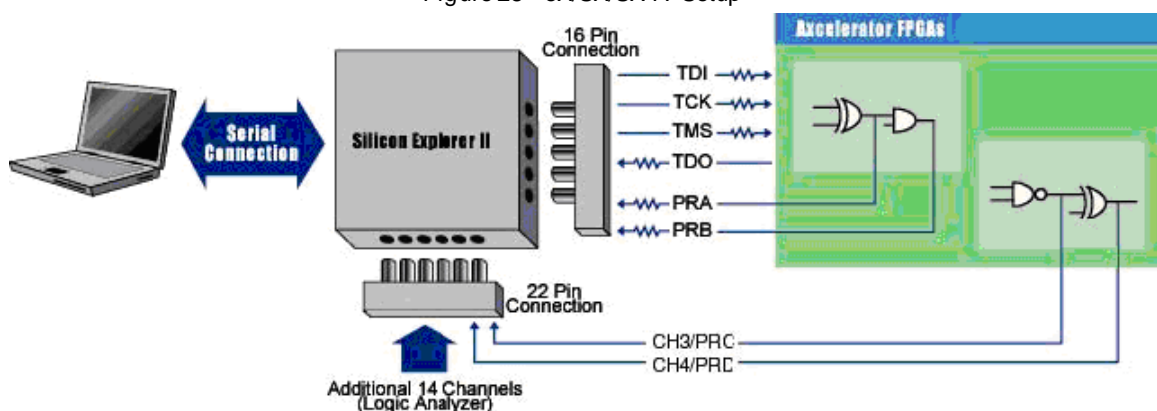


Figure 29 · Explorer Setup

Diagnostic Pin Consideration

To place the IEEE 1149.1 (JTAG) and probe pins (TDI, TCK, TMS, TDO, PRA and PRB) in the desired mode, select the appropriate check boxes in the "Device Variations" dialog box. This dialog box is accessible through the Design Setup Wizard under the Option menu in Designer.

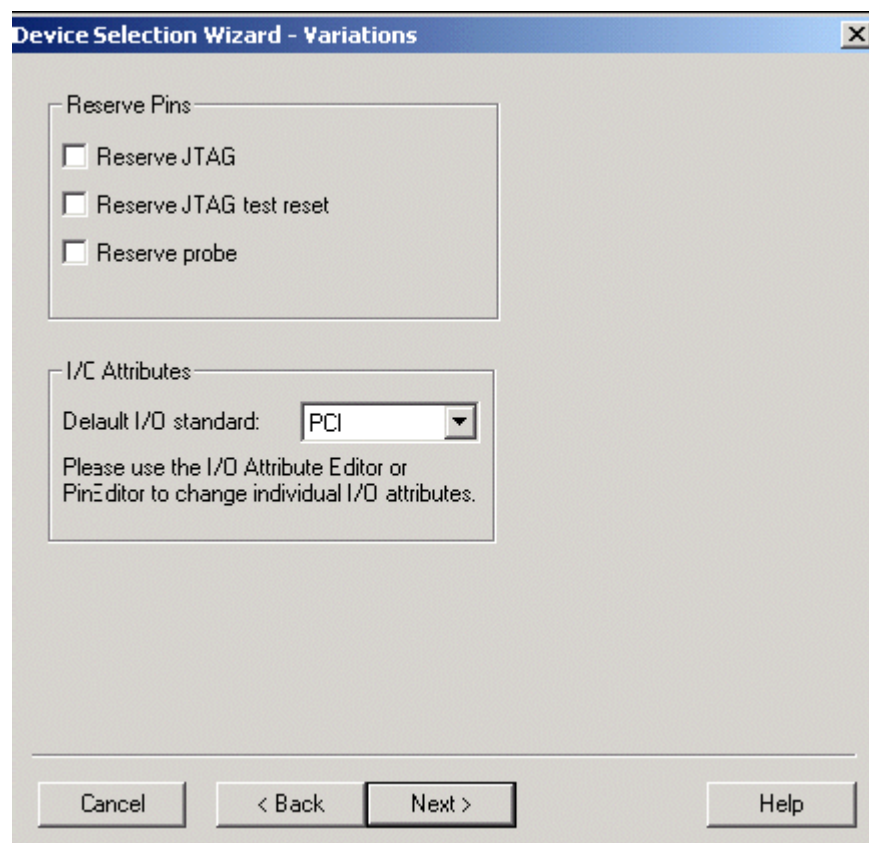


Figure 30 - Diagnostic Pins Configuration

To access the Device Variations dialog box in Designer:

1. Launch Designer.
2. Open your design.
3. From the Options menu choose Device Setup. The Device Selections dialog box appears.
4. Click Next. The Device Variations dialog box appears.

Dedicated JTAG Mode

When you select the “Reserve JTAG Pin” box, you place the FPGA in Dedicated JTAG mode, which configures TDI, TCK, and TDO pins for JTAG boundary scan or in-circuit debug with Silicon Explorer II. Also, you enable an internal pull-up resistor on both the TMS and TDI pins (see figure below). In addition, by checking the “Reserve JTAG Pin” box, TDI, TCK and TDO are not available for pin assignment in the Pin Editor.

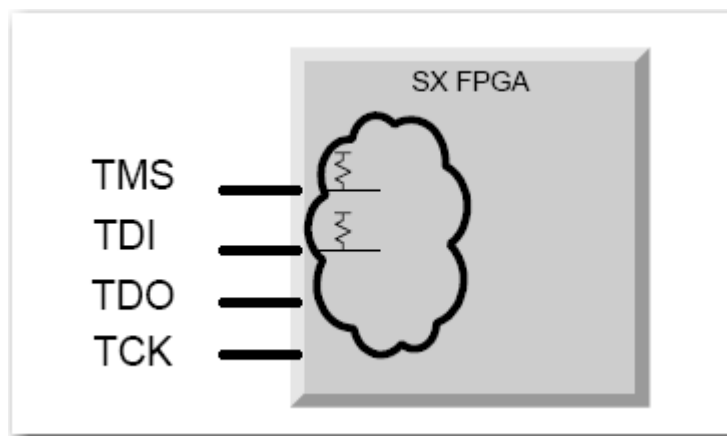


Figure 31 · Dedicated JTAG Mode

You do not need to specify an internal pull-up resistor; SE II automatically configures TMS and TDI with internal pull-up resistors.

Flexible JTAG Mode

When you do not select the “Reserve JTAG Pin” box, you place the FPGA in Flexible JTAG mode, where TDI, TCK and TDO pins may function as user I/Os or JTAG pins. When you select Flexible JTAG mode, you disable the internal pull-up resistors on the TMS and TDI pins. Note that you require an external 10K Ohm pull-up resistor on the TMS pin in this mode (figure below). Silicon Explorer II transforms TDI, TCK and TDO pins from user I/Os into JTAG diagnostic pins when a rising edge at TCK is detected while TMS is at logical low. The JTAG pins revert to user I/Os when the JTAG state machine is in the Test-Logic reset state.

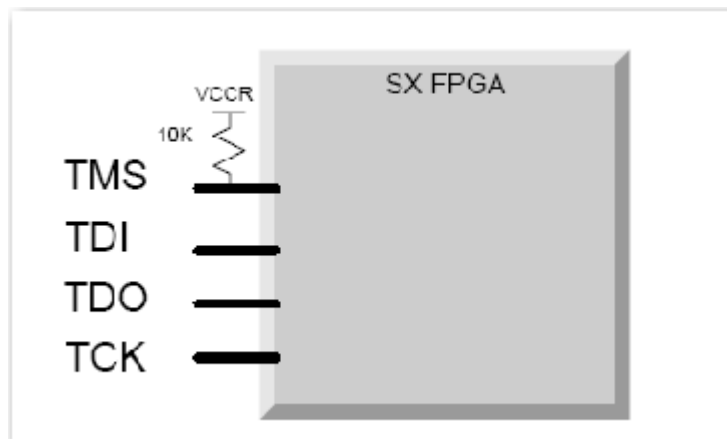


Figure 32 · Flexible JTAG Mode with 10K Pullup Resistor

The table below shows the possible configurations of the diagnostic pins.

Table 10 · Diagnostic Pin Configuration

Dedicated JTAG Mode	Flexible JTAG Mode
TCK, TDI, and TDO are dedicated diagnostic pins.	Use TCK, TDI and TDO as I/O's. You need a 10K pull-up resistor on the TMS Pin.

Probe Pins

When you select the Reserve Probe Pin box, you direct the layout tool to reserve the PRA and PRB pins as diagnostic pins. This option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be

user I/O's to achieve successful layout, then the tool will use these pins as user I/Os. If you assign user I/Os to the PRA and PRB pins and select the Reserve Probe Pin option, the Layout tool overrides the "Reserve Probe Pin" option.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, critical input signals through these pins are not available. In addition, do not program the Security Fuse. Programming the Security Fuse disables the Probe Circuit. However, you can still read the checksum.

Internal Probing Feature for Antifuse Families

Depending on the status of the MODE pin and whether or not the security fuse was programmed, the I/O capability of the probe pins varies. The probe pins are the PRA, PRB, SDI, and DCLK pins and are used by the Silicon Explorer for internal signal probing. Consult the Pin Editor or the I/O Attribute Editor to determine the pin numbers for these pins in the device you are using. The following tables show the I/O capability of the probe pins for all the MODE/Security combinations.

Table 11 · ACT 1 and 40MX Devices

Mode	Program	Probe	PRA, PRB	SDI, DCLK
Low	No	No	User Defined I/O	User Defined Input
Low	No	Yes	User Defined I/O	User Defined Input
Low	Yes	No	User Defined I/O	User Defined I/O
Low	Yes	Yes	User Defined I/O	User Defined I/O
High	No	No	Probe Circuit Outputs	Probe Circuit Inputs
High	No	Yes	Probe Circuit Disabled	Probe Circuit Disabled
High	Yes	No	Probe Circuit Outputs	Probe Circuit Inputs
High	Yes	Yes	Probe Circuit Disabled	Probe Circuit Disabled

Table 12 · ACT, 1200XL, 3200DX, ACT 3, 42MX

Mode or TMS	Security	PRA, PRB	SDI/TDI, DCLK/TCK
Low		User Defined I/O	User Defined I/O
High	No	Probe Circuit Outputs	Probe Circuits Inputs
High	Yes	Probe Circuit Disabled	Probe Circuit Disabled

Table 13 · SX, eX, SX-A, AX

TMS	Security	PRA, PRB, (PRC, PRD) ¹	TDI, TCK
Low		User Defined I/O	User Defined I/O
High	No	Probe Circuit Outputs	Probe Circuit Inputs

TMS	Security	PRA, PRB, (PRC, PRD) ¹	TDI, TCK
High	Yes	Probe Circuit Disabled	Probe Circuit Disabled

¹ The Axcelerator family, with the exception of AX125, has PRA, PRB, PRC, and PRD pins. AX125 only has PRA and PRB pins.

SDO Pin Locations

ACT2 and 1200XL Families

The tables below show SDO pin numbers for ACT2 and 1200XL families.

Note: Note: If the SDO pin is configured as an input, do not use Silicon Explorer.

Figure 33 · A1225A/A1225XL

Package	SDO Pin Number
PLCC8452	52
CPGA100	J9
PQFP100	52
VQFP100	50

Figure 34 · A1240A/A1240XL

Package	SDO Pin Number
PLCC84	52
PQFP100	52
CPGA132	N12
PQFP144	71
TPFP176	87

Figure 35 · A1280A/a1280XL

Package	SDO PinNumber
PLCC84	52
PQFP160	82
CFP172	85
CPGA176	P13
TFP176	87
PQFP208	103

ACT3 Family SDO Pin Locations

The tables below show SDO pin numbers for ACT3 families.

Note: Note: If the SDO pin is configured as an input, do not use Silicon Explorer.

Note:

Figure 36 · A1415

Package	SDO Pin Number
PLCC84	52
CPGA100	19
PQFP100	77
VQFP100	49

Figure 37 · A1425

Package	SDO Pin Number
PLCC84	52
PQFP100	77
VQFP100	49
CPGA132	63
CPGA133	M11
PQFP160	79

Figure 38 · A1440

Package	SDO Pin Number
PLCC84	52
VQFP100	49
PQFP160	79
CPGA175	N12
FQFP176	87

Figure 39 · A1460

Package	SDO Pin Number
PQFP160	79
TQFP176	87

Package	SDO Pin Number
CQFP196	99
CPGA207	P15
PQFP208	103
BGA225	N13

Figure 40 · A14100

Package	SDO Pin Number
RQFP208	103
CQFP256	126
CPGA257	R17
BGA313	AE23

A3200 Family SDO Pin Locations

The tables below show SDO pin numbers for A3200 Family pin locations.

Note: Note: If the SDO pin is configured as an input, do not use Silicon Explorer.

Figure 41 · A3265DX

Package	SDO Pin Number
PLCC84	52
PQFP100	52
PQFP160	82
TQFP176	87

Figure 42 · A32100DX

Package	SDO Pin Number
CQFP84	42
PLCC84	52
PQFP160	82
TQFP176	87
PQFP208	103

Figure 43 · A32140DX

Package	SDO Pin Number
PLCC84	52
PQFP160	82
TQFP176	87
PQFP208	103
CQFP256	67

Figure 44 · A32200DX

Package	SDO Pin Number
CQFP208	103
PQFP208	103
RQFP208	106
RQFP240	123
CQFP256	67

Figure 45 · A32300DX

Package	SDO Pin Number
RQFP208	106
RQFP240	123
CQFP256	67

A42MX SDO Pin Locations

The tables below show SDO pin numbers for A2MX families.

Note: Note: If the SDO pin is configured as an input, do not use Silicon Explorer.

Figure 46 · A42MX09

Package	SDO Pin Number
PLCC84	52
PQFP100	52
VQFP100	50
PQFP160	82
TQFP176	87

Figure 47 · A42MX16

Package	SDO Pin Number
PLCC84	52
PQFP100	52
VQFP100	50
PQFP160	82
TQFP176	87
PQFP208	103

Figure 48 · A1440

Package	SDO Pin Number
PLCC84	52
VQFP100	49
PQFP160	79
CPGA175	N12
FQFP176	87

RT SDO Pin Locations

The tables below show SDO pin numbers for RT families.

Note: Note: If the SDO pin is configured as an input, do not use Silicon Explorer.

Figure 49 · RT1280A/RH1280

Package	SDO Pin Number
CQFP	85

Figure 50 · RT1425A

Package	SDO Pin Number
CQFP132	63

Figure 51 · RT1460A

Package	SDO Pin Number
CQFP196	99

Figure 52 · RT14100A

Package	SDO Pin Number
CQFP256	126

Note: Note: ACT1 and 40MX device families do not contain SDO pins. PRA from the device must be connected to SDO input of Silicon Explorer. Devices not listed (i.e. 42MX24/A42MX36, SX, eX, SX-A, RTSX, RTSX-S, and AX), contain a TDO pin. Please check the "Package Pin Description" section of the appropriate datasheet at <http://www.actel.com/techdocs/ds/default.aspx>.

Specifications

Silicon Explorer Specifications

Table 14 · Specifications

Input	
Channels	18 plus external clock
Sample Rate	1kSa/s to 100 MSa/s
Minimum Pulse Width	7 nsec
Buffer	64K samples per channel
Setup/Hold	2.1 nsec / 0 nsec
Impedance	220k ohm, 10pf typical
Input Voltage	+7V to -3V max
Clock	
Asynchronous	1kSa/s to 100 MSa/s
Synchronous	0 to 66MHz
Trigger	18 channel word recognition High, low and don't care levels on all channels Built-in edge detection for rising, falling or either edge Silicon Explorer: 1 level of trigger Silicon Explorer II: 4 levels of trigger
Operating Environments	
Temperature	0° to 30° Celsius
Power	+3V to +5.5V @ 1.25A maximum
Compliance	CE
System Requirements	See the latest Silicon Explorer Release Notes on www.actel.com for System Requirements.

Accessories

The following accessories are available for Silicon Explorer.

Quick Probe Clips

The Quick Probe Clips kit contains 10 micrograbbers for connecting the target cable assembly to test points on the target board.

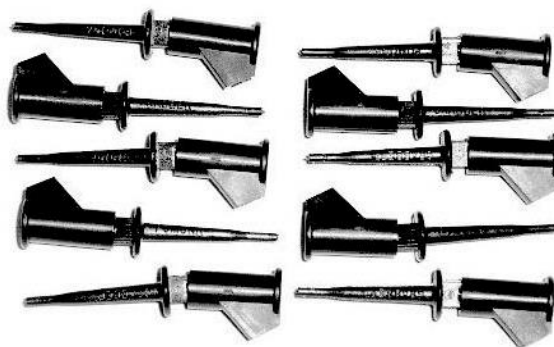


Figure 53 · Quick Probe Clips

TCA Cable

The TCA cable kit contains a replacement logic analysis cable for connecting the 18 channel inputs to the target board.

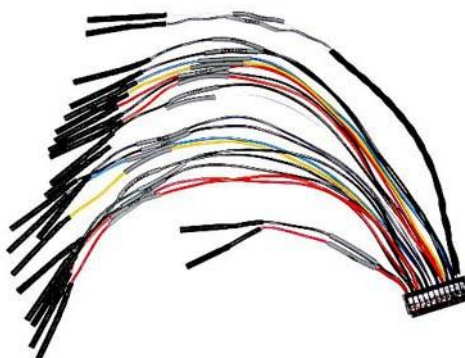


Figure 54 · TCA Cable

Ribbon and Breakout Cables

The Ribbon and Breakout cables accessory kit contains replacement cables for connecting the JTAG control port of the Silicon Explorer to the target board. The Ribbon cable mates with a standard 16 pin header on the target board. The Breakout cable has individual contacts on the target end to mate with individual test points on the target board. The Breakout cable can also be used with the Quick Probe Clips to make connection to the target board.



Figure 55 • Ribbon and Breakout Cables

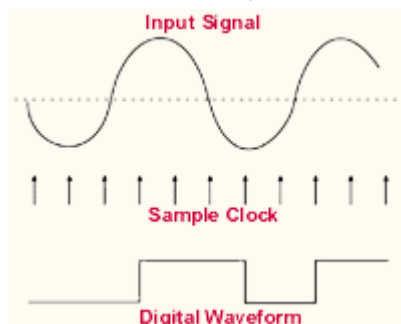
Glossary of Terms

[A](#) [B](#) [C](#) [D](#) [E](#) [F](#) [G](#) [H](#) [I](#) [J](#) [K](#) [L](#) [M](#) [N](#) [O](#) [P](#) [Q](#) [R](#) [S](#) [T](#) [U](#) [V](#) [W](#) [X](#) [Y](#) [Z](#)

A

Acquisition - The sampling of data from a system under test. Data is stored in acquisition memory so it can be displayed in different formats or compared to other acquired data.

Acquisition Clock - The clock that determines the rate at which the logic analyzer samples data. The clock can be an internal analyzer clock with user-selectable sample rate (asynchronous), or it can be an external clock with the sampling rate determined by the system under test (synchronous).

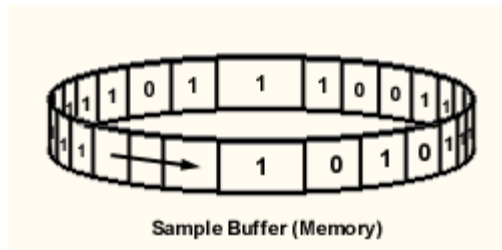


From these sample points, a list of ones and zeros is generated that represents a one-bit picture of the input waveform. As far as the analyzer is concerned, the waveform is either high or low, no intermediate steps. This list is stored in memory and is also used to reconstruct a one-bit picture of the input waveform, as shown above.

The sample clock can be generated internally by the logic analyzer. This is often referred to as *Asynchronous* sampling, since the sampling is *not* synchronous to any signal in the circuit under test. This mode is also referred to as *Timing Mode* since the display shows the *timing* relationships between input signals. To get accurate timing information it is necessary that the [sample rate](#) of the clock is faster than the rate at which the signals change.

An external signal may also be used as the sample clock. This sampling mode and is referred to as *Synchronous* sampling since it is synchronous to an external signal, usually from the system under test. It is also referred to as *State Mode* since the display shows the *state* of the input signals at the moments when the clock occurred. See also [external clock](#) and [internal clock](#).

Acquisition Memory - The memory in which data acquired by the logic analyzer is stored. Logic analyzers typically have memory to store several thousand samples per channel.



Conceptually, the acquisition memory acts as a circular buffer. Once the analyzer is started, samples are stored in sequence. If the analyzer fills memory before a trigger occurs, it will continue to acquire data with the newest data over-writing the oldest. Once a trigger occurs, the analyzer will either:

1. [pre-trigger data](#)
2. [post-trigger data](#)
3. [pre-trigger post trigger](#)

Aliasing - The condition that occurs when data from the target system is sampled at a rate slower than the rate at which data changes. When this happens, meaningless data is displayed because the analyzer misses the changes in data that occurred between sample points.

ASCII - stands for American Standard Code for Information Interchange. ASCII is an eight bit numeric code that represents text characters.

Asynchronous Acquisition - An acquisition that is made using a clock signal generated internally by the analyzer. This clock is unrelated to the clock in the target system, and can be set by the user.

B

Bus - See [Channel Bus](#)

C

Channel - An input signal line used by the logic analyzer to acquire data.

Channel Bus - A user-defined group of input channels whose combined numeric value is displayed in a user specified [radix](#).

Clock - The regular signal pulse that determines the sampling rate for the logic analyzer. See also [acquisition clock](#), [external clock](#), and [internal clock](#).

Clock Qualifier - An external signal that acts as a *gate* for the acquisition clock. When the external signal is false, the acquisition clock is not allowed to load acquired data into acquisition memory.

The Clock Qualifier is handy when we only want to observe signal activity taking place when a particular chip is selected. For example, if the system under test has three devices of the same type connected to a common bus, one of which appears to be defective, we might want to record signal activity on the bus only when the suspect device is selected.

If the logic analyzer's Clock Qualifier input were connected to the chip select line of the device we were interested in, the analyzer would record data only when the chip's select line was active. The Clock Qualifier allows us to filter out irrelevant data by only clocking data of interest into the sample buffer. See also [acquisition memory](#).

Collapse Bus - The process of returning a channel bus from its expanded view to its bus view. See [expand bus](#).

Condition - A value or event which the logic analyzer can recognize. A condition can be a transition on a single channel, a combination of logic highs and lows across multiple channels, a certain number of clock cycles, etc. See also [pattern](#).

Cursor - A vertical line representing a specific location on the logic analyzer display.

D

Define Bus - The process of grouping a set of related signals together as a single, composite signal whose value is the numeric combination of signals it contains. See [undefine bus](#).

Don't Care - A symbol indicating that the channel(s) associated with the symbol may be any logic logic value and the trigger, find or highlight pattern will still match. (see [find](#), [highlight](#), and [trigger](#))

Download - The process of transferring acquisition memory contents from the Pod to the host computer.

E

Edge - A signal transition from low to high or from high to low.

Edge Triggering - The method of triggering on a low-to-high or high-to-low transition instead of on a low or high voltage threshold.

Expand Bus - The process of displaying the individual signal which make up a bus, without [undefining](#) the group. See [collapse bus](#).

External Clock - A clock signal external to the logic analyzer and usually synchronous with the system under test. See also [acquisition clock](#) and [internal clock](#).

External Clocking - A clock mode in which the sampling of the input signals is synchronous with the external clock signal.

F

Find Pattern - A pattern used to locate a specific data pattern within acquisition memory.

G, H

Highlight - Identification all occurrences of a specific data pattern by changing the background color of the data display at all points where the data pattern exists.

I

Internal Clock - The internal logic analyzer clock used to determine the rate at which the input signals are sampled. See also [acquisition clock](#) and [external clock](#).

J, K, L

Level - Refers to the reference made of a signal as being a *logic* high or low based on the signal's voltage at that instant.

M, N, O, P

Pattern - A set of logic conditions (high, low, rising edge, falling edge either edge or don't care) for each channel of the logic analyzer. Patterns define the criteria for triggering the analyzer, locating data and highlighting data.

Post-Trigger Data - Data that occurred after the trigger event.

Pre-Trigger Data - Data the occurred before the trigger event.

Probing - Refers to controlling the Probe Pilot function of Silicon Explorer which enables the dynamic routing of two internal nodes to two dedicated pins of Actel devices.

Q

Qualifier - See [clock qualifier](#)

R

Radix - The alphanumeric base in which the data is displayed. For example, logic analyzers typically display data in hexadecimal, binary, integer, ASCII, analog, etc.

Resolution - See [sample resolution](#)

Rising Edge - A signal transition from logic low to logic high.

S

Sample Clock - See [acquisition clock](#)

Sample Rate - The speed at which the input signals are sampled, often expressed in *mega-samples per second* (MSa/s). Selecting the proper sample rate is important in ensuring the signals are displayed accurately, and completely. See [Understanding Asynchronous Sampling](#)

Sample Resolution - The interval (in seconds) between samples, determined by the frequency of the sample clock. See [Understanding Asynchronous Sampling](#)

State Display - A display mode in which acquisition data is presented vertically in time as a column of samples.

Synchronous Acquisition - An acquisition mode in which an [external signal](#) is used to clock acquisition data into the analyzer.

T

Timing Display - A display mode in which acquisition data is displayed as horizontally in time as signal waveforms.

Trigger - An event or condition that determines the end of the acquisition cycle. When started, the analyzer continuously acquires data from the systems under test until the trigger occurs. After triggering, the analyzer continues to load data until the post-fill requirement is met. See also [post-trigger data](#) and [pre-trigger data](#).

Trigger Pattern - A trigger pattern is a trigger condition comprised of logic levels and/or edges on one or more channels.

Trigger Position - The location of the trigger event in memory. The trigger can be at the beginning, middle or end of acquisition memory, letting the user view pre and post-trigger data. See also [post-trigger data](#) and [pre-trigger data](#).

U, V

Undefine Bus - The process of un-grouping a channel bus so the individual signals are displayed.

W, X, Y, Z

Waveform Display - See [timing display](#).

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**

From the rest of the world, call **650.318.4460**

Fax, from anywhere in the world, **650.318.8044**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

For Microsemi SoC Products Support, visit <http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support>.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group [home page](http://www.microsemi.com/soc), at www.microsemi.com/soc.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

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