PD70101 / PD70201: IEEE 802.3 af/at Power Over Ethernet PD Controller

PRELIMINARY DATA SHEET

GENERAL DESCRIPTION

The PD70101 and PD70201 are integrated Powered Device Interface and PWM controllers for a DC-DC converter used in IEEE802.3af and IEEE802.3at applications. The PD70101 can be used for IEEE802.3af or IEEE802.3at Type 1 applications, while the PD70201 can also be used in IEEE802.3at Type 2 applications.

A single PD70201 can be used in 4-pair applications which consumes up to 47.7W.

These devices have a number of features designed to improve efficiency and reliability:

Detection and Classification: The front end interface includes detection and classification circuitry. The detection signature resistor is disconnected upon completion of the detection phase. The system then begins the classification phase. Classification can be configured for Classes 0 to 4 via an external resistor. The PD70201 includes a two-events classification identification circuit which generates a flag to inform the PD application whether the Power Source Equipment (PSE) is Type 1 or Type 2.

Capacitor: A current limited internal MOSFET switch charges the input capacitor of the DC-DC converter. This capacitor is discharged in a timely manner when the input power is removed.

10V gate drivers: The PWM DC-DC controller has two built-in 10V gate drivers targeted for flyback direct buck or forward converter with secondary synchronous rectifier flyback. The 10V gate drivers lower external Power MOSFET power loss while offering a wider MOSFET selection.

Peak current mode control: The DC-DC converter employs peak current mode control for better line and load step response. The switching frequency can be set from 100 kHz to 500 kHz, enabling a size and efficiency trade off.

Maximum duty cycle is limited to 50% to reduce the power MOSFET switch voltage to two times the input voltage; a 150V rated MOSFET can be used for the primary side switch. The secondary synchronous MOSFET voltage rating depends on the output voltage and can be higher or lower than the primary side MOSFET switch.

Soft-start circuit: The devices include a soft-start circuit to control the output voltage rise time (user settable) at start up, and to limit the inrush current. An integrated start-up bias circuit powers the DC-DC controller, until the device starts up by the voltage generated by the bootstrap circuit.

Low Voltage Protection Warning and Monitoring: Dual Under Voltage Lock Out (UVLO), which monitors both the PoE Port Input Voltage and VCC, ensures reliable operation during any system disturbances. The PoE port UVLO has a programmable threshold and hysteresis to enable tailoring to the desired turn on and turn off voltage. Alternatively, the controller offers Power Fail Warning (PFW) to alert the host processor if PoE power removal occurs.

An internal current sense amplifier with a Kelvin connection allows the use of an extremely low resistor to measure the current sense threshold voltage (100 mV) which optimizes efficiency.

Low Power Mode operation is provided to improve efficiency under light loads such as when the PD is in standby. The user can define at what power level the unit enters low power mode by means of a single resistor value.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: http://www.microsemi.com

KEY FEATURES

- IEEE802.3af and IEEE802.3at compliant
- Support for 4-pair applications of up to 47.7W with a single IC
- Two-events classification identification with a Level Signal indicating Type 1 or Type 2 PSE
- Less than 10 µA (typ) offset current during detection
- Signature resistor is disconnected upon detection
- Programmable classification setting with a single resistor
- Integrated 0.6 Ohm isolating MOSFET switch with inrush current limit
- Power Off DC-DC input capacitor discharge
- 100 kHz to 500 kHz adjustable DC-DC switching frequency
- DC-DC frequency can be synchronized to external clock
- Supports low power mode operation for higher efficiency 50% maximum duty cycle
- Soft-start circuit to control the output voltage rise time
- Support efficient synchronous rectification
- PoE Port Input UVLO/PFW with programmable threshold and hysteresis
- Internal differential amplifier simplifying non-isolated step down converter
- Over load and short circuit protection
- RoHS compliant & Pb-Free

APPLICATIONS

- IEEE802.3at and IEEE802.3af powered devices such as IP phones, WLAN access points and network cameras.
- 48 V input telcom/networks hot swappable power supply

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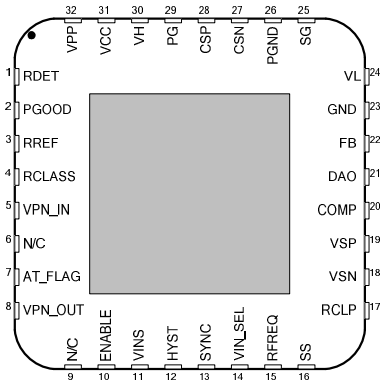
PRELIMINARY DATA SHEET

ABSOLUTE MAXIMUM RATINGS

VPP, RDET, VPN_OUT, RREF, RCLASS ..... -0.3V to 74V_{DC}
PGOOD, AT_FLAG (with respect to VPN_OUT) ..... -0.3V to 74V_{DC}
VCC (with respect to GND) ..... -0.3V to 40V_{DC}
PG, SG (with respect to PGND) ..... -0.3V to 20V_{DC}
VL (with respect to GND)..... -0.3V to 6V_{DC}
VH (with respect to VCC) ..... -0.3V to VCC - 6V_{DC}
All Other Pins (with respect to GND)..... -0.3V to VL + 0.3V_{DC}
Maximum Operating Junction Temperature ..... 150°C
Operating Ambient Temperature ..... -40°C to 85°C
Storage Temperature Range..... -65°C to 150°C
Peak Package Solder Reflow Temp (40 seconds max exposure) ..... 260°C

Note: Exceeding these ratings could cause damage to the device. Unless otherwise specified all voltages are with respect to VPN_IN. Currents are positive into and negative out of specified terminal.

PACKAGE PIN OUT



QFN PACKAGE
(Top View)

RoHS / Pb-free 100% matte Tin Pin Finish

PACKAGE ORDER INFO

T_A (°C)	LD	5x5 Plastic QFN 32 pin
	RoHS Compliant / Pb-free	
-40 to 85	PD70101ILQ (IEEE802.3af compliant) PD70201ILQ (IEEE802.3at compliant)	

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. PD70101ILQ-TR)

THERMAL DATA

23°C/W

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C except where otherwise noted with the following test conditions: VPP= 37V to 57V; VCC = 7V to 20V; V_{EN} = HIGH, f_s = 250 kHz. Production tests performed at 25°C.

Parameter	Symbol	Test Conditions / Comment	PD70101 & PD70201 CONTROLLER			Units
			Min	Type	Max	
PD Interface						
POWER SUPPLY						
Input Voltage	VPP	Supports Full IEEE802.3 functionality	0	55	57	V
DETECTION MODE						
Detection is connected. At this voltage range RDET must be on.	DET_{RANGE}	Measured between VPP and VPN_IN	2.5		10.1	V
Detection Switch ON Resistance PD-detection	RDET-on	2.5V ≤ VPP TO VPN_IN ≤ 10.1V Measured between RDET and VPN_IN			50	Ω
Detection is disconnected	RDET-off	Measured between VPP and VPN_IN	10.1		12.8	V
Detection switch OFF resistance	RDET-off	12.8V ≤ VPP to VPN_IN ≤ 57.0V Measured between RDET and VPN_IN	2.0			MΩ
Input offset current	I_{OFFSET}	2.5V to 10.1V -40°C ≤ T_J ≤ 85°C			16	µA
	I_{OFFSET}	2.5V to 10.1V -40°C ≤ T_J ≤ 55°C			10	µA
RDET reconnection level, VPP falling	V_{RDET}-on	Measured between VPP and VPN_IN	2.45	3.0	4.85	V
CLASSIFICATION MODE						
Classification current source, turn ON threshold range measured at V_{CC}	V_{TH}-low-on	Turn on for any I_{CLASS} while V_{CC} increases	11.1		13.5	V
Classification disconnection minimum hysteresis voltage.	V_{HST}	Hysteresis between V_{TH}-low-on and V_{TH}-low-off	1			V
Classification current source, turn OFF threshold range measured at V_{PP}	V_{TH}-high-off	Turn off while V_{PP} increases	20.9		23.9	V
Current limit threshold	I_{CLASS}-LIM		50.0	55.5	60.0	mA
Input current I_{PP} when classification function is disabled	I_{CLASS}-DIS	Class 0 RCLASS = Disconnect			3.0	mA
Input current I_{PP} when classification function is enabled	I_{CLASS}-EN	Class 1 RCLASS = 113Ω±1%	9.50	10.5	11.5	mA
		Class 2 RCLASS = 64.9 Ω±1%	17.5	18.5	19.5	mA

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Parameter	Symbol	Test Conditions / Comment	PD70101 & PD70201 CONTROLLER			Units
			Min	Type	Max	
		Class 3 RCLASS = 43.2 Ω±1%	26.5	28.0	29.5	mA
		Class 4 RCLASS = 30.9 Ω±1%	38.0	40.0	42.0	mA
MARK						
Mark, working range	V_{MARK}	When voltage decrease Measured between VPP to VPN_IN	4.9		10.1	V
Mark Current	I_{MARK}	Chip current	0.25		4	mA
ISOLATION SWITCH						
Isolation Switch MOSFET switches from off to $I_{LIM-LOW}$	$V_{SW-START}$		36		42	V
Isolation Switch MOSFET switched off	V_{SW-OFF}		31		34	V
Startup current limit, I_{LIM}	$I_{LIM-LOW}$		130	240	320	mA
VPN_IN to VPN_OUT Threshold voltage for $I_{LIM-LOW}$ to $I_{LIM-HIGH}$ switchover	V_{DIFF}	When VPN_IN to VPN_OUT ≤ V_{DIFF}, Isolating switch switches over from $I_{LIM-LOW}$ to $I_{LIM-HIGH}$.			0.7	V
Over current protection limit current	OCP		1500	1800	2000	mA
Continuous operation load	I_{LOAD}	Isolating switch at $I_{LIM-HIGH}$ PD70101 PD70201		 350 600	 450 1123	 mA mA
Continuous operation total RDS_{ON}	$SW-RDS_{ON}$	Total resistance between VPN_IN and VPN_OUT Isolating switch at $I_{LIM-HIGH}$			0.6	Ω
DC/DC CAPACITOR DISCHARGER						
DC/DC input capacitance		For reference only Guaranteed by design (not tested on production)		220		µF
Discharge current.		1.5 ≤ VPP to VPN_OUT ≤ 32v	22.8			mA
Discharge time for full discharge	$T_{DSCFULL}$	V_{CC} < UVLO threshold Guaranteed by design (not tested on production)			500	ms
AT_FLAG						
Output low voltage		I_{OL} = 5mA			0.4	V
Leakage current		V_{ATFLAG} = 57V			1	µA

Parameter	Symbol	Test Conditions / Comment	PD70101 & PD70201 CONTROLLER			Units
			Min	Type	Max	
PGOOD						
Output low voltage		I_{OL} = 5mA			0.4	V
Leakage current		V_{PGOOD} = 57V			1	µA
PD INTERFACE THERMAL SHUTDOWN						
Thermal Shutdown Temperature[1]			180	200	220	°C
DC-DC Controller						
VCC						
Operating Input Voltage	VCC		7		20	V
Input Current	I_{VCC}	VCC< VCC_UVLO or ENABLE = Low.			200	µA
		VCC >VCC_UVLO and ENABLE = High, No Load on PG, SG, VL, and F_{SW} = 500kHz.			3	mA
VCC UVLO Rising Threshold	VCC_UVLO	VCC rise time (10% to 90%) ≥ 0.5 ms	8.85	9.15	9.45	V
VCC UVLO Falling Threshold	VCC_UVLO	VCC fall time (90% to 10%) ≥ 5 ms	7	7.3	7.6	V
POE PORT INPUT UVLO/PFW						
UVLO/PFW Threshold	VINS	Rising or falling (via external resistor divider from VPP to GND). Includes +/- 5mV of input offset.	1.171	1.200	1.229	V
VINS Input Current			-0.1		+0.1	µA
HYST/PFW Output High Voltage	HYST-V_{OH}	I_{SOURCE} = 1mA	2.8			V
HYST/PFW Output Low Voltage	HYST-V_{OL}	I_{SINK} = 5mA			0.4	V
INTERNAL LDOs						
+5 V Internal Linear Regulator	VL	0 < IL < 5mA, Not including internal consumption	4.75	5	5.25	V
-5 V Internal Linear Regulator	VH	Reference to VCC; for Internal use only		-5		V
SOFT-START						
Soft-start Charging Current[2]	I_{SS_CHG}	R_{FREQ}=33.2kΩ; $V_{SOFTSTART}$ = 0.5V	32	36	40	µA
Soft-start Discharging Current	I_{SS_DIS}	$V_{SOFTSTART}$ = 0.5V; percent of I_{SS_CHG}		10		%
Soft-start Completion Threshold[1]	V_{SS}	Percentage of 1.2V Reference	90		95	%
Soft-start Discharge (by current source) Completion Threshold[1]	V_{SS}			50		mV
Soft-start Discharge FET On Resistance				50		Ω
Soft-start Discharge FET On Time[1]		Specified as switching frequency clock cycles		32		cyc

Parameter	Symbol	Test Conditions / Comment	PD70101 & PD70201 CONTROLLER			Units
			Min	Type	Max	
SWITCHING FREQUENCY AND SYNCHRONIZATION						
Switching Frequency Adjust Range	F_{FREQ}		100		500	kHz
Switching Frequency Set Point Accuracy[3]	F_{FREQ}	R_{FREQ} = 33.2k (V_{RFREQ} = 1.2V). Note: Oscillator frequency is 2x the converter switching frequency.	270	300	330	kHz
Synchronization Frequency Range	F_{SYNC}	F_{SYNC} greater than 2x the converter switching frequency.	200		1000	kHz
Synchronization Voltage High Threshold	V_{SYNC}		2.4		5	V
Synchronization Voltage Low Threshold	V_{SYNC}				0.8	V
Synchronization Minimum Pulse Width	PW_{SYNC}		100		200	ns
Synchronization Input Current	I_{SYNC}		-1		+1	µA
ERROR AMPLIFIER						
DC Open Loop Gain[1]		R_{LOAD} = 100k	70	100		dB
Unity gain bandwidth[1]	AV_{UGBW}	C_{LOAD} = 10pF	2	5		MHz
Output Sourcing/Sink Current		0.2V ≤ V_{COMP} ≤ 1.3V	200		500	µA
Input Common Mode Range			0		2	V
Feedback Voltage Accuracy	V_{FB}	COMP shorted to FB.	1.171	1.200	1.229	V
FB Pin Input Current	I_{FB}		-50		50	nA
Output High Clamp	V_{COMP}		1.3	1.4	1.5	V
PWM COMPARATOR						
Input Offset			-10		10	mV
RCLP Voltage range	V_{RCLP}		0		1	V
LOW POWER MODE (SKIP PULSE MODE)						
Low Power Skip Mode Threshold[1,4]		V_{COMP} Rising (as percent of V_{RCLP}).		95		%
		V_{COMP} Falling (as percent of V_{RCLP}).		90		%

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Parameter	Symbol	Test Conditions / Comment	PD70101 & PD70201 CONTROLLER			Units
			Min	Type	Max	
CURRENT SENSE AMPLIFIER AND CURRENT LIMIT						
Gain		Measure at DC	9.5	10	10.5	V/V
Input Common Mode Range			0		2.0	V
Output Rise/Fall time		Measured from 10% to 90%			75	ns
Blanking Time			50		100	ns
Current Limit Threshold	V_{ILIM_TH}	Threshold where PWM pulses are truncated.	1.1	1.2	1.3	V
Current Max Threshold	V_{IMAX_TH}	Threshold where device goes into hiccup.	1..7	1.8	1.9	v
DIFFERENTIAL AMPLIFIER						
Gain		Measured at DC	6.86	7.0	7.14	V/V
Unity Gain Bandwidth[1]				5		MHz
Common Mode Range			0		3.5	V
Input Offset Voltage			-5		+5	mV
Input Bias Current			-1		+1	µA
OUTPUT DRIVERS						
Primary Gate (PG) High On Resistance	PG Rds_{ONH}			10		Ω
Primary Gate (PG) Low On Resistance	PG Rds_{ONL}			5		Ω
Secondary Gate (SG) High On Resistance	SG Rds_{ONH}			10		Ω
Secondary Gate (PG) Low On Resistance	SG Rds_{ONL}			10		Ω
Dead Time – PG low to SG high or SG low to PG high	T_{DEAD}	Measured between 10% levels. C_{LOAD} on PG and SG = 1000pF		110		ns
PG Minimum On Time					100	ns
PG Maximum Duty Cycle			46		50	%
LOGIC (VINS_SEL PIN AND ENABLE PIN)						
Logic High Threshold			2.0			V
Logic Low Threshold					0.8	V

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Parameter	Symbol	Test Conditions / Comment	PD70101 & PD70201 CONTROLLER			Units
			Min	Type	Max	
Input Current			-1		1	µA
PWM CONTROLLER THERMAL SHUT DOWN						
Thermal Shutdown Threshold[1]			150	157	165	°C
Threshold Hysteresis[1]				15	30	

Notes:

1) Guaranteed by design. Not tested during production.
2) Soft Start Charge Current Equation: $I_{ss\_chg} = 1.2V/R_{FREQ}$
3) Switching Frequency Equation: $Freq = 10x10^9/R_{FREQ}$
4) Low Power Mode Clamp Equation: $V_{CLAMP} = 1.2 * (R_{RCLP}/R_{FREQ})$

PD70101/PD70201 FUNCTIONAL BLOCK DIAGRAM

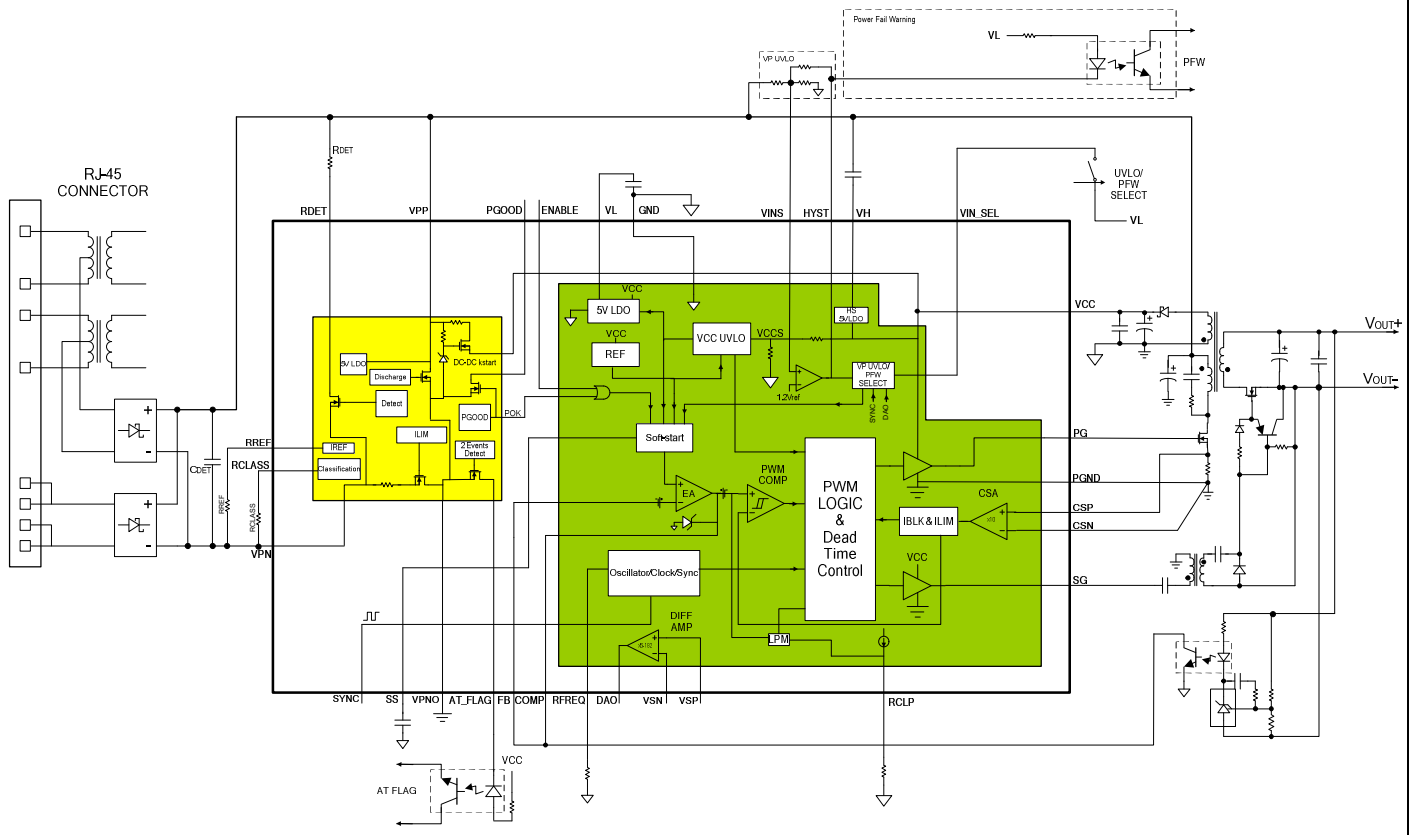

Figure 1: PD70101/PD70201 Functional Block Diagram (PD70201 shown)

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PD70101/PD70201 PIN DESCRIPTION			
Pin	**PD70101 Pin Name**	**PD70201 Pin Name**	**Description**
1	RDET	RDET	Valid Detection Resistor: Connect a 24.9kΩ, 1% resistor from this pin to VPP
2	PGOOD	PGOOD	Open Drain Output (active low): This flag is generated to indicate the power rails (VPN_OUT) are ready
3	RREF	RREF	Bias current resistor for the PD Interface.
4	RCLASS	RCLASS	Power Classification Setting: Connect external class resistor between this pin and VPN_IN.
5	VPN_IN	VPN_IN	VPort Negative Input: Connected to the isolating switch input N-channel MOSFET source.
6	N/C	N/C	Not Used
7	N/C	AT_FLAG	Open Drain Output (active low): This flag indicates if the chip detects an IEEE 802.3at compliant PSE.
8	VPN_OUT	VPN_OUT	VPort Negative Output: Connected to the isolating switch output. N-channel MOSFET Drain.
9	N/C	N/C	Not Used
10	ENABLE	ENABLE	Logic level Enable input for DC-DC controller. Pulling this pin to VL turns on the DC-DC controller. This allows the DC-DC controller to be turned on without power to the PD interface.
11	VINS	VINS	VPP input voltage sensing for UVLO comparator. Connect to an external resistor divider from VPP to GND. Threshold is 1.2V reference.
12	HYST	HYST	Output of the VINS/UVLO comparator. This pin is used for VPP UVLO hysteresis programming, or as the Power Fail Warning flag.
13	SYNC	SYNC	External Clock synchronization for the DC-DC controller. Connect an external clock as defined in the EC table to this pin to synchronize the DC-DC converter switching frequency to this clock. PG rising edge is synchronize with the clock rising edge.
14	VINS_SEL	VINS_SEL	UVLO/PFW select Logic Input. Internally pulled low for VINS Power Fail Warning (PFW) flag. Pull to logic high to use as VINS UVLO
15	RFREQ	RFREQ	DC-DC Switching Frequency Setting. Connect a resistor from this pin to GND to set the switching frequency
16	SS	SS	Soft-start: Connect a capacitor from this pin to GND to set the soft-start time of the DC-DC converter. This capacitor is charged with an internal current source to 1.2V
17	RCLP	RCLP	Low Power Mode Clamp. Connect a resistor from this pin to GND to program the LPM clampimg voltage or connect this pin to GND to disable LPM.
18	VSN	VSN	Differential Amplifier's negative input. Connect this to the junction of a resistor divider from Vo- to GND for the Direct Buck converter application
19	VSP	VSP	Differential Amplifier's positive input. Connect this to the junction of a resistor divider from Vo+ to GND for the Direct Buck converter application
20	COMP	COMP	Error Amplifier Output. Short to FB pin when driven directly with an optoisolator for Isolated DC-DC Converter. Connect to FB via RC compensation networks for Non-Isolated Direct Buck Converter.

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PD70101/PD70201 PIN DESCRIPTION			
Pin	**PD70101 Pin Name**	**PD70201 Pin Name**	**Description**
21	DAO	DAO	Differential Amplifier Output. Connect to FB (externally) via a 1.2kΩ resistor for Non-Isolated Direct Buck Converter.
22	FB	FB	Inverting Input of the Error Amplifier. Connect to SS for Isolated DC-DC. Connect to RC compensation networks for Non-isolated DC-DC
23	GND	GND	This is Analog GND. Connect to a local AGND plane. Soft-start capacitor and the frequency setting resistor return to this local GND plane.
24	VL	VL	5V (GND reference) internal LDO Output. Connect a 1µF or higher ceramic cap from VL to GND.
25	SG	SG	Secondary Gate Driver. Output is the compliment of PG output. Leave open (NC) if not used. SG is low when in Low Power Skip Mode.
26	PGND	PGND	This is the Power Ground. Connect to a local PGND plane. Input, VCC decoupling capacitors, PG and SG drivers, Primary current sense resistor return to this PGND
27	CSN	CSN	Negative Input of the Current Sense Amplifier. Kelvin connect to the PGND side of the primary current sense resistor
28	CSP	CSP	Negative Input of the Current Sense Amplifier. Kelvin connect to the Non-PGND side of the primary current sense resistor
29	PG	PG	Primary Gate Driver. Connect to the gate of the primary side Power MOSFET, directly or via a resistor
30	VH	VH	5V High side (VCC reference) internal LDO Output. Connect a 0.1µF or higher ceramic cap from VH to VCC.
31	VCC	VCC	Input Supply to the DC-DC Controller. Connect a 4.7µF or higher ceramic capacitor from this pin to PGND. Alternately an parallel combination of 1µF ceramic and an greater than 10µF electrolytic capacitor can be used.
32	VPP	VPP	This is the positive terminal of the POE input port. Connect to the positive terminal of the input bridges at the C_{DET} positive side
EP	Exposed Pad	Exposed Pad	Thermal Pad; electrically connected to VPN_IN. For proper thermal management should be tied to a large copper fill or plane that is electrically connected to VPN_IN.

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TYPICAL APPLICATIONS

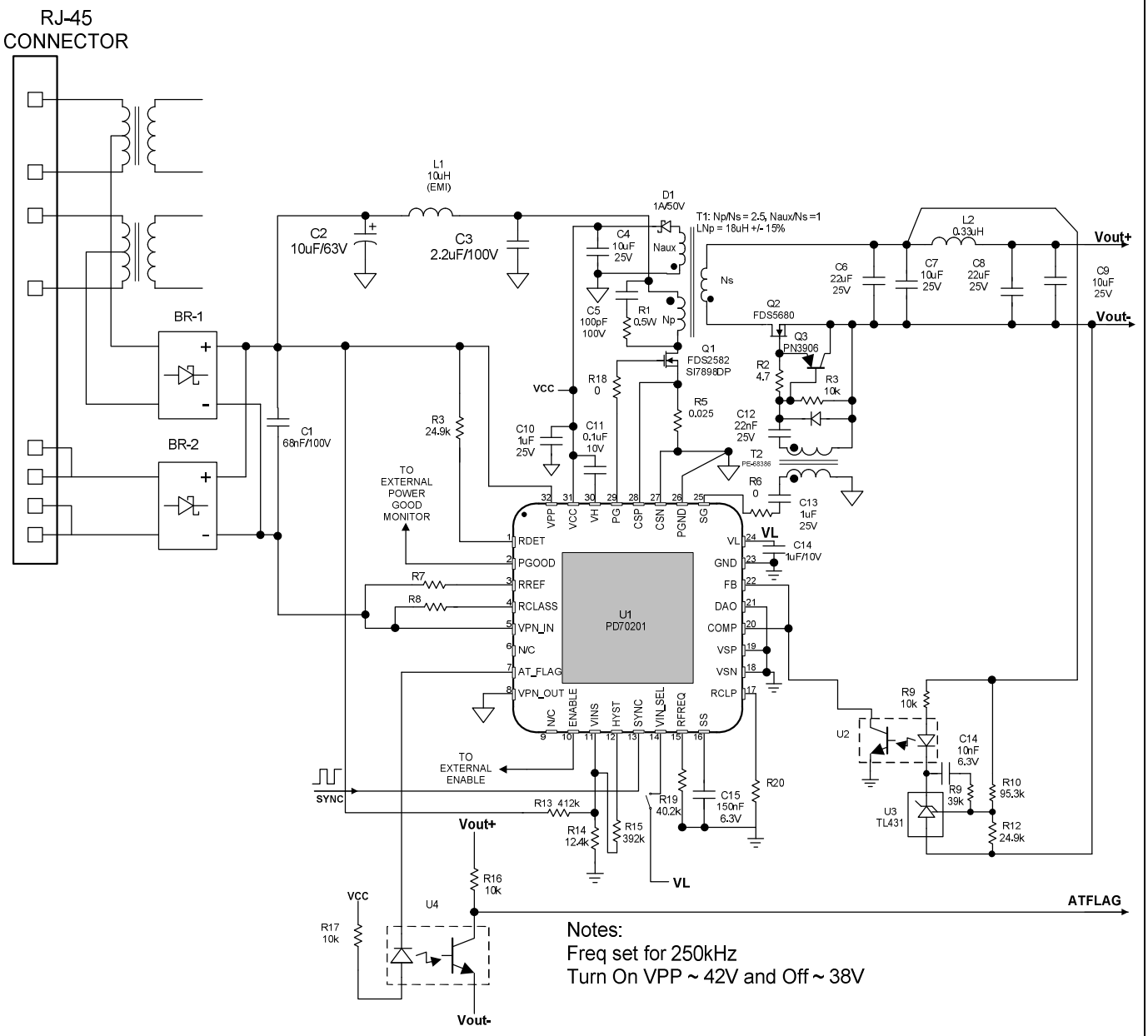

Figure 2: 12V/2A Output Isolated Fly-back with Secondary Synchronous Rectification

TYPICAL APPLICATIONS

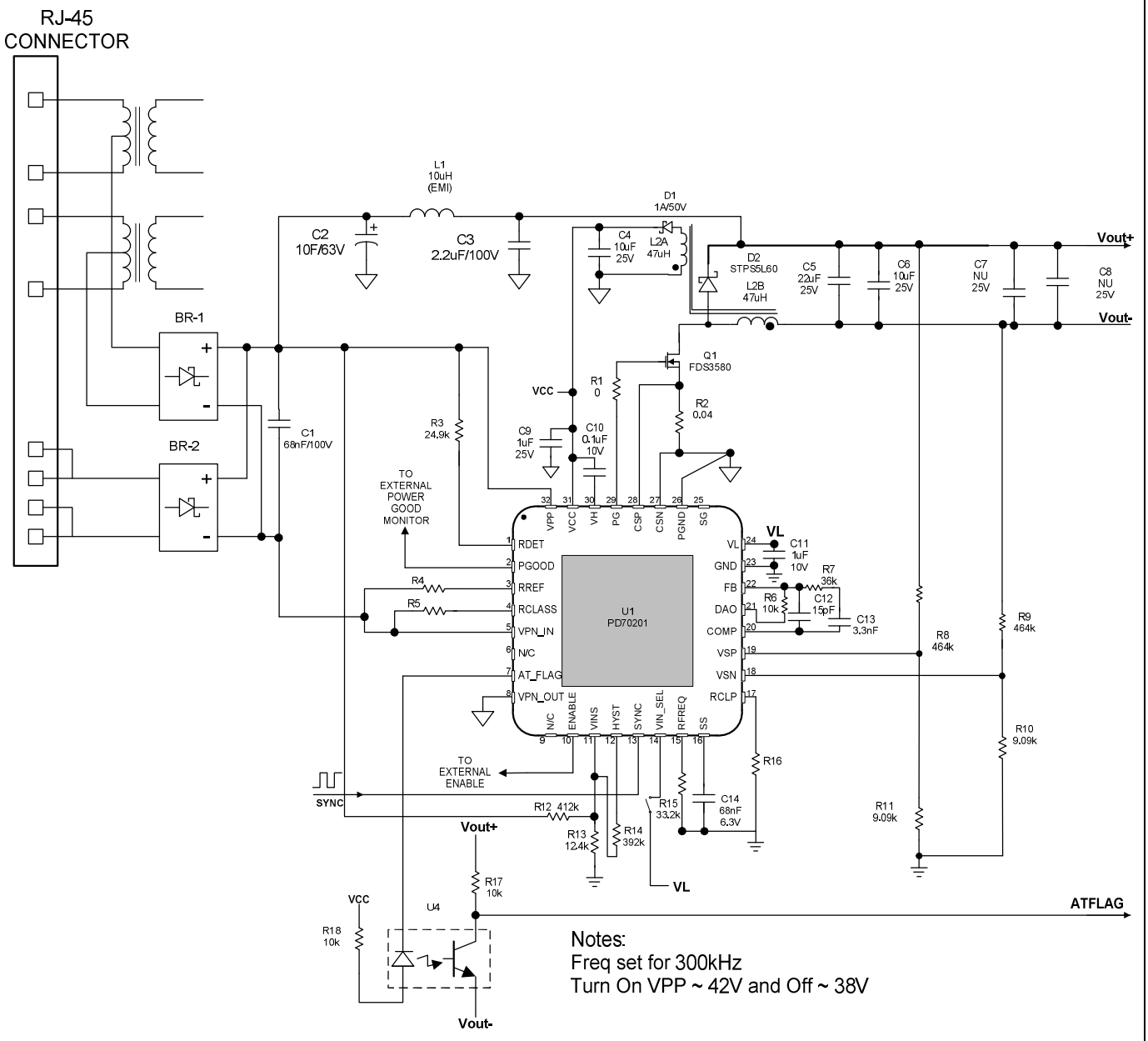

Figure 3: 12V/2.1A Output Non-Isolated Direct Buck Application

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THEORY OF OPERATION

DETAIL DESCRIPTION

PD70101/PD70201 IC integrates IEEE 802.3af/at compliant PD Front-End functions including Detection, Physical Layer Classification, Two-Events Classification (PD70201 only), Power Good, Soft Start Current Limiting, Over-Current Protection, and Bulk Capacitor Discharge with a PWM controller. The integrated PWM controller function provides a PWM controller solution with a minimum requirement of external components.

DETECTION

IEEE 802.3af/at compliant detection is provided by means of a 24.9KΩ resistor connected between VPP and RDET pin. RDET pin is connected to VPN_IN via an open drain MOSFET with a maximum specified RDS_{ON} of 50Ω. Internal logic monitors VPP to VPN_IN and connects the RDET pin to VPN_IN when the rising VPP to VPN_IN voltage is between 1.1V and 10.1V. When rising VPP to VPN_IN voltages exceed 10.1V, the MOSFET is switched off. Once above 10.1V, falling VPP to VPN_IN voltage between 2.45V and 4.85V will reconnect RDET pin to VPN_IN.

PHYSICAL LAYER CLASSIFICATION

Physical Layer (hardware) Classification per IEEE 802.3af/at is generated via a regulated reference voltage of 1.2V, switched onto the RCLASS pin. Internal logic monitors the VPP to VPN_IN voltage and connects the 1.2V reference to RCLASS pin at a rising VPP to VPN_IN voltage threshold between 11.1V and 13.5V. Once VPP to VPN_IN as exceeded the rising threshold, there is a 1V minimum hysteresis between the VPP rising (turn-on) threshold and the VPP falling (turn-off) threshold.

The 1.2V reference stays connected to the RCLASS pin until the VPP to VPN_IN rising voltage exceeds the upper turn-off threshold of 20.9V to 23.9V. The 1.2V reference voltage is disconnected from the RCLASS pin at VPP to VPN_IN voltages above the upper threshold.

Classification current signature is provided via a resistor connected between RCLASS pin and VPN_IN. The classification current is therefore the current drawn by the PD70101/PD70201 IC during the classification phase, and is simply the 1.2V reference voltage divided by the RCLASS resistor value. The maximum current available at the RCLASS pin is current limited to 55mA (typical).

TWO-EVENTS DETECTION AND AT FLAG

The PD70201 IC provides IEEE 802.3at Type 2 compliant detection of the “Two Events Classification Signature”, and generation of the AT flag. This feature is available on the PD70201 IC only.

Simply put, the “Two Events Classification Signature” is a mean by which an IEEE 802.3at Type 2 Power Source can inform a compliant Power Device (PD) that it is AT Type 2 compliant, and as such is capable of providing AT Type 2 power levels.

The Power Source communicates with the Type 2 compliant signature by toggling the VPP to VPN_IN voltage twice (2 “events”) during the Physical Layer Classification phase. The VPP to VPN_IN voltage is toggled from the Physical Layer Classification’s voltage level (13.5V to 20.9V) down to a voltage “Mark” level. Voltage “Mark” level is specified as a VPP to VPN_IN voltage of 4.9V to 10.1V.

PD70201 IC recognizes a VPP to VPN_IN falling edge from Classification level to Mark level as being one event of the Two-Events Signature. If two such falling edges are detected, PD70201 will assert AT flag by means of an open drain MOSFET connected between AT_FLAG pin and VPN_OUT.

AT_FLAG pin is active low; a low impedance state between AT_FLAG and VPN_OUT indicates a valid Two-Events Classification Signature was received, and the Power Source is AT Type 2 compliant.

AT_FLAG MOSFET is capable of 5mA of current and can be pulled up to VPP.

SOFT START AND INRUSH CURRENT PROTECTION

PD70101/PD70201 IC contains an internal isolation switch, that provides ground isolation between Power Source and PD application during Detection and Classification phases. The isolation switch is a N-channel MOSFET, wired in a common source configuration where the MOSFET’s Source is connected to Power Source ground at VPN_IN, and the MOSFET’s Drain is connected to application’s primary ground at VPN_OUT.

THEORY OF OPERATION

Internal logic monitors VPP to VPN_IN voltage and keeps the MOSFET in a high impedance state until VPP to VPN_IN voltage reaches turn-on threshold of 36V to 42V. Once VPP to VPN_IN voltage exceeds this threshold, the MOSFET is switched into one of two modes.

Mode into which the MOSFET is switched is determined by the voltage developed across the MOSFET, or put another way, the VPN_OUT to VPN_IN differential voltage. Two modes are defined below:

Isolation Switch Modes

VPN_OUT to VPN_IN	Mode	Description
≥ 0.7V	Soft Start Mode	Limits VPN_OUT current to 240mA (typical)
≤ 0.7V	Normal Operating Mode	Limits VPN_OUT current to 1.8A (typical)

By controlling the MOSFET current based on VPN_OUT to VPN_IN voltage, inrush currents generated by fully discharged bulk capacitors can be limited. This method limits current to a maximum of 350mA, compliant with IEEE 802.3af/at specification.

Soft Start current limiting is required to reduce occurrences of voltage sag at the PD input during device power-up. A comparison is shown in Figure 3.

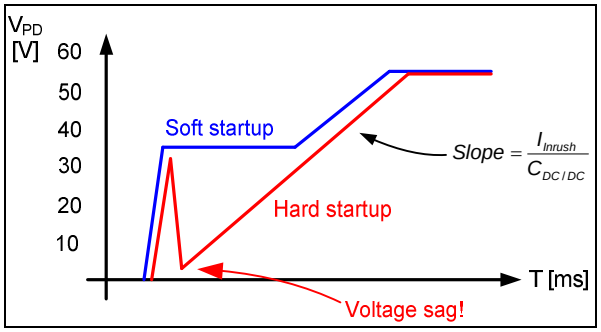

Figure 3. Comparison of input voltages without Soft Start (Hard startup), and with Soft Start (Soft startup).

Once bulk capacitance has charged up to a point where VPN_OUT to VPN_IN differential voltage is less than 0.7V, the isolation MOSFET is switched into normal operating mode with MOSFET current limit set at 1.8A (typical), to provide overcurrent protection.

PD70101 and PD70201 ICs are different in their respective isolation MOSFET's continuous current handling capability:

PD70101: 450mA (max.)

PD70201: 1123mA (max.)

An adequate heatsink for the PD70101/PD70201 IC's exposed pad must be provided to achieve these current levels without damaging the IC. A large, heavy copper fill area and/or a heavy ground plane with Thermal Vias is recommended.

Internal logic monitoring VPP to VPN_IN will place the isolation switch MOSFET in a high impedance state if voltage between VPP and VPN_IN drops below 31V to 34V.

OVER-CURRENT PROTECTION

An over-current protection is provided on the PD70101/PD70201 IC using the Isolation Switch MOSFET, which limits the VPN_OUT current to 1.8A during normal operation. See previous description of Soft Start.

POWER GOOD

During Soft Start mode, the PD70101/PD70201 IC monitors VPN_OUT to VPN_IN differential voltage. When this voltage is less than 0.7V (max.), the IC enters normal operation mode and the isolation switch current limit is increased to 1.8A (typical). At this same 0.7V (max.) threshold the Power Good signal is asserted by means of an open drain MOSFET between PGOOD and VPN_OUT.

PGOOD pin is active low; a low impedance state between PGOOD and VPN_OUT indicates the Soft Start mode has finished and the isolation switch has transitioned into normal operating mode.

PGOOD MOSFET can handle current of 5mA and can be pulled up to VPP.

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THEORY OF OPERATION

START-UP SUPPLY

PD70101/PD70201 IC provides a 10.5V (typical) regulated output used as a start-up supply for the integrated DC/DC controller when V_{CC} is provided via a bootstrap winding. This regulated supply is available at VCC pin, and is referenced to VPN_OUT pin. The VCC start-up supply is current-limited at 10mA (min.).

For stability, the start-up regulator requires a minimum of 4.7µF ceramic capacitor connected directly between VCC and PGND pins (most applications will connect PGND to VPN_OUT).

PD INTERFACE THERMAL PROTECTION

Both PD70101 and PD70201 IC contain temperature sensors which individually monitor both the isolation MOSFET and the Classification Current Source for over temperature conditions. In case of an overtemperature condition, the sensor will activate protection circuitry which will disconnect its respective monitored function.

BULK CAPACITOR DISCHARGE

The bulk capacitor discharge circuitry eliminates the need to place a diode in series with the VPP line to prevent an application's bulk capacitance from discharging through the detection resistor and the isolation switch MOSFET's body diode. Discharge current through the detection resistor can cause failure of the detection signature in cases where a PD is connected and the bulk capacitance is not fully discharged.

During normal operation, PD70101/PD70201 IC continuously monitors voltage at VPP to VPN_IN. Should VPP to VPN_IN voltage fall below isolation switch turn-off threshold (31V to 34V), isolation switch MOSFET is immediately placed in a high-impedance state. At this point the internal logic monitors the voltage at VPP to VPN_OUT. If VPP to VPN_OUT voltage is between 1.5V to 32V, a 23mA (min.) constant current source is connected across the VPP and VPN_OUT pins. This constant current source provides bulk capacitor discharge.

A 220µF bulk capacitance can be discharged from 32V to 1.5V in a maximum period of 292ms.

DC-DC START-UP

The DC-DC controller starts up when it receives the PGOOD high signal from the Front End, or ENABLE goes high provided that VCC UVLO have passed. When the PGOOD signal or ENABLE goes high, the start up sequence begins with ramping up the SS pin from GND to 1.2V. For isolated applications the output voltage may reach the maximum level before the SS reaches 1.2V, depending on the output loading condition. In applications with lighter loads, the output reaches regulation level sooner than in heavy loads, as in this mode the SS voltage directly controls the peak inductor current; hence the energy is delivered to the load. The external secondary error amplifier regulates the output voltage and controls the peak inductor current via the opto-coupler across the isolation barrier. For non-isolated applications, because the internal error amplifier is used to close the regulation loop, the output reaches the regulation level when SS reaches 1.2V.

An additional internal offset is added to the FB to ensure that COMP does not reach its upper limit because of amplifier input offset. This offset is removed (slowly to avoid overshoot) when the SS ramp is complete.

Low Power Mode (refer to Low Power Mode Operation) is not supported during SS ramp as it is not necessary. In addition, over current and short circuit protection functions differently during, and after the SS process. Refer to the "Current Limit and Short Circuit Protection" section below.

CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

During SS ramping up if the current limit trips, both PG and SG go low and stay low for 16 clock cycles. After this time, the PG and SG try again. If the current limit trips again, the 16 clock cycles repeats until the SS ramp is complete. After SS ramp is completed (VSS ≈ 1.08V), the current limit trip will set a "four consecutive event trip counter", with no skip in between. If there is a trip during four consecutive cycles with current limit, the controller enters hiccup mode by discharging the SS capacitor with a constant current that equals 10% of the charging current during

THEORY OF OPERATION

This discharge continues until VSS = 50 mV where an internal ~50Ω MOSFET connected to SS turns on for 25 clock cycles to ensure the SS capacitor fully discharges to GND before ramping back up and restart. The converter will exit the hiccup mode when the over current condition is removed or the four consecutive event counter has been reset. If the over current condition lasts less than four consecutive cycles, the four event counter is reset to start the recount again.

LOW POWER MODE OPERATION

The devices offer a pulse skipping operation for light load condition, referred as Low Power Mode (LPM), to improve the efficiency of light load operation by reducing the power dissipation especially in high frequency switching. Using an external resistor from RCLP pin to GND, the user can program the output power when the unit enters pulse skipping.

Pulse skipping mode is disabled until SS ramp is completed, regardless of the LPM status.

INPUT (VPP &VCC) UNDER VOLTAGE LOCK OUT

The PD interface circuit offers a PGOOD signal that can be used to start the DC-DC converter; however the threshold of the PGOOD is fixed at VPNO-VPNI ≤ 0.7V. This may not fit all possible applications. Therefore the devices offers an option to have a programmable UVLO which is tied to level of VPP-VPNO, plus a programmable hysteresis. The voltage developed across a simple resistor divider is sensed at VINS, and will enable/disable the PWM controller at a nominal 1.2V threshold. A third resistor connected between VINS and HYST pins allows programmable hysteresis. This feature enables the end user to tailor to any desired systems application's requirement for turn on and turn off time. In addition to the VPP sensing for UVLO, the devices also have VCC UVLO to ensure that the PWM controller is always properly powered during operation. These features provide robust solutions under various systems disturbances.

POWER FAIL WARNING

A Power Fail Warning feature is also offered as an option in lieu of VPP UVLO, to fit applications that require PFW more than VPP UVLO. The PFW uses the same resistor-divider connected to VINS to sense the input voltage (VPP). The nominal 1.2V threshold level is set by the user at a point above the VPP voltage level where DC-DC output voltage drop out occurs due to maximum duty cycle limit. This warning lets the system know in advance before the output starts to drop.

As with the VPP UVLO function, hysteresis is controlled by a resistor connected between the HYST and VINS pins.

The warning time depends on the output power, conversion efficiency, the input capacitor and the detection threshold setting relative to the input drop out voltage meaning the difference between the VPP setting threshold and the drop out voltage ($VPP_{\_THRESHOLD} - V_{DROPOUT}$).

Warning time can be calculated by:

$$T_{WARN} = \eta C (V_1^2 - V_2^2)/2Po$$

Where:

C = DC-DC Input Bulk Capacitance

$V_1 = VPP_{\_THRESHOLD}$

$V_2 = V_{DROPOUT}$

Po is the instantaneous output power.

For example: if C = 200 µF, V_1 = 42 V, V_2 = 36 V and Po = 25 W, η = 0.87(efficiency), then T_{WARN} = 1.63 ms.

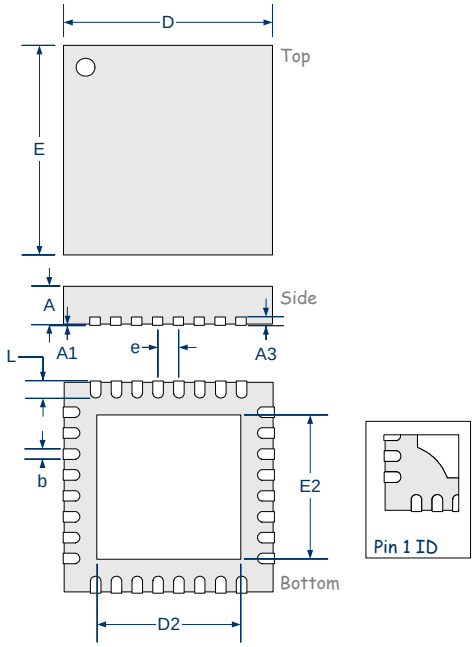
VIN_SEL

The Power Fail Warning and VPP UVLO functions are user selectable via the VINS_SEL pin. Pin function is defined in Table 1:

VINS_SEL	VINS > 1.2V	Operation	Comment
GND	Don't care	PFW	DC-DC controller is enabled depending on VCC and EN pins
VL	No	VPP_{UVLO}	DC-DC controller is not enabled.
VL	Yes	VPP_{UVLO}	DC-DC controller is enabled depending on VCC and EN pins

Table 1 – VINS_SEL Pin Function

LQ 32-Pin 5x5 mm QFN



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	5.00 BSC		0.197 BSC	
D2	3.30	3.60	0.130	0.142
E	5.00 BSC		0.197 BSC	
E2	3.30	3.60	0.130	0.142
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.020

Note:
Dimensions do not include protrusions; these do not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

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PD70101 / PD70201: IEEE 802.3 af/at Power Over Ethernet PD Controller

PRELIMINARY DATA SHEET

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / April 2010		Preliminary Release
0.3 / June 2010		Add Classification Pulse Diagrams
0.3 27 Jul 10		Changing catalog numbers metrology
0.3 12 Nov 10		Extensive changes to document format and Theory of Operation; corrected package drawing; added Product Highlight and Typical Characteristics
0.4 Dec 23 2010		Package update
0.5 Jan 05 2011		Package update
0.6 Jan 21 2011		Extensive format changes for Preliminary Datasheet Release

For support contact: sales_AMSG@microsemi.com

Visit our web site at: www.microsemi.com

Catalogue Number: **DS_PD70101_PD70201**