SmartFusion2 SoC FPGA: Development Kit Demo

User's Guide

Microsemi

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SmartFusion2 SoC FPGA – Development Kit Demo

Purpose

SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) Development Kit demo allows investigating and experimenting with the features of the Smartfusion2 device and development kit. The development kit comes factory programmed to perform this suite of demos. This guide provides instructions for simple demonstrations of the interfaces and peripherals of the development kit. The features can assist engineers with rapid prototyping and testing of their own specific designs.

Introduction

The SmartFusion2 Development Kit demo introduces the components and features of SmartFusion2 SoC FPGAs. This demo design demonstrates—peripheral component interconnect express (PCIe), universal serial bus (USB), double data rate (DDR)3, serial peripheral interface (SPI) flash, Philips inter-integrated circuit (I2C), Flash*Freeze, general purpose I/Os (GPIOs), and the fabric interface controller (FIC) of the SmartFusion2 device.

For more details about SmartFusion2 Development Kit refer to SmartFusion2 Development Kit User's guide.

Demo Requirements

Hardware and Software Requirements

The hardware and software required to run the demo are listed in Table 1:

Table 1. Required Hardware and Software to Run the Demo

Hardware	**Version**
SmartFusion2 Development Kit	Rev C
12 V adapter (provided along with the kit)	–
USB A to USB Mini-B cable (provided along with the kit)	–
USB A to MicroAB cable (provided along with the kit)	–
PCIe Edge Card Ribbon Cable (provided along with the kit)	–
PCIe 2.0 compliant motherboard (not provided – required only for PCIe test)	Operating system: Windows XP SP2 – 32-bit Windows 7 – 32-bit
Software	
USB to UART drivers	–
PciTree	2.04c
Libero® System-on-Chip (SoC)	11.0

Design Files

The design files can be downloaded for this demo from the Microsemi website:

For SmartFusion2 Development Kit Rev C:
http://www.microsemi.com/soc/download/rsc/?f=SF2_DEV_KIT_DEMO_REVC_DF.

For SmartFusion2 Development Kit Rev B:
http://www.microsemi.com/soc/download/rsc/?f=SF2_DEV_KIT_DEMO_REVB_DF.

Design files include:

1. Libero SoC project
2. Readme file

Refer to the Readme.txt file provided in the design files for the complete directory structure.

Demo Setup

Jumper Settings

Table 2. Jumper Settings

Jumper	Pin (From)	Pin (To)
J70, J93, J94, J117, J123, J142, J157, J160, J167, J225, J226, J227	1 (default)	2
J2	1 (default)	3
J23,	2 (default)	3
For USB Connection		
J139, J163, J164	1 (default)	2
For SPI to SPI Flash Connection		
J110, J118, J119, J121	1 (default)	2
For Serial Terminal Connection		
J129, J133	2	3
For I2C0 to I2C1 Connection (It requires patch cords to make connections)		
J135, J172	pin 2 of J135	pin 2 of J172
J213, J174	pin 2 of J213	pin 2 of J174

Host PC to Board Connections

1. Connect one end of the USB Mini-B cable to the J24 connector provided in the SmartFusion2 Development Kit. Connect the other end of the USB cable to the host PC.
2. Connect one end of the USB MicroAB cable to the P1 on-board connector and connect other end of that cable to the PC (type A).

   Note: This cable is required for testing the on-board USB interface.
3. Connect J230 – PCIe Edge connector to the host PC's PCIe GEN1 slot through the PCIe Edge Card Ribbon cable. This is required for testing the PCIe interface.

   Note: Make sure the host PC is OFF while plugging the PCIe connector cable into its PCIe GEN1 slot. Make sure the PCIe slot is enabled in the BIOS settings.
4. Connect the power supply to the J18 connector and power on the board using the SW7 switch. The board setup is shown in Figure 1.

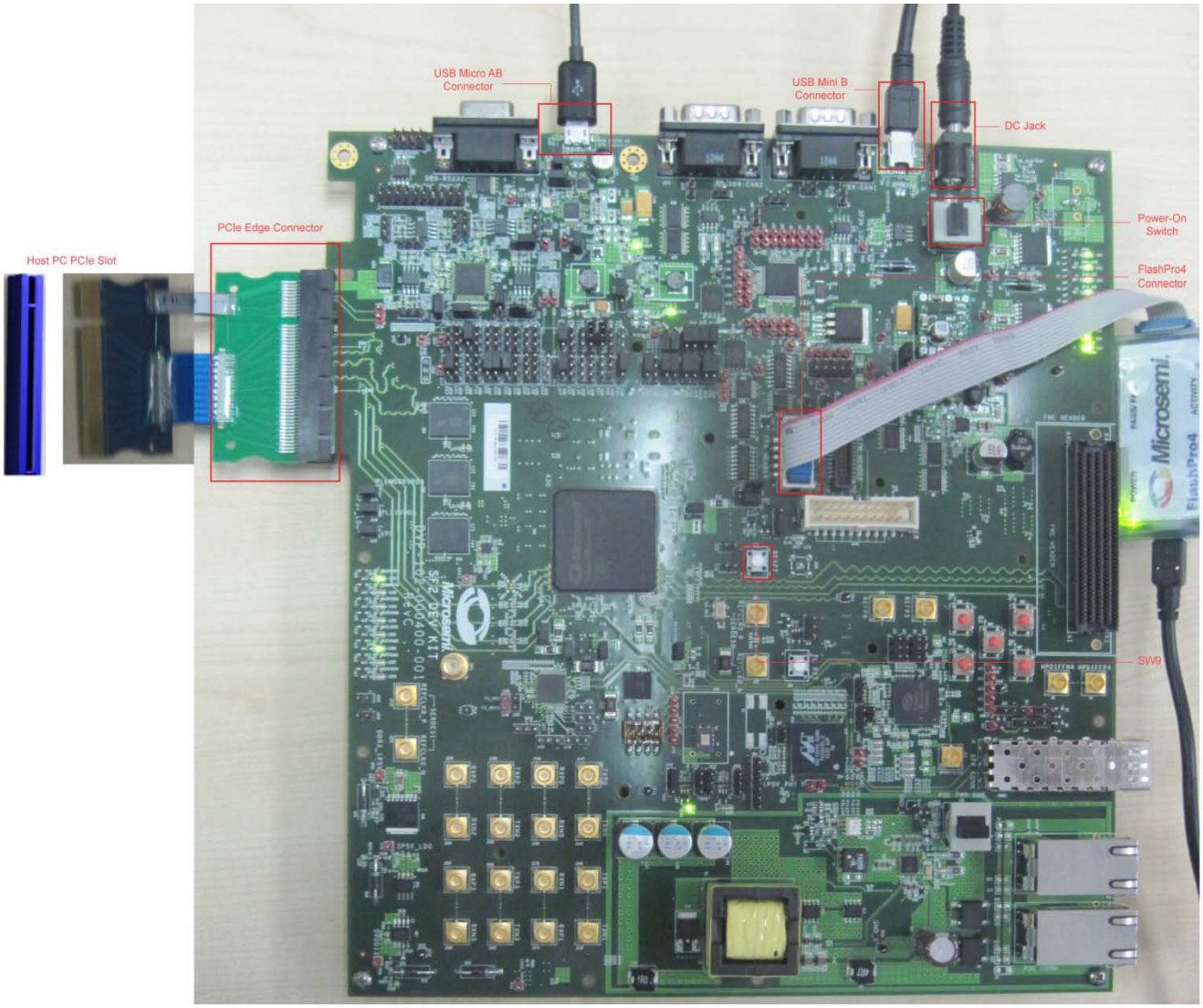

Figure 1. SmartFusion2 Development Kit Setup

Drivers Installation

Serial-Terminal Communication

For serial terminal communication through the Future Technology Devices International (FTDI) mini USB cable, install the FTDI D2XX driver. The drivers and installation guide can be downloaded from http://www.ftdichip.com/Drivers/D2XX.htm.

Make sure that the USB to UART bridge drivers are detected (can be verified in Device Manager), as shown in Figure 2. Note the COM port number for serial port configuration and ensure that the COM port location is specified as **on USB serial Converter D**, as shown in Figure 2.

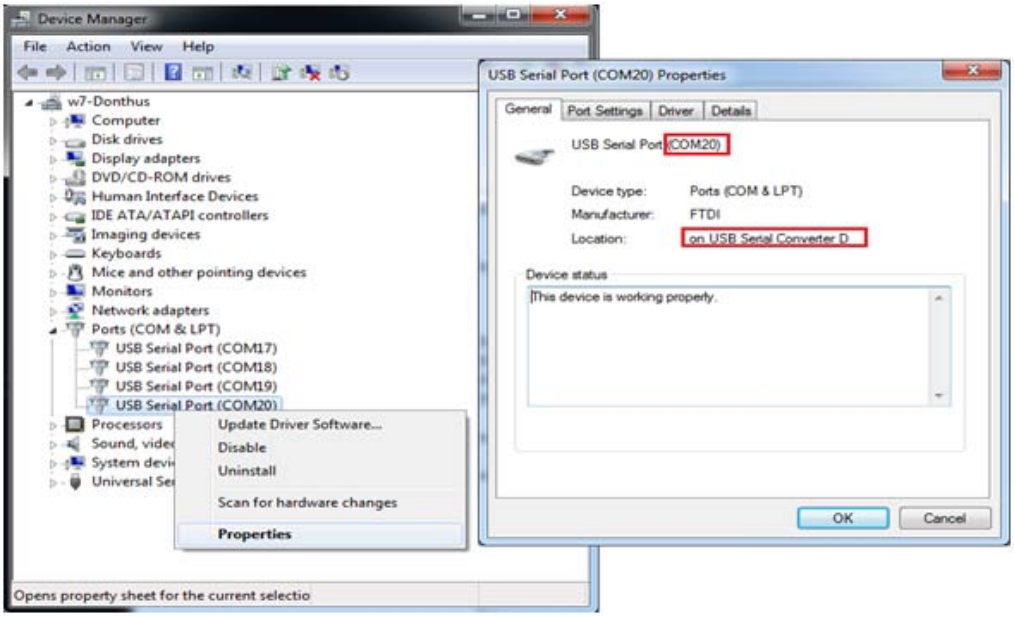

Figure 2. USB to UART Bridge Drivers

PCIe Test

PciTree is a graphic Windows tool for viewing the hardware devices of the PCI bus. Download the PciTree Software from http://www.pcitree.de/download.html. Extract the files to the C drive of the host PC (C:\pcitree).

Make sure that the following files are in the same directory:

- pcitree.exe
- gbhlp.dll
- hlp.vxd
- pcidevs.txt; if present VIDs and DIDs are taken from this list

For **Win NT/2000** systems: hlp.sys must be copied to the \WINNT\SYSTEM32\DRIVERS directory.

For **Windows XP/Vista/7** systems: hlp.sys must be copied to the WINDOWS\SYSTEM32\DRIVERS directory.

Note: PciTree does not support a 64-bit operating system.

For more information on PciTree software and system requirements, refer to http://www.pcitree.de/userguide.html.

Serial Terminal Setup

Start a HyperTerminal session with a baud rate of 57600, 8 data bits, 1 stop bit, no parity, and no flow control.

If your PC does not have HyperTerminal, use any free serial terminal emulation program as PuTTY or Tera Term. Refer to the Configuring Serial Terminal Emulation Programs tutorial for configuring HyperTerminal, Tera Term, and PuTTY.

Running the Tests

The demo design has 9 tests and the following steps describe how to run each test. Tests 1 through 8 can be run independently in any order but test 9 (PCIe test) requires the following steps:

a. Rebooting the host PC as explained in Step 14.

b. Invoking the PCITree GUI as explained in Step 15.

1. Press **Reset Switch SW9** on the SmartFusion2 Development Kit to reset the board. A message is displayed on HyperTerminal, as shown in Figure 3.

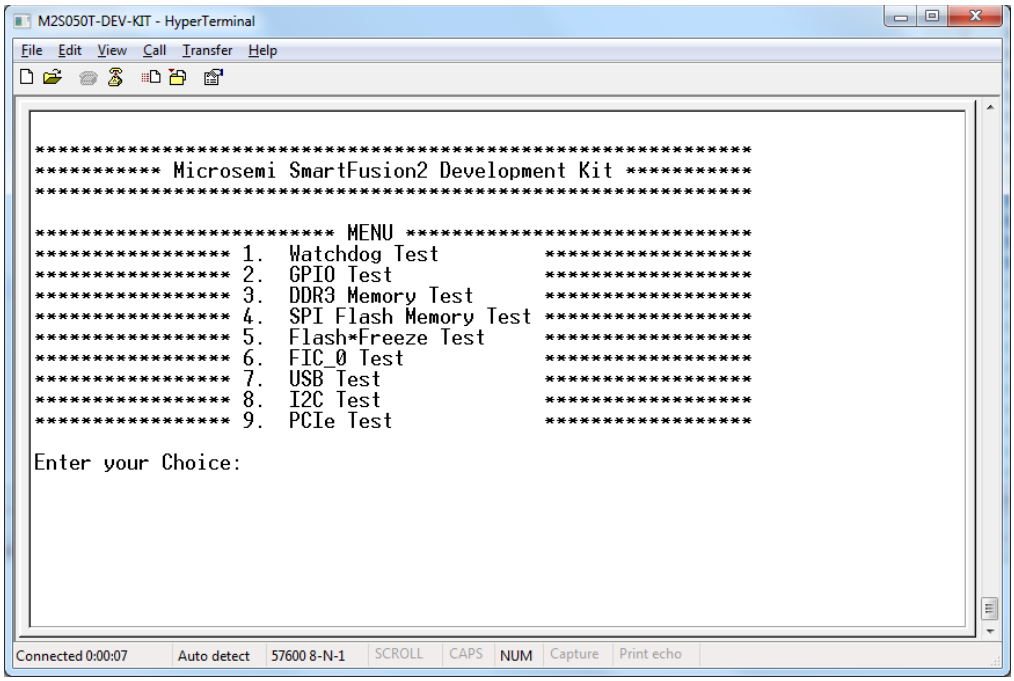

Figure 3. Test Menu

Note: If this message does not appear, press SW9. If the above message still does not appear, refer to the Serial Terminal Setup and Drivers Installation sections and ensure that the terminal has been set up correctly.

2. Enter **1** into the terminal to begin the Watchdog test. Messages are displayed, as shown in Figure 4. The Watchdog Timer is configured to generate a system reset on timing out. Watchdog Timer will generate a system reset after 35 seconds.

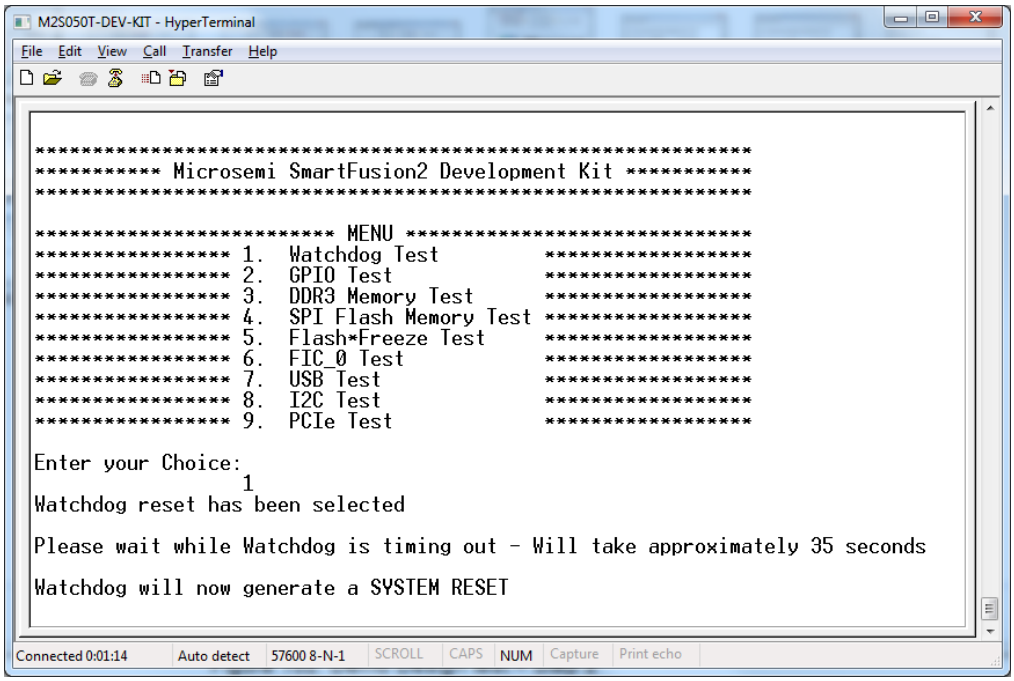

Figure 4. Watchdog Test

3. Enter **2** into the terminal to begin the GPIO test. A message is displayed, as shown in Figure 5.

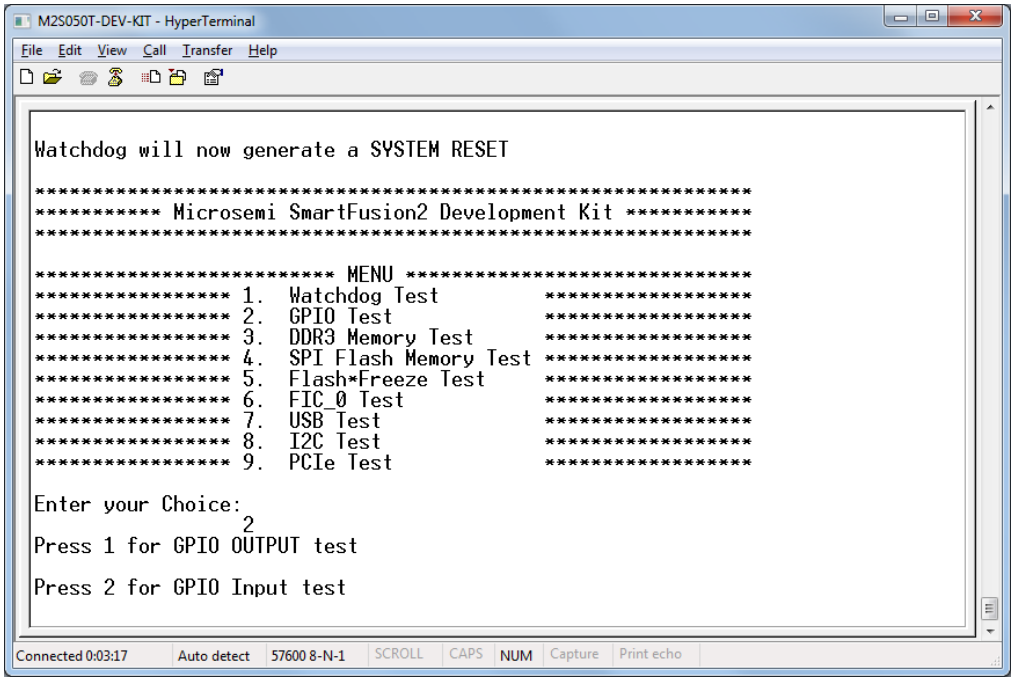

Figure 5. GPIO Test

4. Enter **1** for GPIO output test. Follow the instructions that appear in the terminal window to complete the GPIO Output test. On completion of the GPIO output test a message is displayed, as shown in Figure 6.

   GPIO 14 and 15 are configured as outputs and connected to LED2 and LED3 on the board. The firmware running on the Cortex-M3 processor controls the LED's through GPIO's.

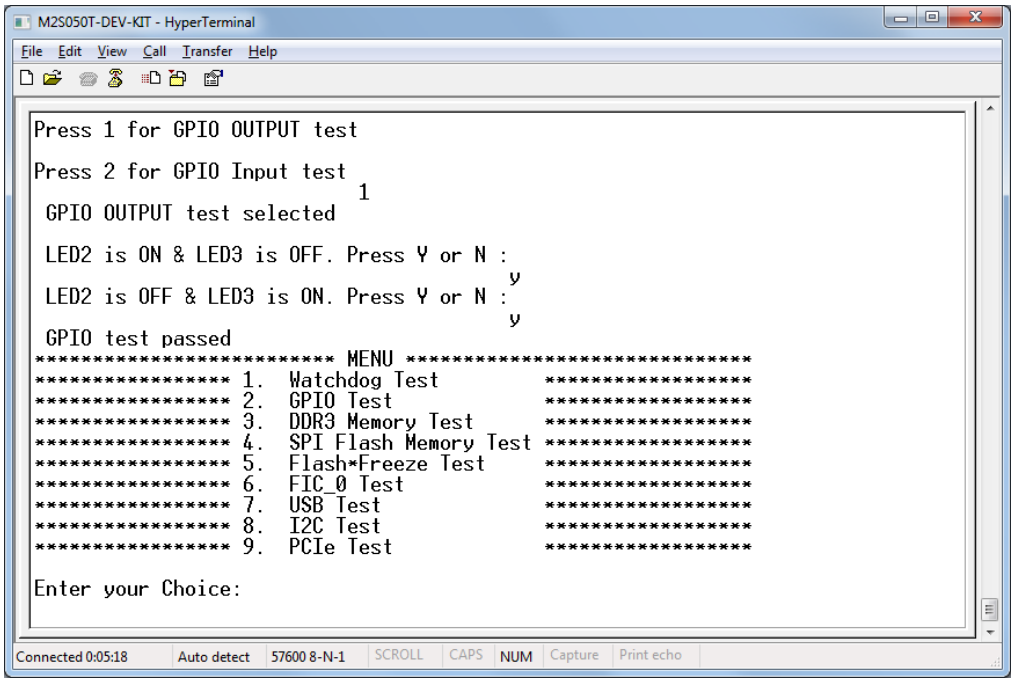

Figure 6. GPIO Output Test

5. Enter **2** into the terminal to begin the GPIO test and enter **2** for GPIO output test. A message is displayed, as shown in Figure 7. Follow the instructions that appear in the terminal window to complete the GPIO input test. Press **SW9** to exit from GPIO input test.

GPIO 11, 12, and 13 are configured as inputs and their respective interrupts to the ARM® Cortex™-M3 processor are enabled. Change the DIP2/DIP3/DIP4 state on the SmartFusion2 Development Kit.

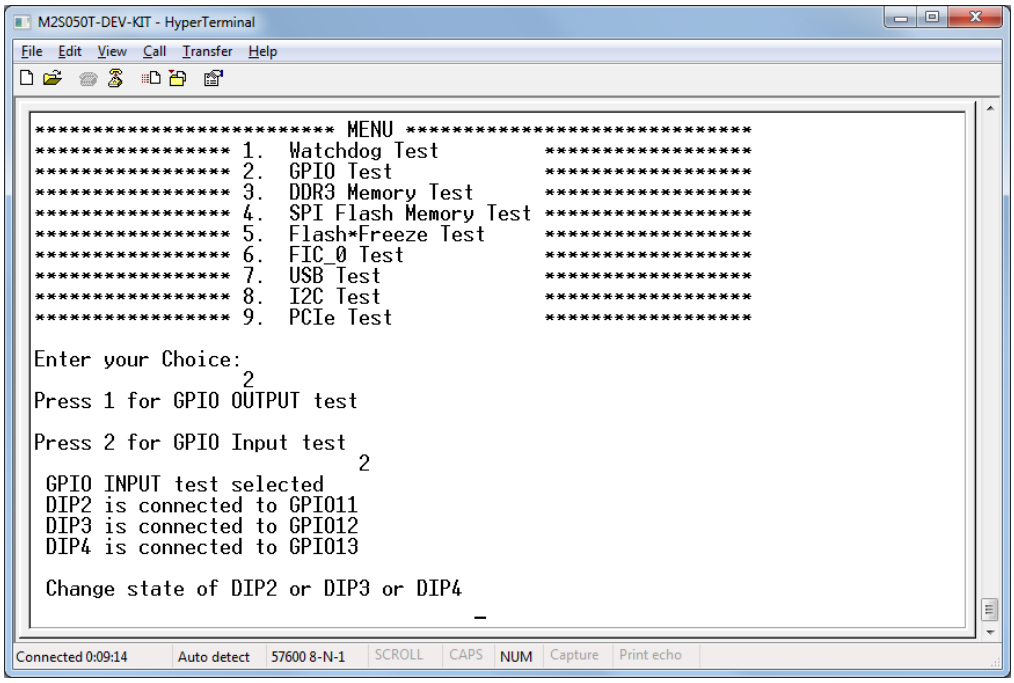

Figure 7. GPIO Input Test

6. Enter **3** into the terminal to begin the DDR3 test. A message is displayed, as shown in Figure 8.

   The high performance DMA (HPDMA) controller writes 256 MB of data to the DDR3 memory. The Cotex-M3 processor compares the written data against expected values. Verifying the DDR contents takes approximately 1 minute.

   On successful verification, **DDR3 Memory test passed** is displayed. If the comparison fails, the DDR address for which verification failed is displayed along with the expected data and read data. At the end, the number of read and write access errors will be displayed.

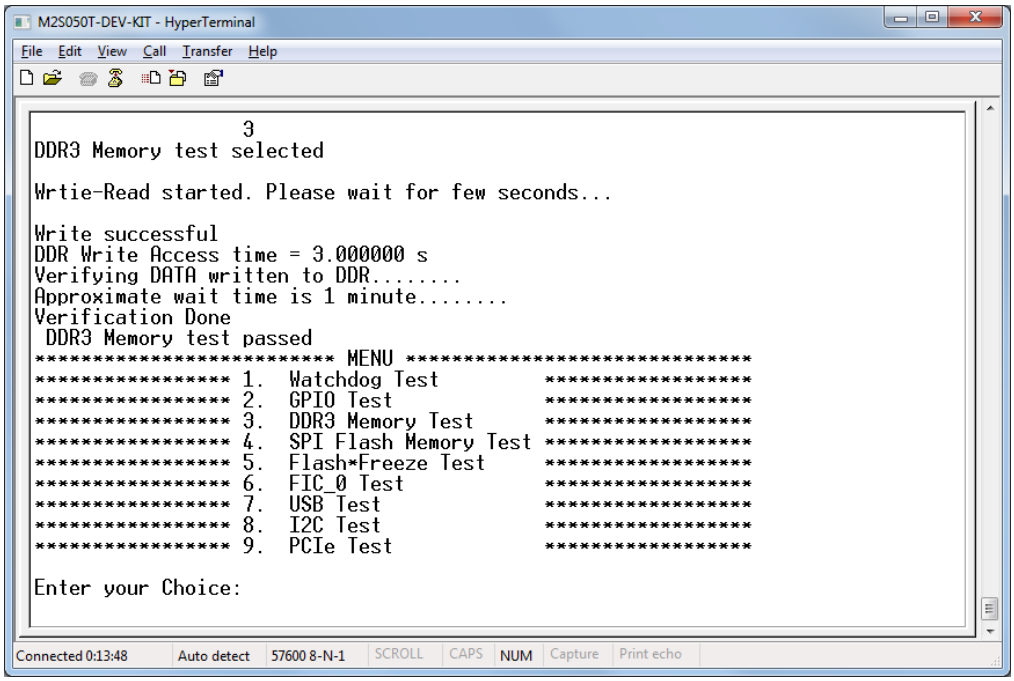

Figure 8. DDR3 Memory Test

7. Enter **4** into the terminal to begin the SPI test. A message is displayed, as shown in Figure 9.
   In the SPI memory test, the SPI controller first reads the device ID of on-board SPI flash.

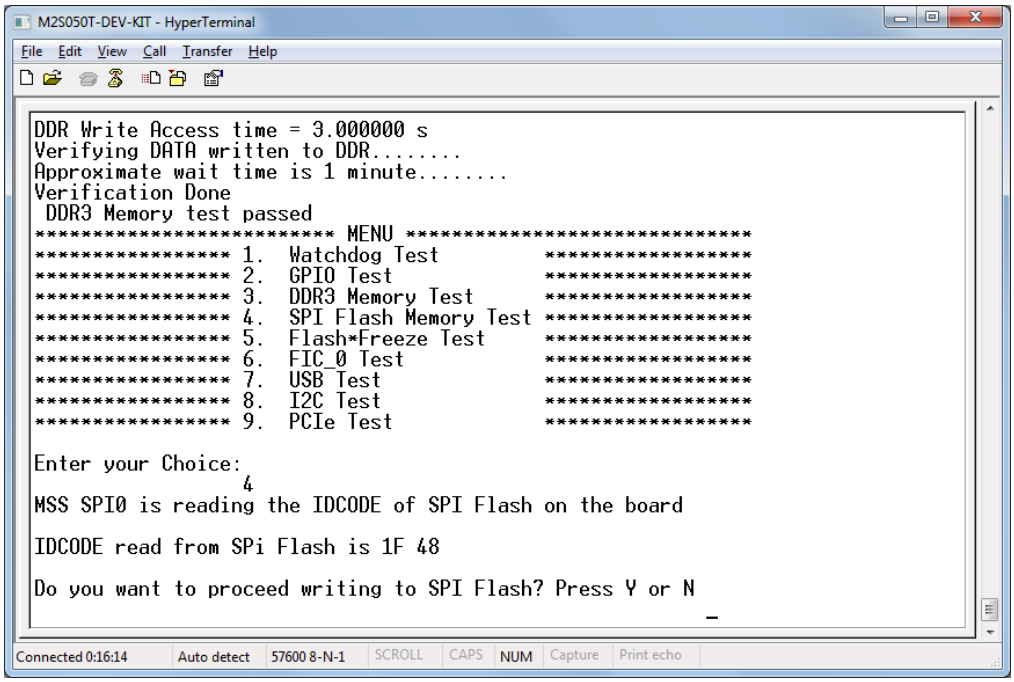

Figure 9. SPI Flash Memory Test

8. Enter **y** to write and read the data to and from SPI flash. After completion of the test, a message is displayed, as shown in Figure 10. The Cortex-M3 processor writes 256 bytes of data to SPI flash, reads back from the SPI flash memory and is compared with the data to validate a successful read write transaction on the SPI memory.

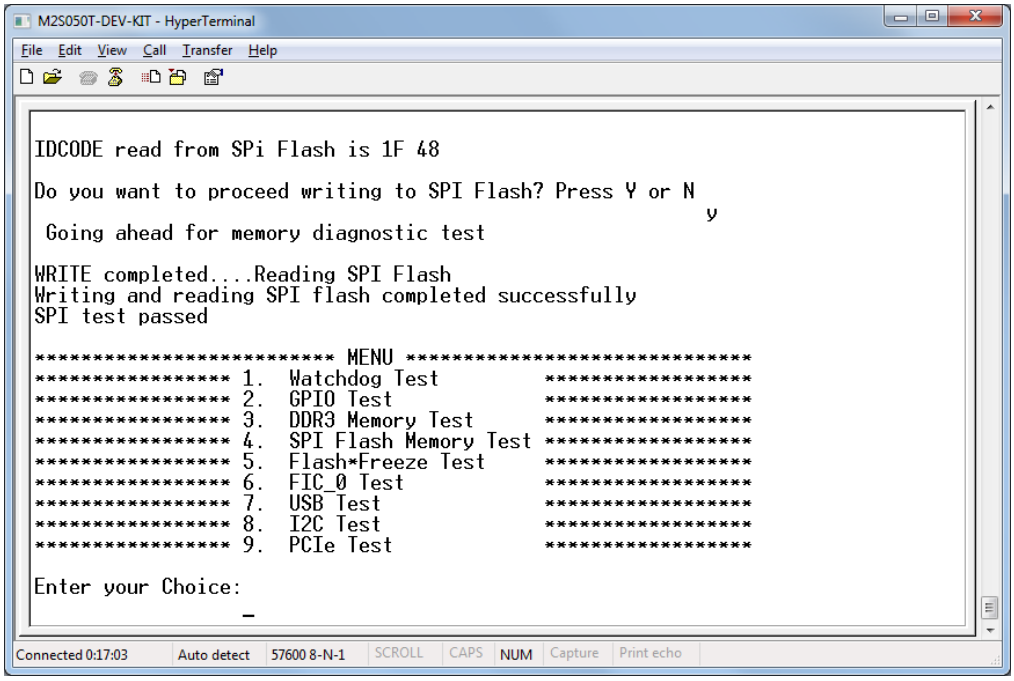

Figure 10. SPI Flash Memory Test

9. Enter **5** into the terminal to begin the Flash*Freeze test. A message is displayed, as shown in Figure 11.

Follow the instructions shown in the terminal window. The SmartFusion2 device enters into Flash*Freeze mode. To exit from Flash*Freeze mode, press **SW3** on the board and press **SW9** for the main menu.

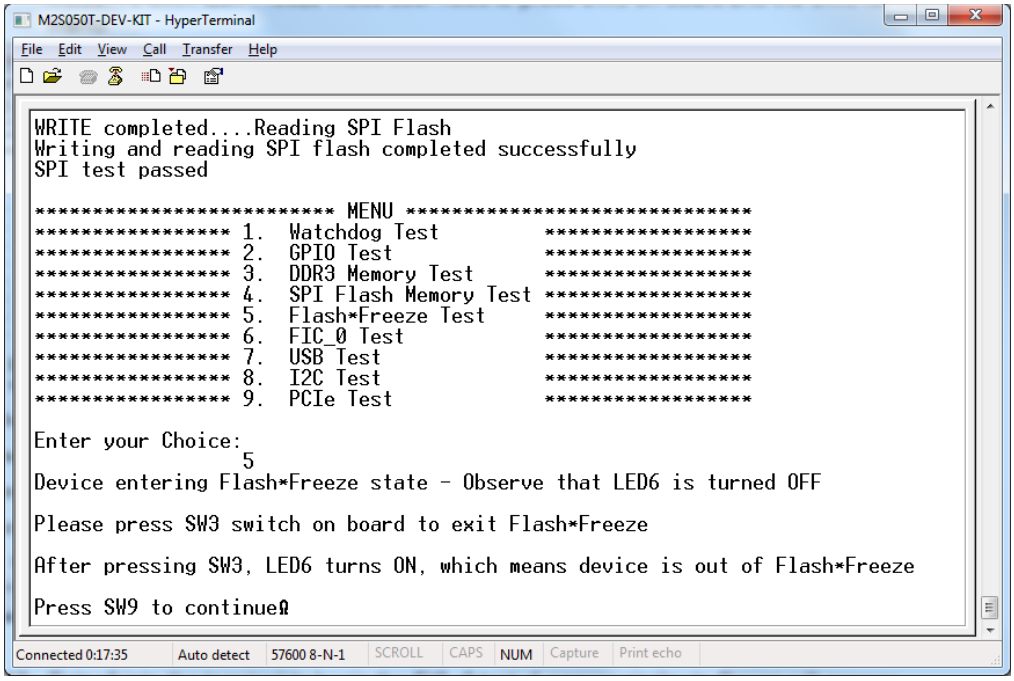

Figure 11. Flash*Freeze Test

10. Enter **6** into the terminal to begin the FIC_0 test. A message is displayed, as shown in Figure 12. The CoreABC is used as the fabric master for accessing eSRAM1 memory through FIC_0. The CoreABC writes data to the eSRAM1, reads back from the eSRAM1 and is compared with the data to validate successful read write transactions.

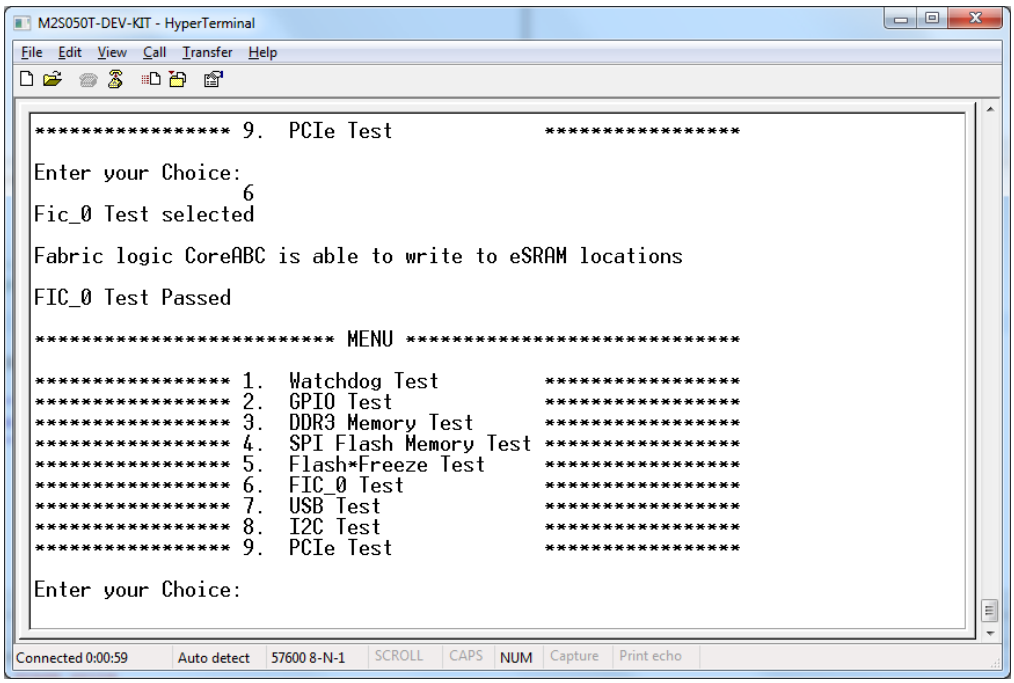

Figure 12. FIC_0 Test

11. Enter **7** in the terminal to begin the USB test. A message is displayed, as shown in Figure 13.

In this test, the Smartfusion2 USB is configured in Device mode. The application firmware configures the device to work as a human interface device (HID) mouse. The directions of the mouse are controlled through the switches on the SmartFusion2 Development Kit.

Follow the instructions that appear on HyperTerminal and observe the cursor movement on the host PC screen.

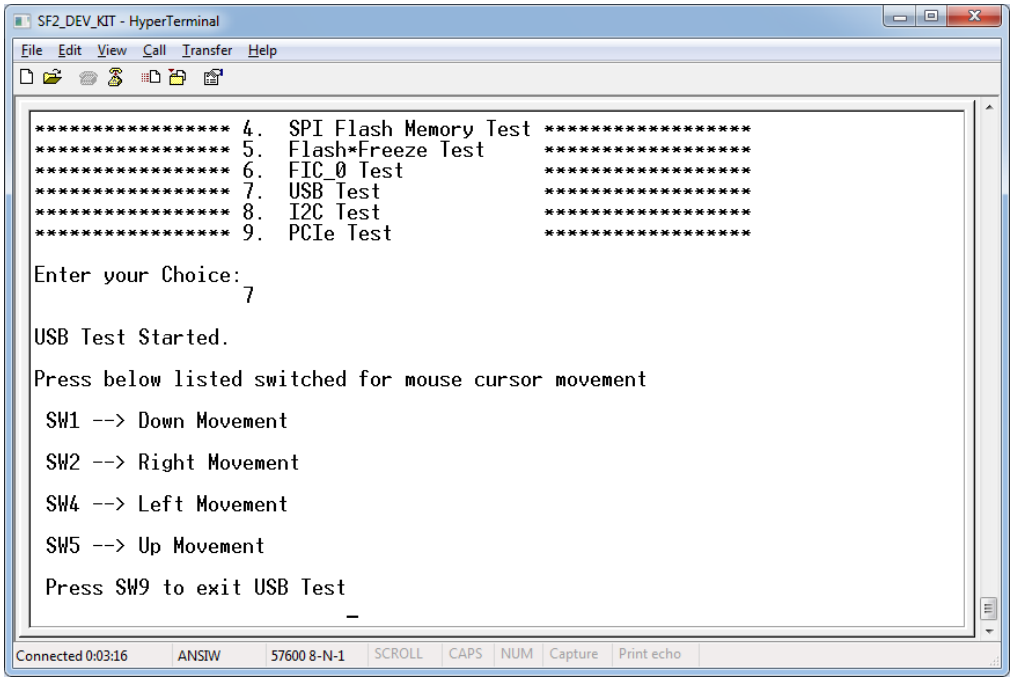

Figure 13. USB Test

12. Enter **8** in the terminal to begin the I2C test. A message is displayed, as shown in Figure 14.

    For the I2C test, I2C0 is configured as the slave and I2C1 is configured as the master. Master sends data to slave. Received data by slave is compared with the expected data to validate the successful transaction.

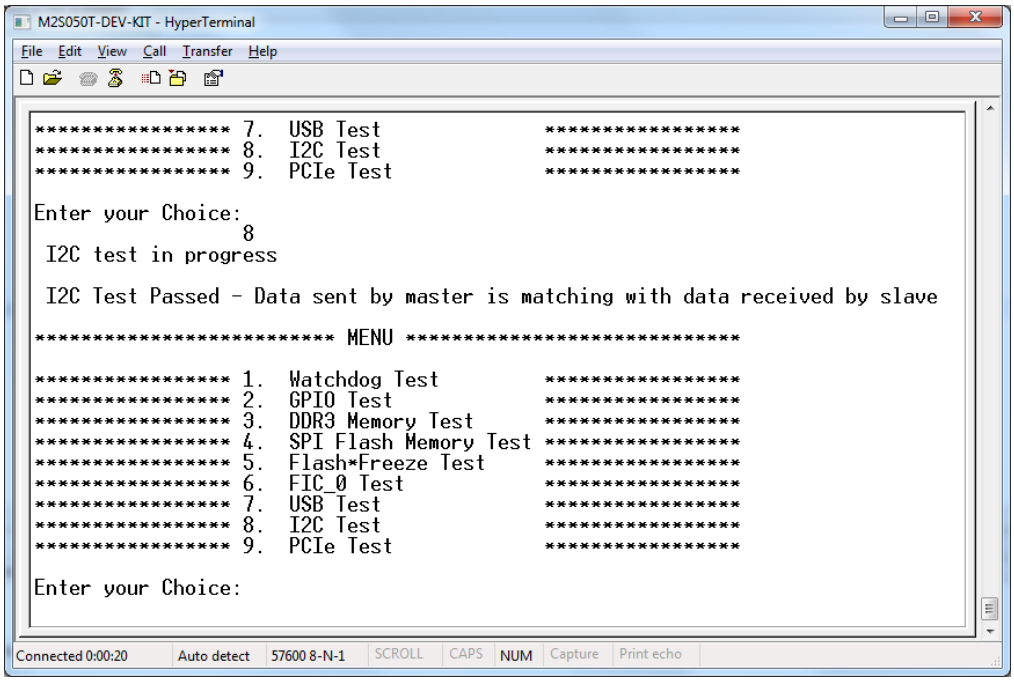

Figure 14. I2C Test

13. **To run the PCIe test**:
    a. Switch-off the SmartFusion2 Development Kit using **SW7**.
    b. Shutdown the host PC.
    c. Power-on the SmartFusion2 Development Kit using **SW7**.
    d. Start the host PC.
14. After restarting the host PC, start the HyperTerminal program and enter **9** into the HyperTerminal to begin the PCIe test. A message is displayed, as shown in Figure 15.

    Note: Make sure that the SmartFusion2 Development Kit PCI Edge connector J230 is connected to PCIe GEN 1 slot of host PC.
    Make sure that the PciTree software is installed on host PC.
    Make sure that the host PC has been restarted while keeping the SmartFusion2 Development Kit in ON state.

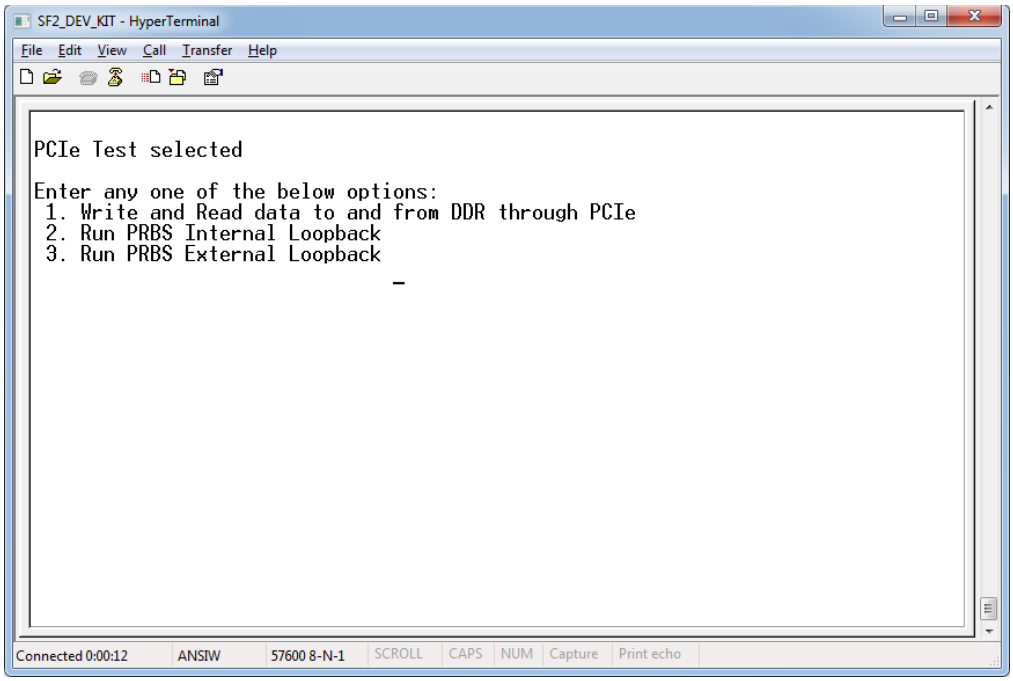

Figure 15. PCIe Options

15. Enter **1** in the terminal to write the data to DDR3 memory through PCIe using PciTree. A message is displayed, as shown in Figure 16.

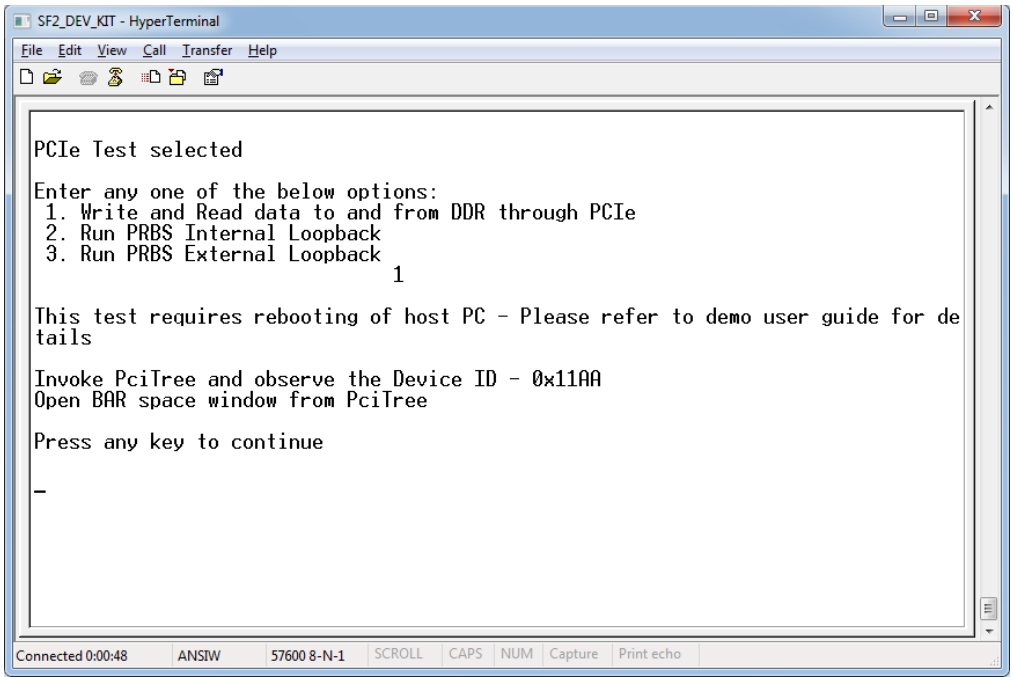

Figure 16. PCIe Write

16. Double-click **pcitree.exe** to invoke PciTree. A window is displayed, as shown in Figure 17. In the PciTree tool, observe the PCI device with ACTEL ID 0x11AA (Figure 17). If unable to locate the PCI device, check the PCIe connections, restart the host PC, and begin the PCIe test again.

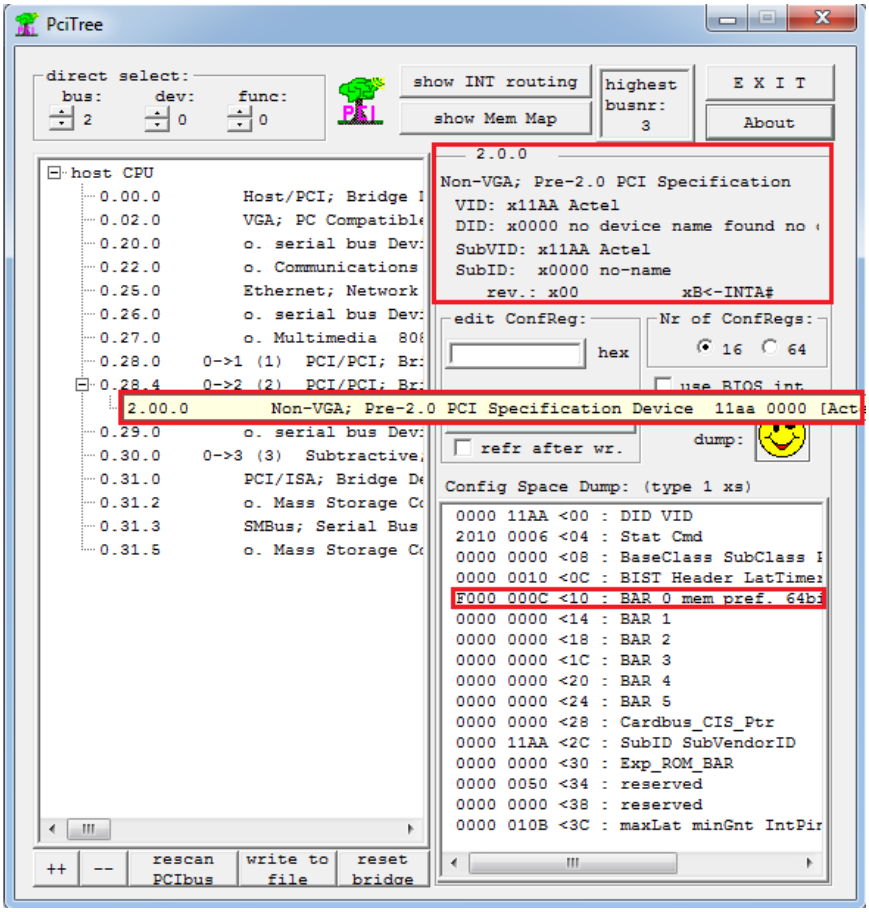

Figure 17. PciTree Tool

17. Click **Actel device x11AA**, select **BAR0,** and double-click **Bar**.
18. Click **Yes** to perform read-write.

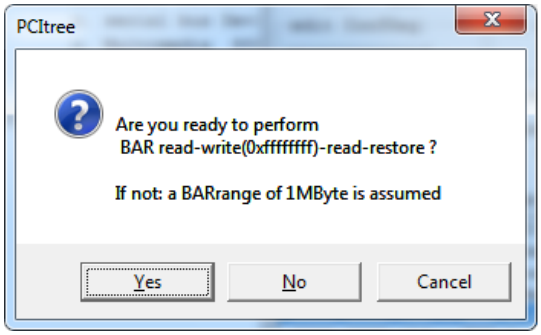

Figure 18. Perform BAR Read-Write

19. The BAR space window is displayed, as shown in Figure 19.

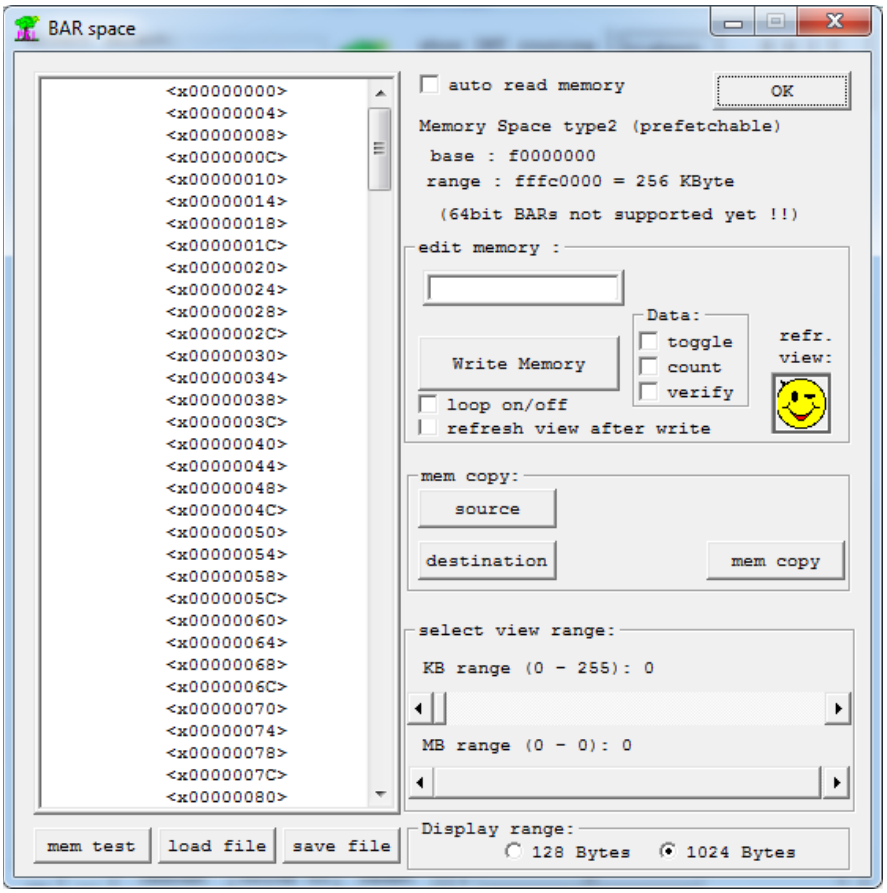

Figure 19. BAR Space

20. Enter any key in the HyperTerminal. A message is displayed, as shown in Figure 20.

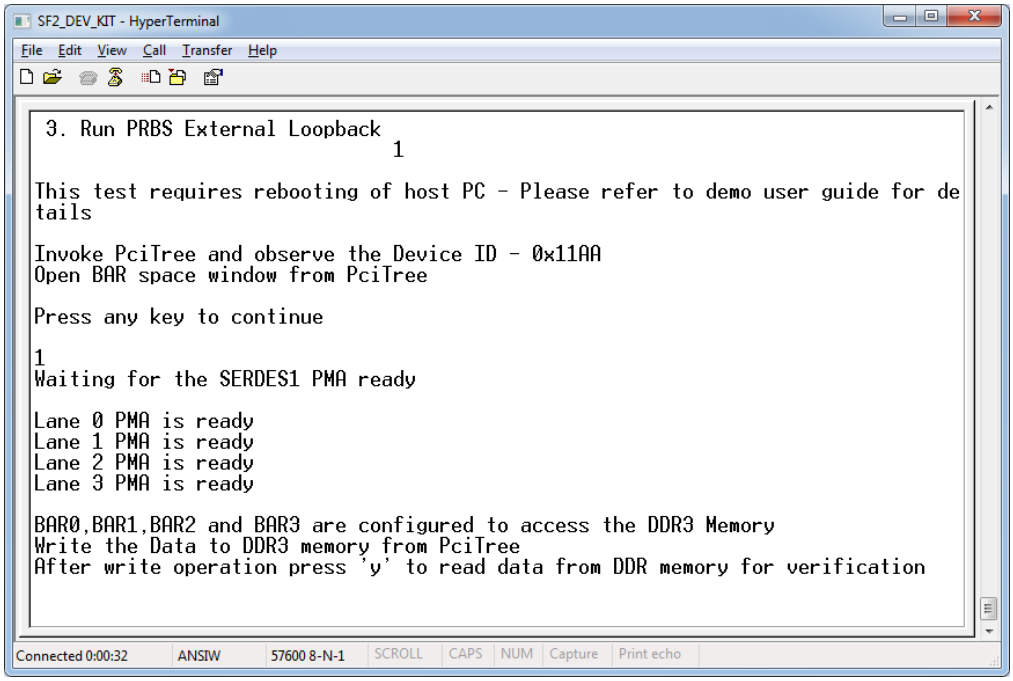

Figure 20. PCIe Test

21. Select the **refresh view after write** check box in the Bar space window and select the **auto read memory** check box, as shown in Figure 21.

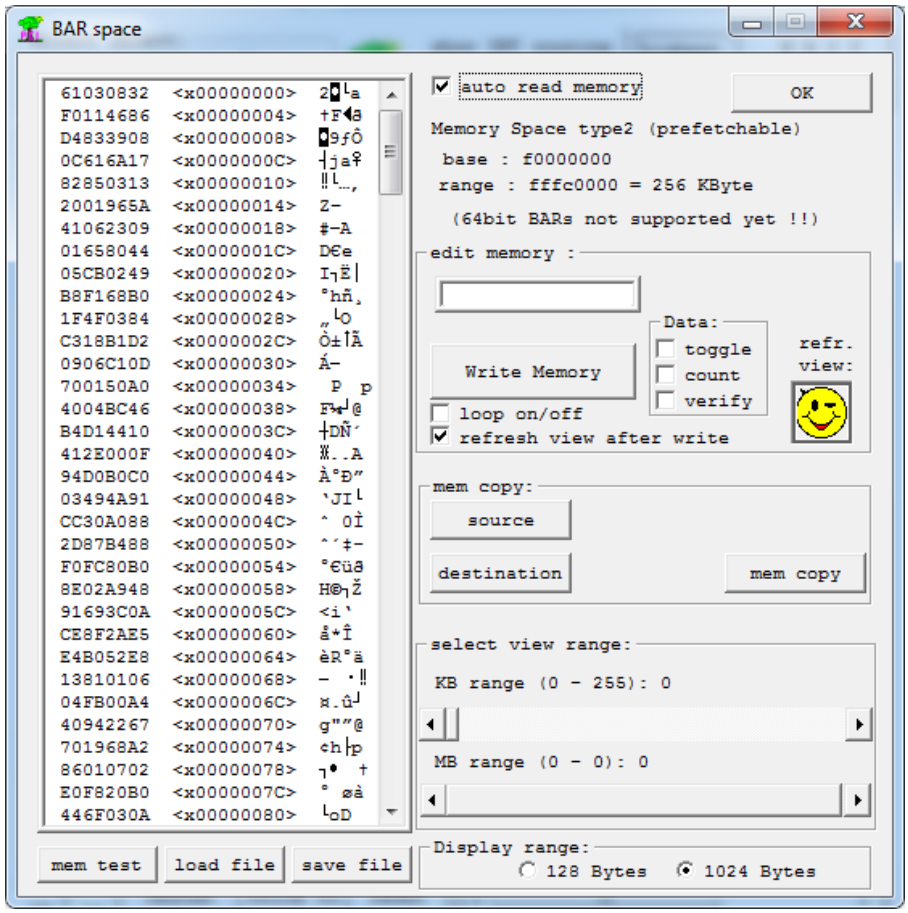

Figure 21. BAR Space

22. Click **mem test**. Click **Yes** when it prompts for 1K memory range display.

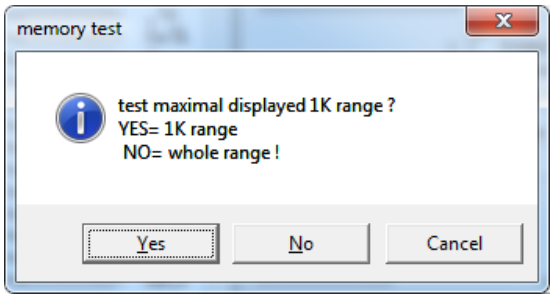

Figure 22. Memory Test

23. Press **OK** when the following tab appears. This shows PciTree is successfully completed writing and reading the data from DDR3 memory through the MDDR AXI interface. PciTree checks for data integrity when you choose the **auto read** memory check box during the mem test.

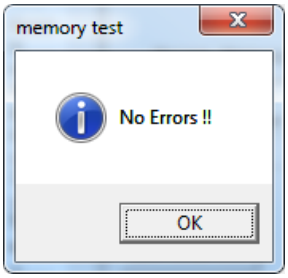

Figure 23. Memory Test

24. Enter **y** in the terminal to Read data from DDR3 for verifying the written data on DDR3 memory using HyperTerminal. To skip reading the data from DDR3, enter any other key. The messages will appear on HyperTerminal, as shown in Figure 24.

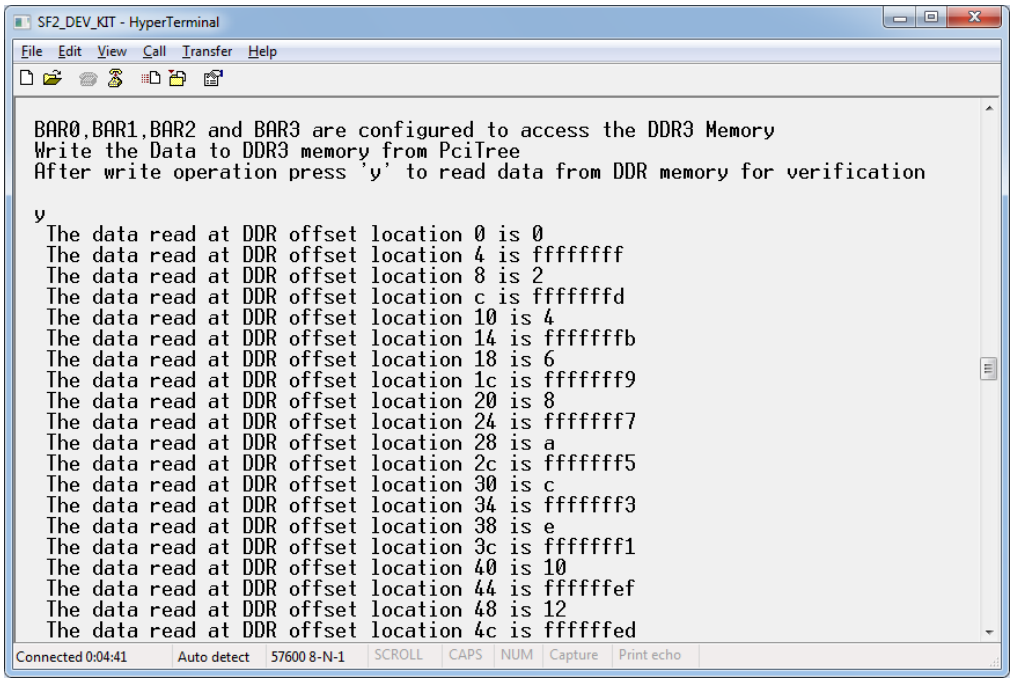

Figure 24. Read DDR3 Memory

25. Compare the HyperTerminal values with PciTree memory, as shown in Figure 25. This confirms successful completion of read and write from PCIe.

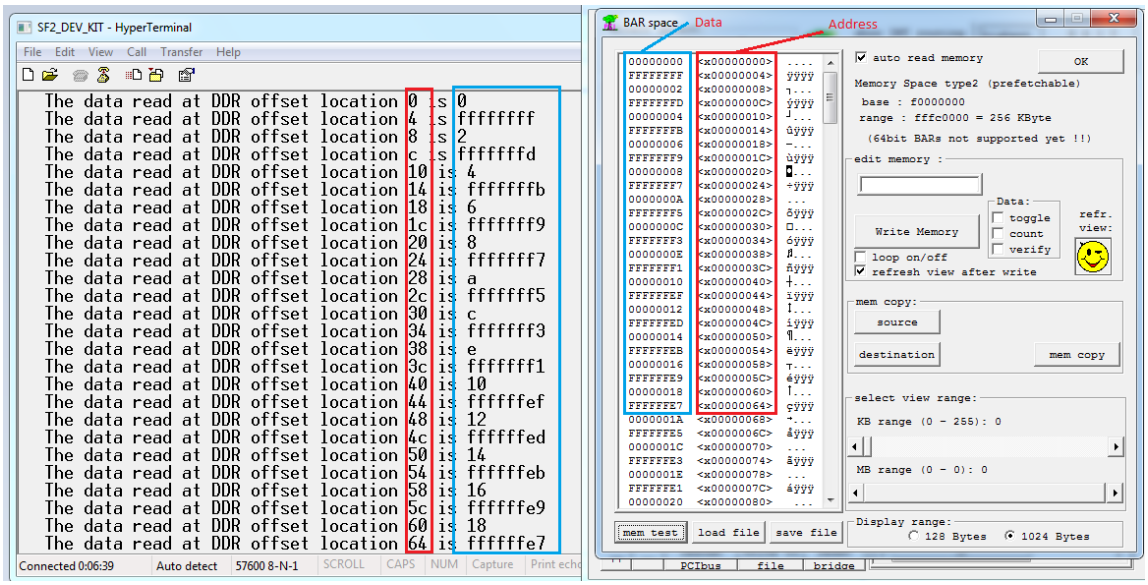

Figure 25. Comparing DDR3 Data and PciTree Bar

26. Enter **9** in the terminal and enter 2 to begin the pseudo-random binary sequence (PRBS) Internal Loopback test. A message is displayed, as shown in Figure 26.

    In PRBS Internal Loopback test, the TX and RX are internally looped back; thus it loses the connection with the Host PC.

    Note: The DDR3 read write data test should be run prior to the PRBS test.

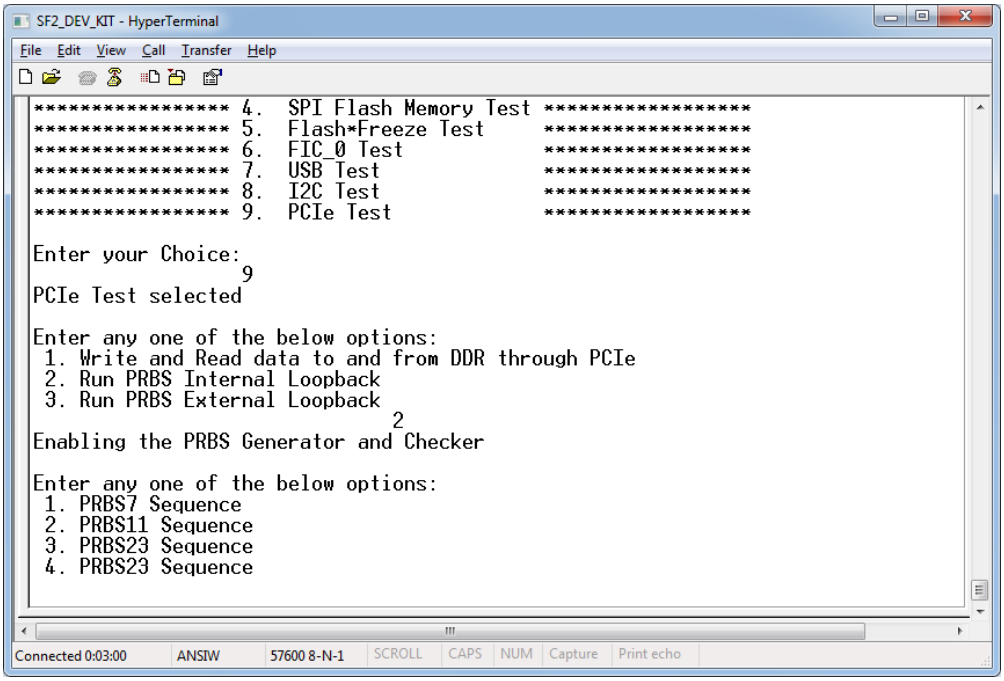

Figure 26. PRBS Internal Test

27. Enter your choice on terminal window. A message is displayed as shown in Figure 27.

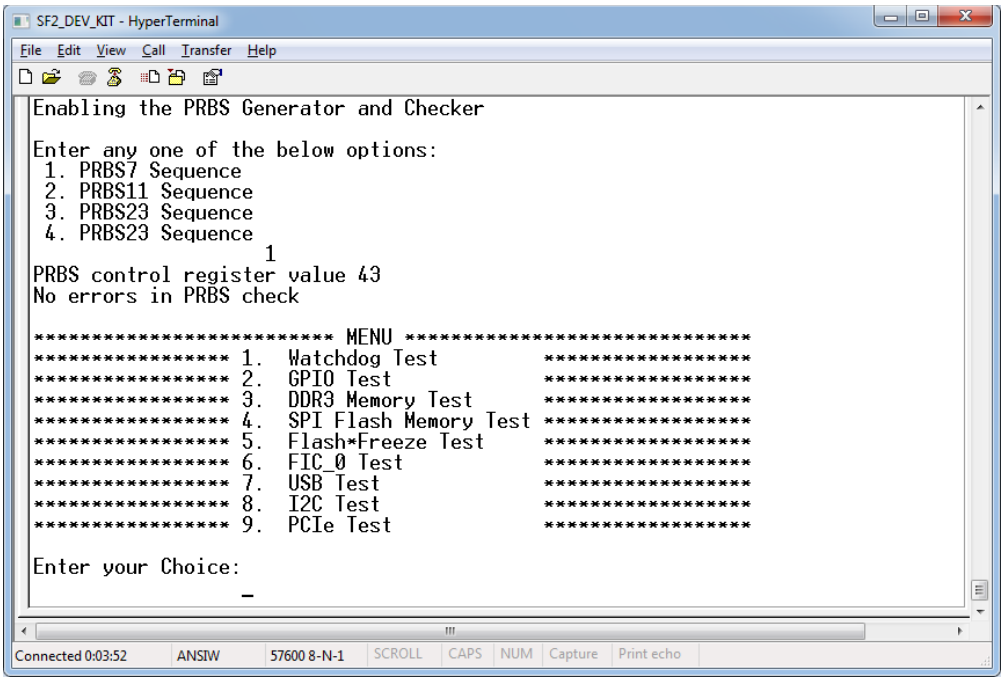

Figure 27. PRBS7 Sequence Check

28. PRBS external loop back test needs TX and RX lanes to be looped back externally. This requires removal of certain resistors from SmartFusion2 Development Kit. Refer to Table 3 for list of resistor changes required to run this test. The resistor changes are required only for running External loop back test and need to be replaced with original resistors that were on the board for running the Test 9 (PCIe test) again.

Table 3. Set Up for PCIe External Loopback Test

Function	Resistor	Instructions
RX lane	R609 R608	Depopulate these resistors
	R611 R610	
	R612 R613	
	R614 R615	
	R604 R598	Populate these resistors
	R605 R599	
	R600 R606	
	R607 R602	
TX lane	R279 R278	Depopulate these resistors

	R277 R276	
	R275 R274	
	R283 R282	
	R267 R269	Populate these resistors
	R280 R281	
	R268 R270	
	R285 R286	

Once set-up is done, run the external loopback test by following the instructions on HyperTerminal.

Reprogramming the M2S050T Development Kit

1. Open **FlashPro** programming software.

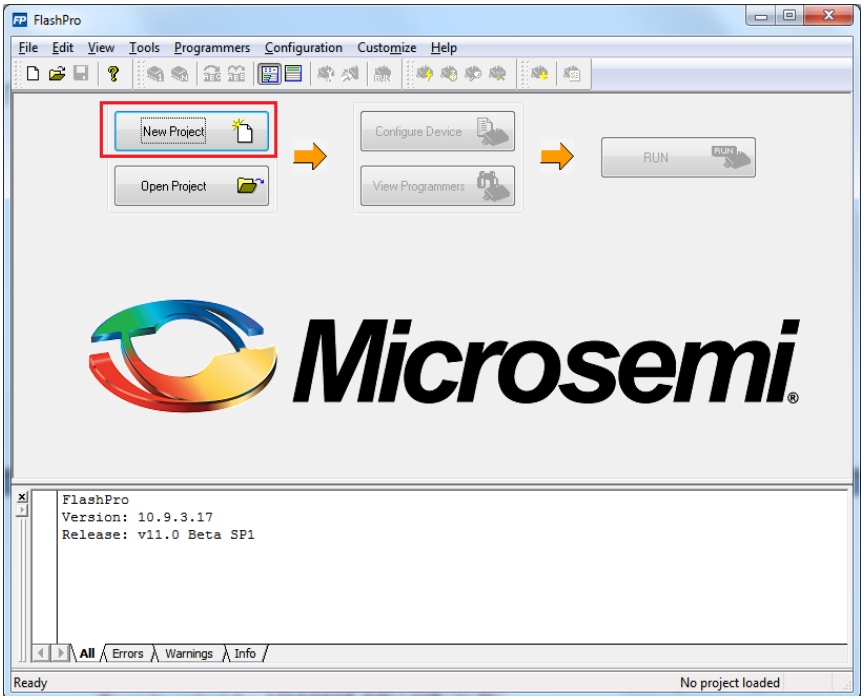

Figure 28. FlashPro

2. Create a new programming project. Select **Single device** under Programming mode.

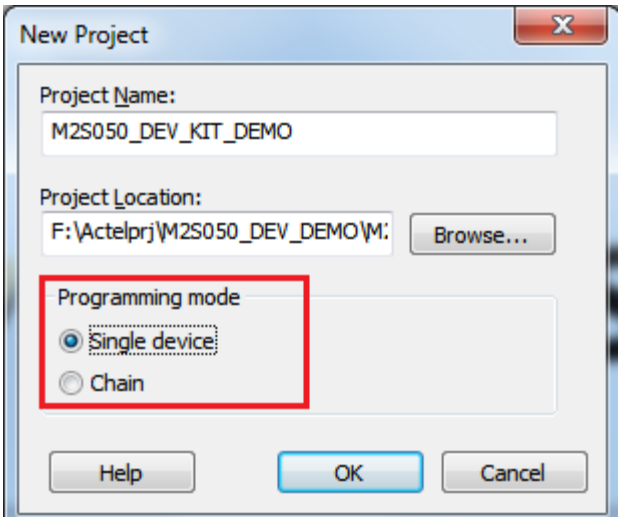

Figure 29. Creating New Project

3. Click **Configure Device**. This shows the existing **Programming file** section, as shown in Figure 31.

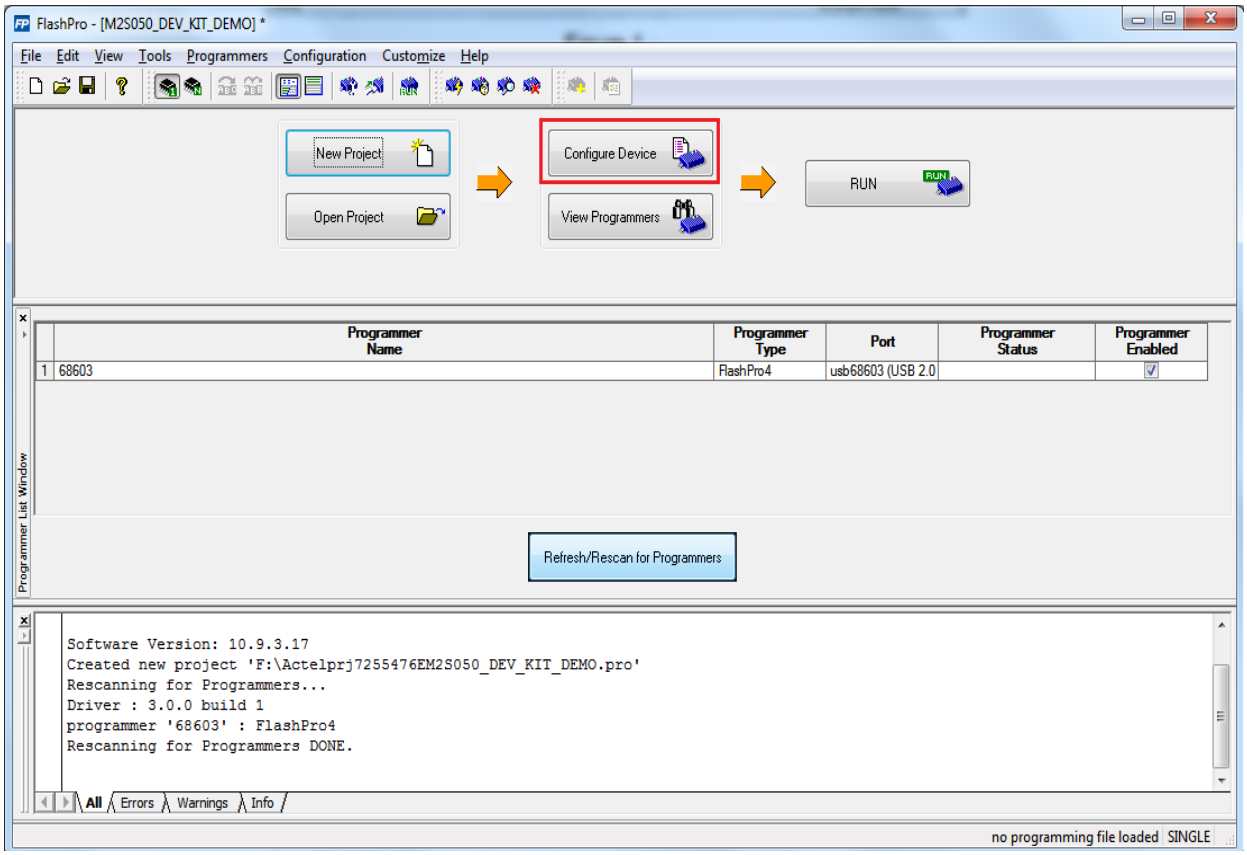

Figure 30. Configure Device

4. Click **Browse** to select the DEV_KIT_DEMO_top.stp programming file from the PC. Click **Open** to select the DEV_KIT_DEMO_top.stp file. The programming file can be downloaded from Microsemi website:

   For SmartFusion2 Development Kit Rev C:
   http://www.microsemi.com/soc/download/rsc/?f=SF2_DEV_KIT_DEMO_REVC_PF.

   For SmartFusion2 Development Kit Rev B:

   http://www.microsemi.com/soc/download/rsc/?f=SF2_DEV_KIT_DEMO_DESIGN_REVB_PF.

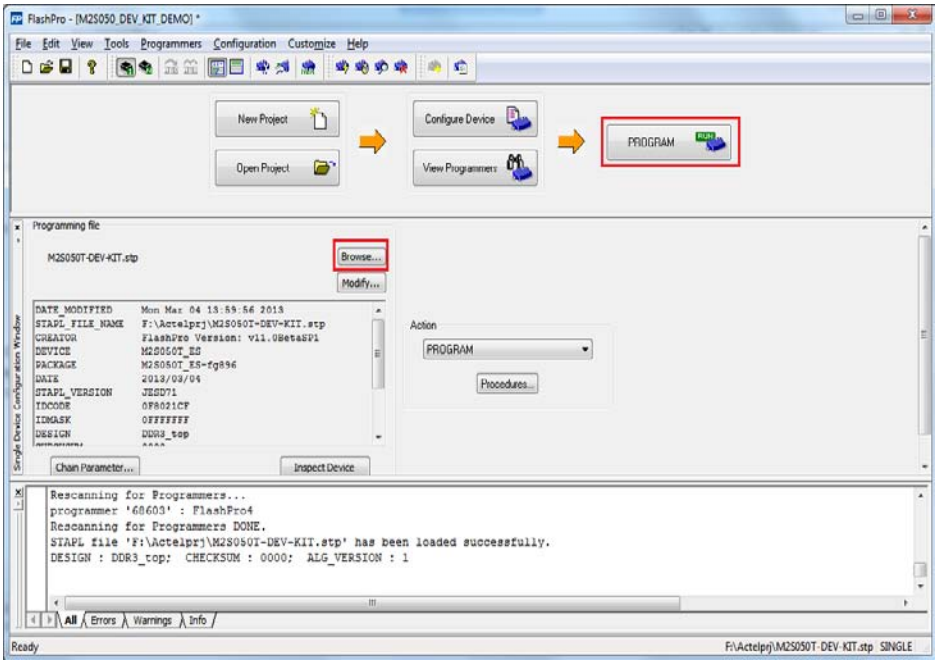

Figure 31. Program The Device

5. Click **PROGRAM** to program the M2S050T development kit.

   Note: Do not interrupt the programming sequence. It may damage the device or the programmer. If you face any problems, contact Microsemi SoC Products Group Tech Support at soc_tech@microsemi.com.

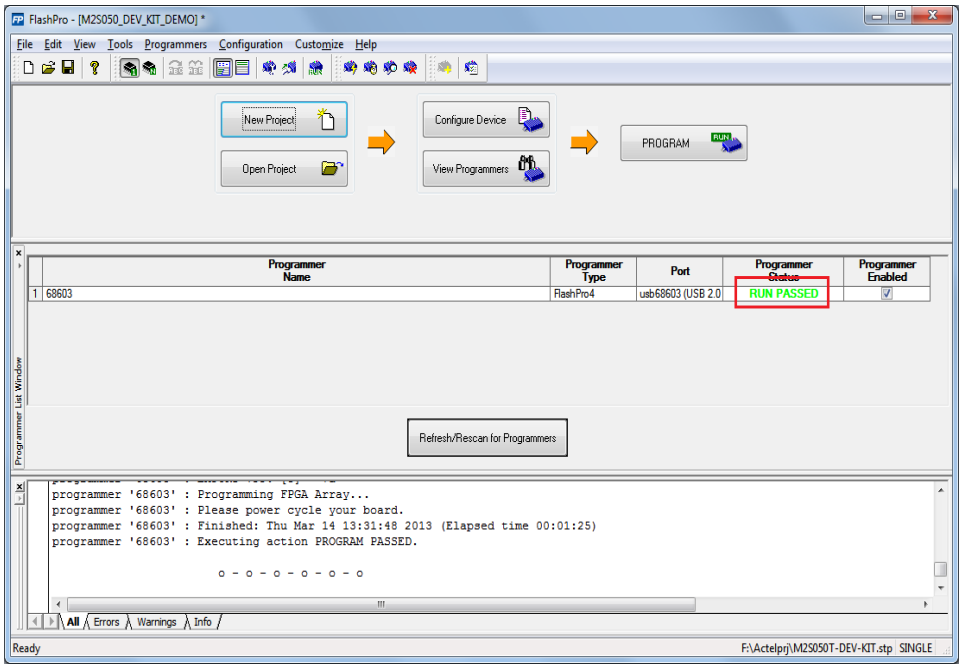

Figure 32. Successful Programming

Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**
From the rest of the world, call **650.318.4460**
Fax, from anywhere in the world **408.643.6913**

Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Visit the Microsemi SoC Products Group Customer Support website for more information and support (http://www.microsemi.com/soc/support/search/default.aspx). Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on website.

Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at http://www.microsemi.com/soc/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.

Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Sales office listings can be found at www.microsemi.com/soc/company/contact/default.aspx.

ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech_itar@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.

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