Innoveda eProduct Designer

Interface Guide

Table of Contents

Introduction

The *Mentor Graphics® eProduct Designer Interface Guide* contains information about using the eProduct Designer CAE software tools with the Actel Designer FPGA development software tools to create designs for Actel devices. Refer to the *Actel Quick Start Tutorial* for additional information about using the Designer series software and the Innoveda documentation for information about using the eProduct Designer software.

Document Organization

The *Mentor Graphics eProduct Designer Interface Guide* contains the following chapters:

Chapter 1 - Setup contains information about setting up the eProduct Designer software for use in creating Actel designs.

Chapter 2 - Design Flow describes the design flow for creating Actel designs using eProduct Designer software and Designer Series software.

Chapter 3 - Actel-Mentor Graphics Design Considerations contains information to assist you in creating Actel designs with eProduct Designer and Designer Series software.

Chapter 4 - Simulation Using ViewSim® contains information about simulating Actel designs with ViewSim.

Chapter 5 - Simulation Using SpeedWave™ contains information about simulating Actel designs with SpeedWave.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

This document assumes the following:

1. You have installed the Designer Series software in the "C:\Actel" directory.

2. You have installed the eProduct Designer software in the "C:\ePD" directory.

3. You are familiar with PCs and Windows operating environments.

4. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

This document uses the following conventions:

Information input by the user follows this format:

keyboard input

The content of a file follows this format:

file contents

The <act_fam> variable represents an Actel device family. To reference an actual family, substitute the name of the Actel device when you see this variable. Available families are Fusion, IGLOO™/e, ProASIC3/E, act1, act2 (for ACT2 and 1200XL devices), ACT3, 3200DX, MX, SX, SX-A, eX, Axcelerator, A500k, and APA.

The <vhd_fam> variable represents Compiled VHDL libraries. To reference an actual compiled library, substitute the name of the library Fusion, IGLOO/e, ProASIC3/E, act1, act2 (for ACT 2 and 1200XL devices), ACT3, A3200DX, MX, SX, eX, Axcelerator, A500k, and APA) when you see this variable. Compiled VHDL libraries must begin with an alpha character.

Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products, so you can get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **documentation@actel.com**.

Online Help

Designer software comes with online help. Online help specific to each software tool is available in available in Libero, Designer, SmartGen, Silicon Explorer II, Silicon Sculptor, and APSW.

1

Setup

This chapter contains information about setting up eProduct Designer to create Actel designs. This includes information about accessing the Actel and migration libraries, setting up eProduct Designer to interface with the Designer Series software, and setting up Actel projects in eProduct Designer. Refer to the Innoveda documentation for additional information about setting up eProduct Designer.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R1-2003 or later and Innoveda eProduct Designer. For specific information about which versions this release supports, go to the Guru automated technical support system on the Actel web site (http://www.actel.com/custsup/search.html) and type the following in the Keyword box:

    third party

Actel Libraries

The Actel libraries contain models for each Actel core in all Actel families for use in ePd. The Actel libraries are sufficient for most cases. Refer to "Migration Libraries" below for exceptions to using the Actel libraries.

Migration Libraries

In addition to the Actel libraries, Actel provides a set of migration libraries. These libraries contain cores supported in earlier versions of the Designer software and cores needed to retarget designs from a different Actel family. If you are upgrading from a previous version of Designer and you have existing Actel designs, you must use the migration libraries. Actel does not recommend using the migration libraries on new designs.

The eProduct Designer software uses a "libs.lst" file to access the Actel libraries. When you install the Designer Series software, a "migrate.lst" file is automatically installed in the "c:\actel\lib\wv" directory. You must use this "migrate.lst" file as your "libs.lst" file to properly access the migration libraries.

To access the migration libraries, perform these steps:

1. (Optional) Create a backup copy of the "libs.lst" in the "c:\ePD\2.0\standard" directory.

2. Delete the "libs.lst" file in the "c:\ePD\2.0\standard" directory.

3. Copy the "migrate.lst" file in the "c:\actel\lib\wv" directory to the "c:\ePD2.0\standard" directory.

4. Rename the "migrate.lst" file as the "libs.lst" file in the "c:\ePD\2.0\standard" directory.

User Setup

Before creating designs, there are some one-time procedures to perform so that the eProduct Designer and Designer Series software can interface properly. This section describes those procedures.

Note: For SmartGen, make sure that environment variable "ePD_root" is set and "c:\ePD\2.0\wv\2000.2\win32\bin" is added to the path.

Actel EDIF Command

To automatically generate an Actel compatible EDIF netlist, add a custom command to the Tools menu in ViewDraw. Once added, this command appears as the Actel EDIF command. The following steps describe the procedure.

1. **Invoke ViewDraw.** If you have not already set up a project, the Project Manager Wizard dialog box is displayed. You must set up an Actel project for ViewDraw to open. Go to "Project Setup" on page 12 for the procedure.

2. **Open the Customize Tools Menu dialog box.** Choose the Customize command from the Tools menu.

3. **Add the Actel EDIF command.** Click the User Menu radio button. In the Menu Text box, type "Actel EDIF." In the Command box, type or use the Browse button to select: "c:\ePD\2.0\wv\1999.2\win32\bin\edifneto.exe." In the Arguments box, type "-L unit -L hard

$BLOCKNAME." Click OK. Figure 1-1 shows the configured Customize Tools Menu dialog box.
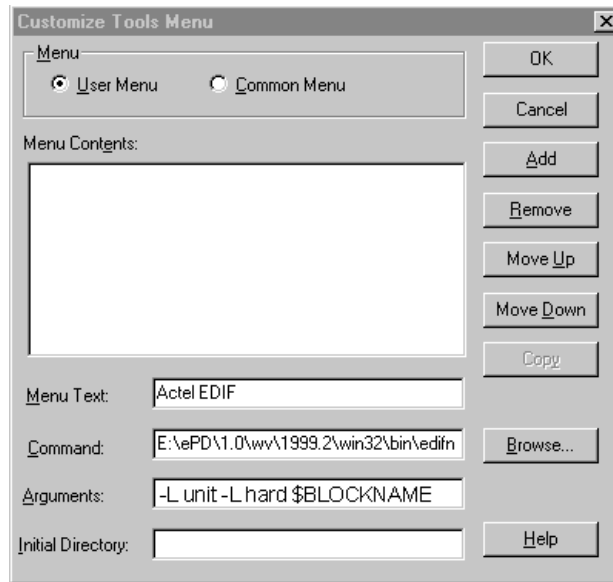

Figure 1-1. Customize Tools Menu Dialog Box

Compiling Actel VITAL Libraries

Before simulating VHDL netlists that reference Actel cores in Speedwave, you must compile Actel VITAL libraries. The following procedures describe the process.

1. **Create a directory called "swave" in the "c:\actel\lib\vtl\95" directory.**

2. **Set your project directory.** Invoke Project Manager and click the New button. Enter "swave" in the Project Name box and "c:\actel\lib\vtl\95\swave" in the Project Directory box. Click the Next button three times, then click the Finish button to complete the process. Do not set your library search order. The New Project Information box appears.

3. **Click the OK button in the New Project Information Dialog Box.**

4. **Save your project and exit Project Manager.**

5. **Open the VHDL Manager.** This displays the HDL Manager dialog box.

6. **Create a <vhd_fam> library.** Choose the Create command from the Library menu. Specify "c:\actel\lib\vtl\95\swave" in the Library Path box and <vhd_fam> in the Symbolic Name box. Click OK.

7. **Add system libraries to search order.** Make sure that the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under the VHDL System Libraries section in the VHDL View window.

8. **Add the Actel VITAL library to the <vhd_fam> library.** Choose the Add Source Files command from the Library menu. Select the <act_fam>.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.

9. **Compile the Actel VITAL library.** Select the <act_fam>.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.

10. **(Optional) Add the Actel VITAL Migration library to the <vhd_fam> library.** Select the <act_fam>_mig.vhd file from the "c:\actel\lib\vtl\95\" directory. Click OK.

11. **(Optional) Compile the Actel VITAL Migration library.** Select the <act_fam>_mig.vhd file in the VHDL View section of the HDL Manager window. Choose the Analyze Source File command from the Analyze menu.

Project Setup

You must set up an Actel project in the eProduct Designer Project Manager for each Actel design before creating your design in eProduct Designer. The following procedures describe the process.

1. **Invoke Dashboard.** From the Start menu, select eProduct Designer and Dashboard to open the Dashboard.

2. **Create or Open a project.** Click the New Project wizard. Choose to create or open a project.

3. **Set the Project Directory.** Type the full path name of your design directory in the Project Directory box or use the Browse button. Type the name of your project in the Project Name box. Click the OK button.

4. **Select an Actel FPGA library.** Choose a library in the Configured FPGA Libraries box. Click the icon of the Actel library you want to select, then click Next.

5. **(Optional) Add additional libraries.** Click the Add button and type the full path name of the library you want to add or use the Browse button.

6. **Click the Finish button in the Creating a New Project box.** The New Project information box appears. Click OK.

Creating a Project Library in SpeedWave

If you use SpeedWave to simulate your designs, you must create a project library in SpeedWave, in addition to creating an Actel project in Project Manager, for each VHDL synthesis-based Actel project. The following procedures describe the process.

1. **Open the VHDL Manager from the simulation toolbox.** This displays the HDL Manager window.

2. **Setup a project.** Choose the Create command from the Library menu. The Create Library dialog box is displayed. Make sure the path in the Library Path box is correct and already exists. Type "user" in the Symbolic Name box and click OK. Make sure the Output window reports no errors in the Output window.

3. **Verify that the "user" library icon appears under the VHDL User Libraries section in the VHDL View window.**

4. **Add the compiled Actel VITAL library to the Project Libraries.** Choose the Add to Workspace command from the Library menu. The Add Existing Library to Workspace dialog box is displayed. Click the ellipsis box to open the Select Directory dialog box. Browse to the "c:\actel\lib\vtl\95\swave\<vhd_fam>.lib" directory and click OK. Click OK again in the Add Existing Library to Workspace dialog box. If you have not compiled the Actel VITAL library, go to "Compiling Actel VITAL Libraries" on page 11 for the procedure.

    Note: Only add the <vhd_fam>.lib if you have referenced Actel cores in your VHDL netlist.

5. **Add system libraries to the Project Libraries.** Make sure the "SYNOPSYS.LIB" and "IEEE.LIB" libraries are listed under VHDL System Libraries in the VHDL View window. If they are not present you must reinstall SpeedWave making sure to choose the Synopsys IEEE libraries when prompted.

6. **Save the project workspace.** Choose the Save command from the File menu.

2

Actel-Innoveda Design Flow

This chapter describes the design flow for creating Actel designs using the eProduct Designer and Designer Series software.

Schematic-Based Design Flow Illustrated

Figure 2-2 shows the schematic-based design flow for creating an Actel device using the eProduct Designer and Designer Series software[1].
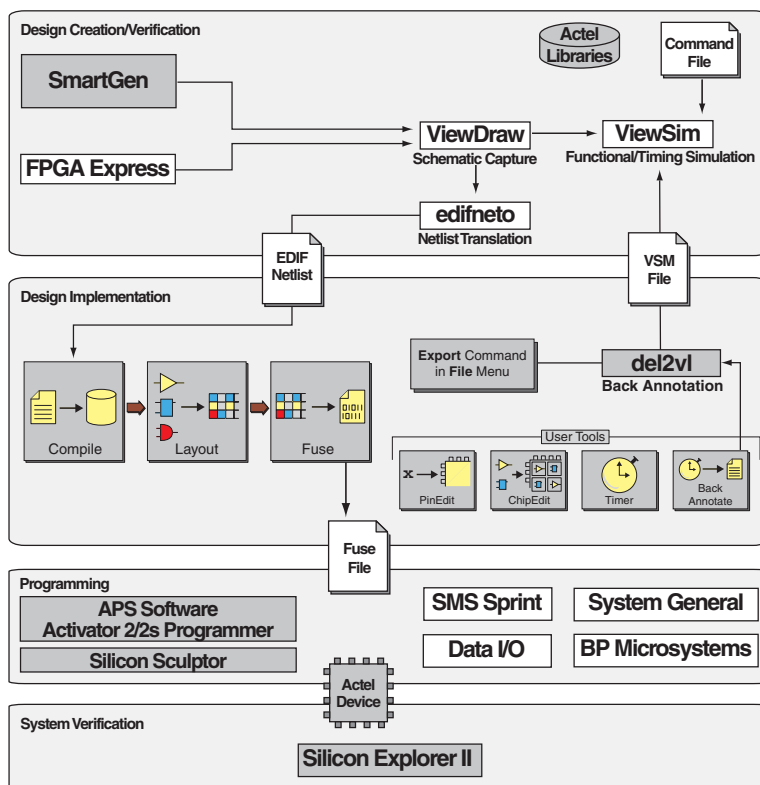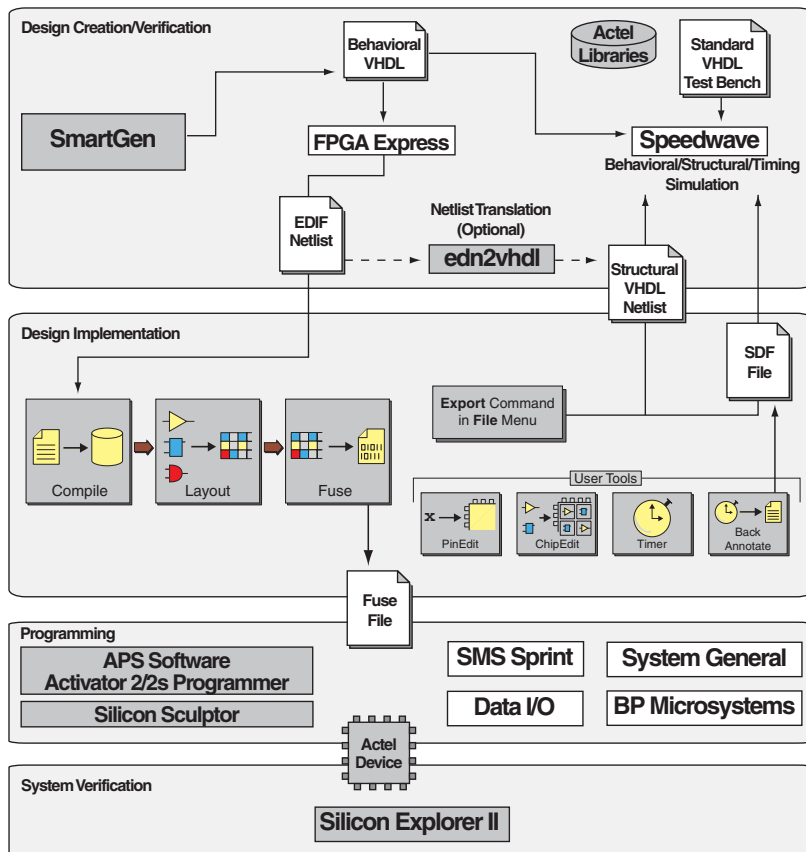

Figure 2-2. Actel-Innoveda Schematic-Based Design Flow

1. The grey boxes in Figure 2–2 denote Actel–specific utilities/tools.

Schematic-Based Design Flow Overview

The Actel-Innoveda schematic-based design flow has four main steps; design creation/verification, design implementation, programming, and system verification. These steps are described in the following sections.

Design Creation/Verification

During design creation/verification, a schematic representation of a design is captured using the eProduct Designer ViewDraw software. After design capture, you can perform a prelayout (functional) simulation with the ePD ViewSim software. Finally, an EDIF netlist is generated for use in Designer.

Schematic Capture

Enter your schematic in ViewDraw. Refer to chapter 3, "Actel-Innoveda Design Considerations" on page 21 and the Innoveda documentation for information about using ViewDraw.

Functional Simulation

Perform a functional simulation of your design using ViewSim before generating an EDIF netlist for place-and-route. Functional simulation verifies that the logic of the design is correct. Unit delays are used for all gates during functional simulation. Refer to "Functional Simulation" on page 27 and the Innoveda documentation for information about performing functional simulation.

EDIF Netlist Generation

After you have captured and verified your design, you must generate an EDIF netlist for place-and-route in Designer. Refer to "Generating an EDIF Netlist" on page 25 for information about generating an EDIF netlist.

Design Implementation

During design implementation, a design is placed-and-routed using Designer. Additionally, you can perform static-timing analysis on a design in Designer with the Timer tool. After place-and-route, perform postlayout (timing) simulation with the eProduct Designer ViewSim software.

Place-and-Route

Use Designer to place-and-route your design. Make sure you specify INNOVEDA as the Edif Flavor and Generic as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designer User's Guide* for information about using Designer.

Static-Timing Analysis

Use the Timer tool in Designer to perform static-timing analysis on your design. Refer to the *Timer User's Guide* for information about using Timer.

Timing Simulation

Perform a timing simulation of your design using ViewSim after placing-and-routing it in Designer. Timing simulation requires information extracted and back annotated from Designer. Refer to "Timing Simulation" on page 27 and the Innoveda documentation for information about performing timing simulation.

Programming

Program a device with programming software and hardware from Actel or a supported third-party programming system. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Silicon Explorer User's Guide* or for information about using the Silicon Explorer.

VHDL Synthesis-Based Design Flow Illustrated

Figure 2-3 shows the VHDL synthesis-based design flow for an Actel device using the eProduct Designer and Designer Series software[1].

Figure 2-3. Actel-Innoveda VHDL Synthesis-Based Design Flow

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1. *The grey boxes in Figure 2–3 denote Actel–specific utilities/tools.*

VHDL Synthesis-Based Design Flow Overview

The Actel-Innoveda VHDL synthesis-based design flow has four main steps; design creation/ verification, design implementation, programming, and system verification. Two verification tools are described, SpeedWave and ViewSim. Use SpeedWave if it is available. It is a VHDL simulator that allows you to perform behavioral, structural, and timing simulation. It also allows you to write stimulus in VHDL. If SpeedWave is not available, use ViewSim for structural and timing simulation. A description of these steps follows.

Design Creation/Verification

During design creation/verification, a design is captured in an RTL-level (behavioral) VHDL source file. After capture of the design, you may perform a behavioral simulation of the VHDL file with SpeedWave to verify that the VHDL code is correct. The code is then synthesized into a structural EDIF netlist using FPGA Express. After synthesis, you can perform a structural simulation of the design with SpeedWave or ViewSim. Import the EDIF netlist into Designer and perform a timing simulation using SpeedWave or ViewSim.

VHDL Design Source Entry

Enter your design source using a text editor or a context-sensitive VHDL editor. Your VHDL design source can contain RTL-level constructs, as well as instantiations of structural elements, such as SmartGen cores.

Behavioral Simulation

If SpeedWave is available, perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your VHDL code. Typically, unit delays are used and a standard VHDL test bench can be used to drive simulation. Refer to "Behavioral Simulation" on page 31 and the Innoveda documentation for information about performing behavioral simulation.

Synthesis

Synthesize your design using FPGA Express. This transforms the behavioral VHDL file into a gate-level EDIF netlist, optimizing the design for a target technology.

Structural VHDL Netlist Generation

If you use SpeedWave for structural and timing simulation, generate a structural VHDL netlist from your EDIF netlist by either exporting it from Designer or by using the Actel "edn2vhdl" program. Refer to "Generating a Structural VHDL Netlist" on page 25 for information about generating a structural netlist.

Structural Simulation

Perform a structural simulation of your design before placing-and-routing it. Structural simulation verifies the functionality of your postsynthesis structural netlist. Unit delays are used for each gate. Refer to "Functional Simulation" on page 27 if using ViewSim or "Structural Simulation" on page 32 if using Speedwave. Also refer to the Innoveda documentation for information about performing structural simulation.

Design Implementation

During design implementation, use Designer to place-and-route a design. Additionally, you can perform static-timing analysis on a design in Designer with the Timer tool. After place-and-route, perform postlayout (timing) simulation with the Innoveda SpeedWave software.

Place-and-Route

Use Designer to place-and-route your design. Make sure to use GENERIC for the Edif flavor when importing the EDIF netlist into Designer. Refer to the *Designer On-line Help* for information about using Designer.

Static-Timing Analysis

Use the Timer tool in Designer to perform static-timing analysis on your design. Refer to the *Timer On-line Help* for information about using Timer.

Timing Simulation

Perform a timing simulation of your design after placing-and-routing it. Timing simulation uses information extracted from Designer, which overrides unit delays in the Actel VHDL. Refer to "Timing Simulation" on page 27 if using Viewsim or "Timing Simulation" on page 33 if using SpeedWave. Also refer to the Innoveda documentation for information about performing timing simulation.

3

Actel-Innoveda Design Considerations

This chapter contains information to assist in creating Actel designs with the Innoveda eProduct Designer software. Topics include naming conventions, adding pins to the schematic, generating a top-level symbol, buried I/Os, adding power and ground, sheets and symbols, assigning pins in a schematic, adding SmartGen cores, adding FPGA Express blocks, generating an EDIF netlist, generating a structural VHDL netlist, using FPGA Express with SpeedWave, and using FPGA Express with ViewSim.

Naming Conventions

Top-level blocks in ViewDraw and FPGA Express must have a design name that follows the DOS file-naming convention (e.g., 8.3 naming convention). The Actel back annotation program can only accept file names that follow this convention.

Use only alphanumeric and underscore "_" characters for schematic net and instance names. Do not use asterisks, forward and backward slashes, spaces, or periods.

Adding Pins to the Schematic

Add pins to the top-level schematic of the design by using the I/O buffer cores with a dangling net attached to the pad, as shown in Figure 3-4. The label on the dangling net becomes the I/O pin name.
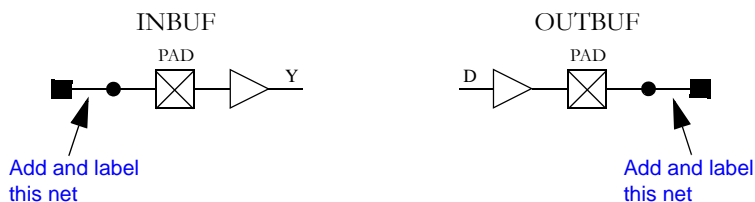
Figure 3-4. Adding Pins to a design

Generating a Top-Level Symbol

When generating a top-level symbol, ViewGen looks for an In or Out port. The convention is illustrated in Figure 3-5. ViewGen does not generate symbols for schematics without IN/OUT ports. The IN/OUT ports are found in the "c:\actel\lib\wv\asicbin" directory.
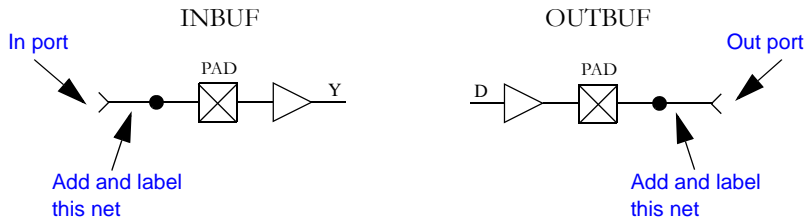
Figure 3-5. Input/Output Ports

Buried I/Os

I/O cores can be buried in the design hierarchy.

Adding Power and Ground

To add power or ground signals in the schematic, use the Actel VCC or GND symbols. You can also label the nets as VDD or GND.

Sheets and Symbols

A multiple-page design is composed of more than one schematic file or <design.n> file in the schematic directory. For a multiple-page design, treat each sheet as part of a top-level schematic and do not consider it a hierarchy level.

Assigning Pins in a Schematic

Nets in your schematic that have the "PIN" attribute assigned to them in ViewDraw are automatically assigned to that pin during design implementation in Designer.

To assign the "PIN" attribute to a net:

1. **Double-click the net to assign pin information.** This displays the Net Properties dialog box.

2. **Select the Attributes Tab.**

3. **Assign the "PIN" attribute to the net.** Type "PIN" in the Name box and the pin number to be assigned in the Value box. Click OK.

Note: This procedure assigns the pin name to the signal net in the netlist. If you use this method to fix pins and you change your pin assignments in PinEdit, you will not be able to back annotate. PinEdit does not change netlist information.

Adding SmartGen Cores

The SmartGen Core Builder can automatically generate symbols that you can add to your schematic. The following steps describe the procedure.

1. **Invoke SmartGen.**

2. **Select the family, core type, and core options.**

3. **Generate your core as a Innoveda symbol.** Make sure that you specify Innoveda as the Netlist/CAE Formats in the Generate dialog box.

4. **Add the core as a component in the schematic.** Refer to the Innoveda documentation for information about adding components to a schematic.

Refer to the *SmartGen On-line Help* for additional information about using SmartGen.

Adding IP cores in a Schematic

VHDL or Verilog cores can be added to the schematic design, without generating any schematics for the core. The following steps describe the procedure.

1. **Generate both EDIF and VHDL netlist for the core using the synthesis tool.**

2. **Invoke EDIF Interface tool.**

3. **Generate wire files for the core using EDIF netlist reader option in the EDIF interface tool.**

4. **Invoke Viewgen.**

5. **Generate top-level symbol for the core using Viewgen tool.**

6. **Invoke Viewdraw.**

7. **Add the core as a component in the schematic.** Add the top-level symbol of the design. Refer to the Innoveda documentation for information about adding the components to a schematic.

8. **Add attributes to the core.** Double click on the component, Component properties dialog box appears, as shown in Fig. 1.

9. **Click Attributes tab of the dialog box.**

10. **Set the following three attributes for this component.** LEVEL: Set this attribute value to VHDL, as core used in this example is a VHDL core. VHDL: Set this value to top level entity name. VHDL_FILE: Set this attribute to, path to the VHD file for the core.

11. **Enter Attributes name in the Name field.**

12. **Enter Attributes value in the Value field.**

13. **Click set to add the attributes.**

14. **Click OK to dismiss the properties dialog box.**

15. **Save check the schematic.**

16. **Generate EDIF netlist for this schematic.** Follow the method shown in ""Generating an EDIF Netlist" on page 25.

17. **Import this netlist into designer.**

Adding FPGA Express Blocks

FPGA Express can generate blocks that can be added to your ViewDraw schematic. The following steps describe the procedure.

1. **Invoke FPGA Express.**

2. **Create a new project or open an existing one.** Add your VHDL source file(s) to the project.

3. **Create an implementation.** In the Create Implementation form, select "Do not insert I/O pads."

4. **Export the Netlist.** In the Export form, select "%s<%d:%d>" for Bus Style and NONE for the Simulation Output Format.

5. **Save the Project and exit FPGA Express.**

6. **Translate the EDIF file into ViewDraw's wir format.** Invoke the EDIF Interfaces program and select the EDIF Netlist Reader tab. Specify the EDIF file created by FPGA Express as the Input and your Innoveda project directory as your Output Dir.

7. **Invoke ViewGen to generate a symbol.** Specify the .wir file generated by the EDIF Netlist Reader as the input. Select "Generate the top level symbol" and optionally, "Generate schematic."

8. **Add the symbol to your ViewDraw schematic.** Refer to the Innoveda documentation for information about adding symbols to a schematic.

Refer to the FPGA Express and other eProduct Designer online help for additional information.

Generating an EDIF Netlist

This section describes the procedures for generating an EDIF netlist for your design. Use the EDIF netlist for place-and-route in Designer.

To generate an EDIF netlist from a schematic-based design:

Select the Actel EDIF command from the Tools menu of ViewDraw. If you have not added the Actel EDIF command to the tools menu in ViewDraw, go to "Actel EDIF Command" on page 10 for the procedure.

To generate an EDIF netlist from a synthesis-based design:

FPGA Express creates an EDIF file that you can import directly into Designer. No special procedure is required.

Generating a Structural VHDL Netlist

You can generate a structural VHDL netlist for SpeedWave simulation from your EDIF netlist by either exporting it from Designer or by using the "edn2vhdl" program. The structural VHDL netlist generated by Designer and the "edn2vhdl" use std_logic for all ports. The bus ports are in the same bit order as they appear in the EDIF netlist.

To generate a structural VHDL netlist using Designer, perform these steps:

1. **Invoke Designer.**

2. **Import the EDIF netlist.** Select the Import Netlist File command from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC (or INNOVEDA if you are using an Innoveda synthesis tool) as the Edif Flavor. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.

3. **Export the structural VHDL netlist.** Select the Export command from the File menu. The Export dialog box is displayed. Specify Netlist File as the File Type and VHDL as the Format. Click OK.

To generate a structural VHDL netlist using edn2vhdl, perform these steps:'

1. **Open a DOS window.**

2. **Change to the directory that contains the EDIF netlist.**

3. **Translate the EDIF netlist to a structural VHDL Netlist.** Type the following command at the prompt:

   ```
   edn2vhdl fam:<act_fam> <design_name>
   ```

Using FPGA Express with SpeedWave

When using FPGA Express with SpeedWave, you do not need to use ViewDraw, ViewSim, ViewGen, or Innoveda EDIF interfaces. You use three point tools: SpeedWave, FPGA Express, and Designer.

1. **Synthesize your design in FPGA Express.** Create or open an existing FPGA Express project. Add your VHDL source file(s) to the project.

2. **In the Create Implementation dialog box, be sure that the "Do not insert I/O pads" checkbox is not selected.**

3. **In the Export dialog box, select "%s<%d:%d>" for Bus Style and NONE for the Simulation Output Format.** An EDIF netlist is exported by FPGA Express.

Using FPGA Express with ViewSim

When using FPGA Express with ViewSim, you cannot perform a behavioral simulation. You need to import the synthesized design into the ViewDraw/ViewSim environment.

1. **Synthesize your design in FPGA Express.** Create or open an existing FPGA Express project. Add your VHDL source file(s) to the project.

2. **In the Create Implementation form, make sure that the "Do not insert I/O pads" checkbox is not selected.**

3. **In the Export dialog box, select "%s<%d:%d>" for Bus Style and NONE for the Simulation Output Format.** FPGA Express exports an EDIF netlist.

4. **Import the synthesized EDIF into the ViewDraw/ViewSim environment.** Invoke the EDIF Interfaces program and select the EDIF Netlist Reader tab. Specify the EDIF file created by FPGA Express as the Input and your Innoveda project directory as your Output Dir.

4

Simulation Using ViewSim

This chapter describes the procedures for performing functional and timing simulations of an Actel design using the Innoveda ViewSim simulation tool.

Note: ViewSim not supported in A500k, APA, and Ax devices.

Functional Simulation

Use the following procedure to perform a functional simulation of an Actel design:

1. **Select your Actel project in the Dashboard.** If you have not created or setup your project, go to "Project Setup" on page 12 for the procedure.

2. **Open the ViewSim Wirelister dialog box.** Invoke ViewVSM or, from ViewDraw, choose the Create Digital Netlist command from the Tools menu.

3. **Generate a simulation (.vsm) wirelist.** Type in the design name or use the Browse button. Click OK. A simulation wirelist is generated and the eProduct Designer window is displayed.

4. **Simulate the design.** Invoke ViewSim. Type in the design name in the Design Name box and click OK.

Refer to the Innoveda documentation for additional information about performing simulation with ViewSim.

Timing Simulation

ViewSim timing simulation is no longer supported by Actel since the Innoveda back-annotate feature is not available in the Actel Designer software any more. To perform timing simulation:

1. **Export a VHDL or Verilog nelist and *.sdf file from the Actel Designer software**

2. **Use the HDL netlist and *.sdf file to run timing simulation in other HDL based simulators**

Multichip Simulation

System designs are typically divided into functional modules implemented by several Actel devices. To check the functionality of the system, you must simulate all Actel devices together. You can use ViewSim and Designer to perform multichip simulation. Use the following procedure to perform a multichip simulation of an Actel design:

Note: Because the viewdraw.ini file uses the same alias for all Actel families, you can only simulate multiple Actel devices of the same family.

1. **Create a top-level schematic and instantiate the individual chip designs.** This example assumes there are three designs with instance names "chip1," "chip2," and "chip3." The name of the top-level schematic is "top." Figure 4-6 depicts the directory structure for this example. Names written in normal text represent file names and those in bold text represent directory names.
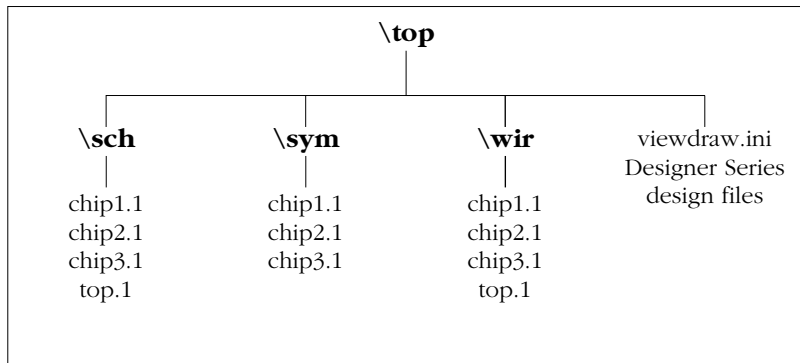
Figure 4-6. Directory Structure for Multichip Simulation

Note: This example only contains single-sheet schematics for each design. Similar procedures apply to multiple-sheet designs.

2. **Place-and-route your design in Designer.** Refer to the Using Designer Guide for information about using Designer.

3. **Extract timing information for your design.** From the File menu, select Export > Timing Files. Choose the format (SDF is most common), name your file <design_name>.SDF, and click Save to continue.

4. **Back annotate your delays.** Click the back annotate button in the Designer menu. The Open dialog box is displayed. Select the "chip1.sdf" file and click OK to generate the "chip1.dtb" file. Repeat for the "chip2.dtb" and "chip3.dtb" files.

5. **Generate a "top.dtb" file for the top-level schematic.** The top-level DTB file includes the following lines:

```
.ba
c chip1
a dtb=chip1.dtb
c chip2
a dtb=chip2.dtb
c chip3
a dtb=chip3.dtb
.ab
```

The "c" line above specifies an instance name, "chip1." If you have not labeled an instance, use the default handle name of an instance, "$1I38" as it appears in your top-level schematic. Also, the individual DTB files reside in the top-level design directory, "top."

6. **Run ViewVSM on "top.dtb."** Reference the "top.dtb" file in the VSM pop-up dialog box. The VSM program processes the DTB files for each chip and creates the "top.vsm" file with back-annotated postlayout timing delays.

7. **Simulate "top.vsm."** Invoke ViewSim. Type "top.vsm" in the Design Name box and click OK.

Refer to the Innoveda documentation for additional information about performing simulation with ViewSim.

5

Simulation Using SpeedWave

This chapter describes the procedures for performing behavioral, structural, and timing simulations of an Actel design using the Innoveda SpeedWave simulation tool.

Behavioral Simulation

Use the following procedures to perform a behavioral simulation of an Actel design. Refer to the Innoveda documentation for additional information about performing simulation with SpeedWave:

1. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup" on page 12 for the procedure.

2. **Open the HDL Manager.** This displays the HDL manager dialog box.

3. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select an .hws file and click the Open button in the Open dialog box.

4. **Analyze your behavioral VHDL design files and testbench.** Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Assign Source Files dialog box is displayed. Select the behavioral VHDL and testbench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

    Note: SpeedWave can only simulate configurations. You must have at least one configuration in your testbench.

5. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double-click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

6. **Simulate your design.** Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Structural Simulation

Use the following procedures to perform a structural simulation of an Actel design. Refer to the Innoveda documentation for additional information about performing simulation with SpeedWave.

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.

2. **Select your Actel project in Project Manager.** If you have not created your project, go to "Project Setup" on page 12 for the procedure.

3. **Open the HDL Manager.** This displays the HDL manager dialog box.

4. **Open a project HDL workspace (.hws) file.** Choose the Open command from the File menu. Select an .hws file and click the Open button in the Open dialog box.

5. **Analyze your structural VHDL netlist and testbench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 25 for the procedure. Select the user library icon in the VHDL User Libraries section of the VHDL View window. Choose the Add Source Files command from the Library menu. The Assign Source Files dialog box is displayed. Select the structural VHDL netlist and testbench files from the VHDL Source File Name window and click OK. Select each file and choose the Analyze Source File command from the Analyze menu. Check the Output window for successful completion. Save the HDL workspace and close the HDL Manager window.

   Note: SpeedWave can only simulate configurations. You must have at least one configuration in your testbench.

6. **Select a configuration to simulate.** Choose the Load Design command from the File menu. Double-click "user.lib" and select the configuration you want to simulate. Click OK. A Source Viewer window and a Hierarchy Viewer window are displayed.

7. **Simulate your design.** Choose the Run Simulation command from the Simulate menu. The Run Simulation dialog box is displayed. Select the desired options and click the Apply button. Click the Close button when you have completed your simulation.

Timing Simulation

SpeedWave timing simulation is no longer supported by Actel. To perform timing simulation:

1. Export a VHDL or Verilog netlist and *.sdf file from Actel Designer software

2. Use the HDL netlist and *.sdf file to run timing simulation in other HDL based simulators

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0)1276.401500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support (http://www.actel.com/kb/search.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

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