# *Innoveda eProduct Designer*

*Interface Guide*

Actel

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## Trademarks

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# Introduction

The *Mentor Graphics eProduct Designer Interface Guide* contains information about using the Innoveda eProduct Designer CAE software tools with the Actel Designer Series FPGA development software tools to create designs for Actel devices. Refer to the *Designer User's Guide* for additional information about using the Designer series software and the Innoveda documentation for additional information about using the Powerview software.

## Document Organization

The *Innoveda eProduct Designer Interface Guide* contains the following chapters:

**Chapter 1 - Setup** contains information about setting up the Powerview software for use in creating Actel designs.

**Chapter 2 - Actel-Mentor Graphics Design Flow** describes the design flow for creating Actel designs using the Powerview and Designer Series software.

**Chapter 3 - Actel-Mentor Graphics ePd Design Considerations** contains information to assist in creating Actel designs with the Powerview and Designer Series software.

**Chapter 4 - Simulation Using ViewSim®** contains information about simulating Actel designs with ViewSim.

**Chapter 5 - Simulation Using SpeedWave™** contains information about simulating Actel designs with SpeedWave.

**Appendix A - Product Support** provides information about contacting Actel for customer and technical support.

## Document Assumptions

This document assumes the following:

1. You have installed the Designer Series software.
2. You have installed the Powerview software.
3. You are familiar with UNIX workstations and operating systems.
4. You are familiar with FPGA architecture and FPGA design software.

# Document Conventions

This document uses the following conventions:

Information input by the user follows this format:

```
keyboard input
```

The contents of a file follows this format:

```
file contents
```

This document uses the following variables:

- Actel FPGA family libraries are shown as <act_fam>. Substitute the desired Actel FPGA family Fusion, IGLOO™/e, ProASIC3/E, ACT1, ACT2 (for ACT 2 and 1200XL devices), ACT3, 3200DX, MX, SX, SX-A, eX, Axcelerator, A500k, and APA as needed. For example:

  ```
  edn2vhdl fam:<act_fam> <design_name>
  ```

- Compiled VHDL libraries are shown as <vhd_fam>. Substitute <vhd_fam> for the desired VHDL family Fusion, IGLOO/e, ProASIC3/E, ACT1, ACT2 (for ACT 2 and 1200XL devices), ACT3, A3200DX, MX, SX, SX-A, eX, Axcelerator, A500k, and APA as needed. The VHDL language requires that the library names begin with an alpha character.

# Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products, so you can get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **documentation@actel.com**.

# 1 Setup

This chapter contains information about setting up the Powerview software to create designs for Actel devices. Refer to the Innoveda documentation for additional information about setting up Powerview.

## Software Requirements

The information in this guide applies to the Actel Designer Series software release R1-2003 or later and Mentor Graphics eProduct Designer. For specific information about which versions this release supports, go to the Guru automated technical support system on the Actel web site (http://www.actel.com/custsup/search.html) and type the following in the Keyword box:

```
third party
```

## System Setup

After installing Powerview, make sure you set the proper environment variables in your UNIX shell script. The following are C-shell variables. If you are using another shell, adjust the syntax accordingly.

```
setenv WORKVIEWHOME <ePD_install_directory>
setenv ALSDIR <actel_install_directory>
setenv WDIR <powerview_install_directory>
set path=($ALSDIR/bin $path)
set path=($WORKVIEWHOME/bin $path)
```

For example:

```
WORKVIEWHOME/ax_1/viewlogic/ePD10/epd/I-O/common/sun05551
```

If you use SunOS or Solaris, you must also set the following variable:

```
setenv LD_LIBRARY_PATH $ALSDIR/lib
```

If you use HP-UX, you must also set the following variable:

```
setenv SHLIB_PATH $ALSDIR/lib
```

If you use SpeedWave, you must also set the following variable:

```
setenv VANTAGE_VSS <vantage_install_directory>
```

Refer to the *Designer User's Guide* and the Innoveda documentation for additional information about setting environment variables.

## Actel EDIF Command

To automatically generate an Actel compatible EDIF netlist, add a custom command to the Tools menu in ViewDraw. Once added, this command appears as the Actel EDIF command. The following steps describe the procedure.

1. **Invoke ViewDraw.** If you have not already set up a project, the Project Manager Wizard dialog box is displayed. You must set up an Actel project for ViewDraw to open. Go to "Project Setup" on page 11 for the procedure.
2. **Open the Customize Tools Menu dialog box.** Choose the Customize command from the Tools menu.
3. **Add the Actel EDIF command.** Click the User Menu radio button. In the Menu Text box, type "Actel EDIF." In the Command box, type or use the Browse button to select: "c:\ePD\2.0\wv\1999.2\win32\bin\edifneto.exe." In the Arguments box, type "-L unit -L hard $BLOCKNAME." Click OK. Figure 1-1 shows the configured Customize Tools Menu dialog box.

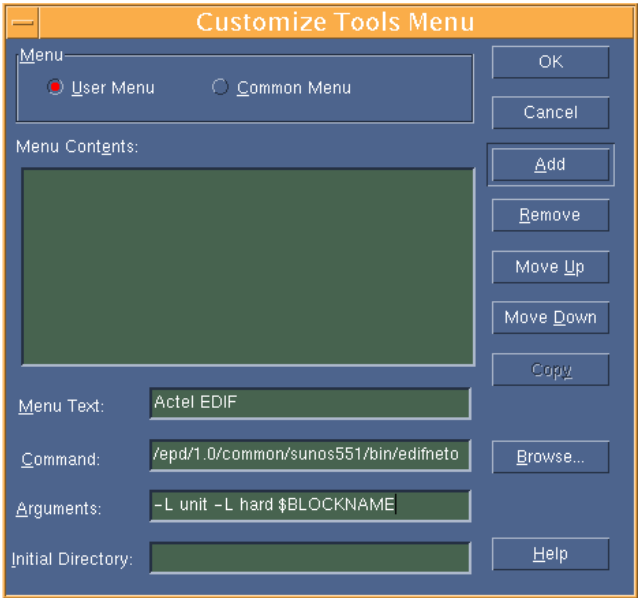


Figure 1-1. Customize Tools Menu Dialog Box

# Actel Libraries

The Actel libraries contain models for each Actel core in all Actel families for use in Innoveda. The Actel libraries are sufficient for most cases. Refer to "Migration Libraries" on page 9 for exceptions to using the Actel libraries.

The Powerview software uses a "viewdraw.ini" file to access the Actel libraries. Actel has provided template "viewdraw.ini" files in the "$ALSDIR/lib/wv/<act_fam>" directories that you can use. If you manually add the paths, they must be the first paths specified in the directories section of your "viewdraw.ini" file.

### *To access the Actel libraries,*

add the following lines to your "viewdraw.ini" file:

```
dir [p] .
dir [rm] $ALSDIR/lib/wv/<act_fam>/cells (ACTELCELLS)
dir [rm] $ALSDIR/lib/wv/smartgen (SMARTGEN)
dir [rm] $ALSDIR/lib/wv/sim (ACTELSIM)
dir [rm] $WDIR/lib/builtin (builtin)
```

For example, to configure Powerview to use the ACT3 family library, replace "<act_fam>" with "act3" in the lines above.

# Migration Libraries

In addition to the Actel libraries, Actel provides a set of migration libraries. These libraries contain cores supported in earlier versions of the Designer Series software and cores possibly needed to retarget designs from a different Actel family. If you are upgrading from a previous version of Designer and you have existing Actel designs, you must use the migration libraries. Actel does not recommend using the migration libraries on new designs.

The Powerview software uses a "viewdraw.ini" file to access the Actel libraries. Actel has provided template "viewdraw.ini" files in the "$ALSDIR/lib/wv/<act_fam>" directories that you can use. If you manually add the paths, they must be the first paths specified in the directories section of your "viewdraw.ini" file.

### *To access the migration libraries,*

add the following lines to your "viewdraw.ini" file:

```
dir [p] .
dir [rm] $ALSDIR/lib/wv/<act_fam>/cells (ACTELCELLS)
dir [rm] $ALSDIR/lib/wv/<act_fam>/migrate (ACTELCELLS)
dir [rm] $ALSDIR/lib/wv/<act_fam>/migrate (ACTELMIGRATE)
```

```
dir [rm] $ALSDIR/lib/wv/<act_fam>/migrate (ACTELMODELS)
dir [rm] $ALSDIR/lib/wv/smartgen (SMARTGEN)
dir [rm] $ALSDIR/lib/wv/sim (ACTELSIM)
dir [rm] $WDIR/lib/builtin (builtin)
```

For example, to configure Powerview to use the ACT3 family library, replace "<act_fam>" with "act3" in the lines above.

# Compiling Actel VITAL Libraries

Before simulating VHDL netlists that reference Actel cores in SpeedWave, you must compile Actel VITAL libraries. Use the following procedure to compile an Actel VITAL library.

1. **Create a directory called "swave" in the "/$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "/$ALSDIR/lib/vtl/95/swave" directory.**
3. **Create and map the library directory for your simulator.** Compiled VITAL library names must begin with an alpha character. Type the following command at the prompt:

   ```
   vanlibcreate $ALSDIR/lib/vtl/95/swave/<vhd_fam> <vhd_fam>
   ```

   For example, to create and map the 40MX library for your simulator, type the following command:

   ```
   vanlibcreate $ALSDIR/lib/vtl/95/swave/a40mx a40mx
   ```

4. **Compile the library.** Compiled VITAL library names must begin with an alpha character. Type the following command at the prompt:

   ```
   analyze -src ../<act_fam>.vhd -lib <vhd_fam> -libieee -lib
   $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

   For example, to compile the 40MX library, type the following command:

   ```
   analyze -src ../40mx.vhd -lib a40mx -libieee -lib$VANTAGE_VSS/pgm/lib/
   synopsys.lib
   ```

5. **(Optional) Compile the migration library.** If you are using the migration library, type the following command at the prompt:

   ```
   analyze -src ../<act_fam>_mig.vhd -lib <vhd_fam> -libieee
   -lib $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

   For example, to compile the 40MX migration library, type the following command:

```
analyze -src ../40mx_mig.vhd -lib a40mx -libieee -lib$VANTAGE_VSS/pgm/
lib/synopsys.lib
```

# Project Setup

You must set up an Actel project in the eProduct Designer Project Manager for each Actel design before creating your design in eProduct Designer. The following procedures describe the process.

1. **Invoke Dashboard.** From the Start menu, select eProduct Designer and Dashboard to open the Dashboard.
2. **Create or Open a project.** Click the New Project wizard. Choose to create or open a project.
3. **Set the Project Directory.** Type the full path name of your design directory in the Project Directory box or use the Browse button. Type the name of your project in the Project Name box. Click the OK button.
4. **Select an Actel FPGA library.** Choose a library in the Configured FPGA Libraries box. Click the icon of the Actel library you want to select, then click Next.
5. **(Optional) Add additional libraries.** Click the Add button and type the full path name of the library you want to add or use the Browse button.
6. **Click the Finish button in the Creating a New Project box.** The New Project information box appears. Click OK.

# 2

# Actel-Mentor Graphics Design Flow

This chapter describes the design flow for creating Actel designs using the Powerview and Designer Series software.

## Schematic-Based Design Flow Illustrated

Figure 2-2 shows the schematic-based design flow for creating an Actel device using the Powerview and Designer Series software[1].

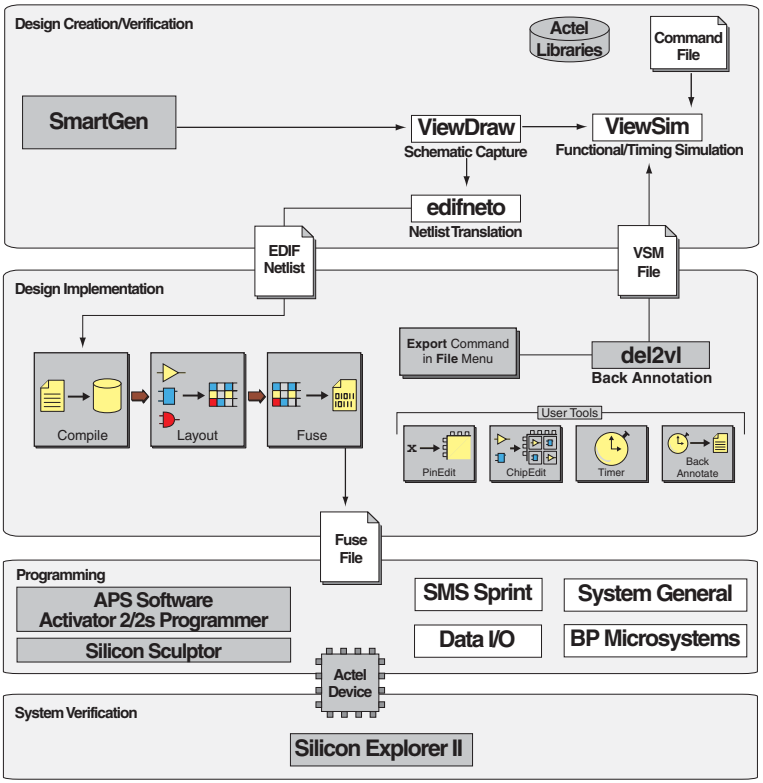


Figure 2-2. Actel-Innoveda Schematic-Based Design Flow

*1. The grey boxes in Figure 2-2 denote Actel-specific utilities/tools.*

# Schematic-Based Design Flow Overview

The Actel-Innoveda schematic-based design flow has four main steps:

1. Design Creation/Verification
2. Design Implementation
3. Programming
4. System Verification

The following sections describe these steps.

## Design Creation/Verification

During design creation/verification, you capture a schematic representation of a design using the Innoveda ViewDraw software. After design capture, you can perform a prelayout (functional) simulation with the Innoveda ViewSim software. Finally, you generate an EDIF netlist for use in Designer.

### Schematic Capture

Enter your schematic in ViewDraw. Refer to chapter 3, "Actel-Mentor Graphics ePd Design Considerations" on page 19 and the Innoveda documentation for information about using ViewDraw.

### Functional Simulation

Perform a functional simulation of your design using ViewSim before generating a netlist for place-and-route. Functional simulation verifies that the logic of the design is correct. Unit delays are used for all gates during functional simulation. Refer to "Functional Simulation" on page 23 and the Innoveda documentation for information about performing functional simulation.

Note: Functional simulation is not supported for A500K, APA, and AX devices.

### EDIF Netlist Generation

After you have captured and verified your design, you must generate an EDIF netlist for place-and-route in Designer. Refer to "Generating an EDIF Netlist" on page 21 for information about generating an EDIF netlist.

## Design Implementation

During design implementation, you place-and-route a design using Designer. Additionally, you can perform static-timing analysis on a design in Designer with the Timer tool. After place-and-route, you perform postlayout (timing) simulation with the Innoveda ViewSim software.

### Place-and-Route

Use Designer to place-and-route your design. Make sure you specify Innoveda as the Edif Flavor and Generic as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designer User's Guide* for information about using Designer.

### Static-Timing Analysis

Use the Timer tool in Designer to perform static-timing analysis on your design. Refer to the *Timer User's Guide* for information about using Timer.

### Timing Simulation

Perform a timing simulation of your design using ViewSim after placing-and-routing it in Designer. Timing simulation requires information extracted and back annotated from Designer. Refer to "Timing Simulation" on page 23 and the Innoveda documentation for information about performing timing simulation.

## Programming

Program a device with programming software and hardware from Actel or a supported third-party programming system. Refer to the *Silicon Sculptor User's Guide* or the *FlashPro User's Guide* for information about programming an Actel device.

## System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Silicon Explorer User's Guide* for information about using the Silicon Explorer.

# VHDL Synthesis-Based Design Flow Illustrated

Figure 2-3 shows the VHDL synthesis-based design flow for an Actel device using the Powerview and Designer Series software[1].

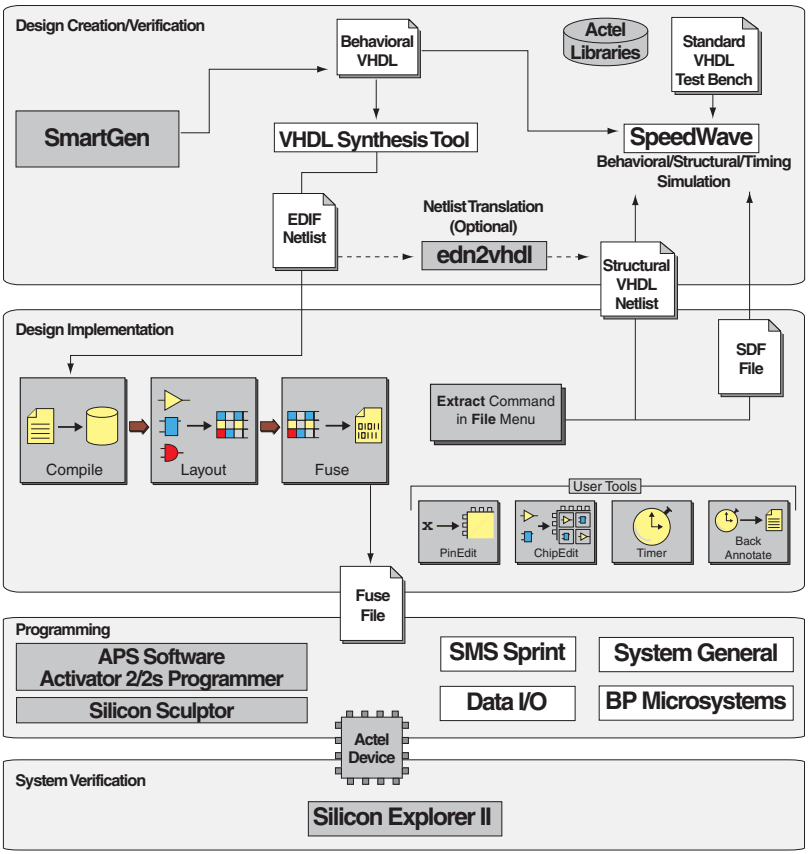


Figure 2-3. Actel-Innoveda VHDL Synthesis-Based Design Flow

*1. The grey boxes in Figure 2-3 denote Actel-specific utilities/tools.*

# VHDL Synthesis-Based Design Flow Overview

The Actel-Innoveda VHDL synthesis-based design flow has four main steps:

1. Design Creation/Verification
2. Design Implementation
3. Programming
4. System Verification

The following sections describe these steps.

## Design Creation/Verification

During design creation/verification, you capture a design in an RTL-level (behavioral) VHDL source file. After capturing the design, you can perform a behavioral simulation of the VHDL file with the Innoveda SpeedWave software to verify that the VHDL code is correct. You then synthesize the code into a structural VHDL netlist. After synthesis, you can perform a structural simulation of the design. Finally, you generate an EDIF netlist for use in Designer and a VHDL structural netlist for structural and timing simulation in SpeedWave.

### VHDL Design Source Entry

Enter your design source using a text editor or a context-sensitive VHDL editor. Your VHDL design source can contain RTL-level constructs, as well as instantiations of structural elements, such as SmartGen cores.

### Behavioral Simulation

Perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your VHDL code. Typically, you use unit delays and a standard VHDL testbench to drive simulation. Refer to "Behavioral Simulation" on page 27 and the Innoveda documentation for information about performing behavioral simulation.

### Synthesis

After you have created your behavioral VHDL source file, you must synthesize it before placing-and-routing it in Designer. Synthesis transforms the behavioral VHDL file into a gate-level netlist and optimizes the design for a target technology. Refer to the documentation included with your synthesis tool for information about performing design synthesis.

### Netlist Generation

After you have created, synthesized, and verified your design, generate a netlist for place-and-route in Designer. The netlist is also used to generate a structural VHDL netlist. Refer to "Generating an EDIF Netlist" on page 21 for information about generating an EDIF Netlist.

### Structural VHDL Netlist Generation

Generate a structural VHDL netlist from your EDIF netlist for use in structural and timing simulation by either exporting it from Designer or by using the Actel "edn2vhdl" program. Refer to "Generating a Structural VHDL Netlist" on page 21 for information about generating a structural VHDL netlist.

### Structural Simulation

Perform a structural simulation of your design before placing-and-routing it. Structural simulation verifies the functionality of your postsynthesis structural VHDL netlist. Unit delays included in the compiled Actel VHDL libraries are used for every gate. Refer to "Structural Simulation" on page 28 and the Innoveda documentation for information about performing structural simulation.

## Design Implementation

During design implementation, you place-and-route a design using Designer. Additionally, you perform static-timing analysis on a design in Designer with the Timer tool. After place-and-route, you perform postlayout (timing) simulation with the Innoveda SpeedWave software.

### Place-and-Route

Use Designer to place-and-route your design. Make sure to specify GENERIC (or Innoveda if you are using a Innoveda synthesis tool) as the Edif Flavor and VHDL as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designer User's Guide* for information about using Designer.

### Static-Timing Analysis

Use the Timer tool in Designer to perform static-timing analysis of your design. Refer to the *Timer User's Guide* manual for information about using Timer.

### Timing Simulation

Perform a timing simulation of your design after placing-and-routing it. Timing simulation requires information extracted from Designer, which overrides unit delays in the compiled Actel VHDL libraries. Refer to "Timing Simulation" on page 29 and the Innoveda documentation for information about performing timing simulation.

# 3

# Actel-Mentor Graphics ePd Design Considerations

This chapter contains information to assist in creating Actel designs with Innoveda eProduct Designer software. This includes schematic design considerations and netlist generation procedures.

## Schematic Naming Conventions

Use only alphanumeric and underscore "_" character for schematic net and instance names. Do not use asterisks, forward and backward slashes, spaces, or periods.

## Adding Power and Ground

To add power or ground signals in the schematic, use the Actel VCC or GND symbols. You can also label the nets as VDD or GND.

## Adding Pins to the Design

Add pins to the top-level schematic of the design by using the I/O buffer cores with a dangling net attached to the pad, as shown in Figure 3-4. The label on the dangling net becomes the I/O pin name.

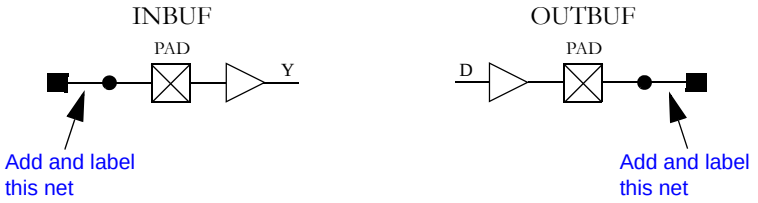


Figure 3-4. Adding Pins to a design

# Generating a Top-Level Symbol

When generating a top-level symbol, ViewGen looks for an In or Out port. The convention is illustrated in Figure 3-5. ViewGen does not generate symbols for schematics without IN/OUT ports. The IN/OUT ports are in the "$ALSDIR/lib/wv/asicbin" directory.

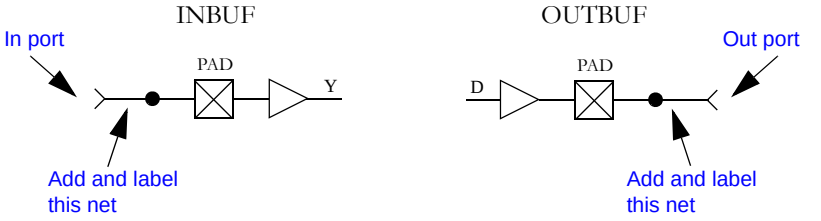


Figure 3-5. Input/Output Ports

# Buried I/O cores

You can bury I/O cores in the design hierarchy.

# Sheets and Symbols

A multiple-page design is composed of more than one schematic file or <design>.n file in the schematic directory. For a multiple-page design, treat each sheet as a part of a top-level schematic and do not consider it a hierarchy level.

# Assigning Pins in a Schematic

Nets in your schematic that have the "PIN" attribute assigned to them in ViewDraw are automatically assigned to that pin during design implementation in Designer.

### *To assign the "PIN" attribute to a net in ViewDraw,*

1. **Select the net to assign pin information.**
2. **Add a Pin attribute to the net.** Select the Attr command from the Add menu. The Add Attribute dialog box is displayed. Type the following in the Attribute box:

   ```
   pin=<valid_pin_number>
   ```

   Click OK.

Note: This procedure assigns the pin name to the signal net in the netlist. If you use this method to fix pins and you change your pin assignments in PinEdit, you will not be able to back annotate. PinEdit does not change netlist information.

# Adding SmartGen Cores

The SmartGen Core Builder can automatically generate symbols that you can add to your schematic. The following steps describe the procedure.

1. **Invoke SmartGen.**
2. **Select the family, core type, and core options.**
3. **Generate your core as a Innoveda symbol.** Make sure that you specify Innoveda as the Netlist/CAE Formats in the Generate dialog box.
4. **Add the core as a component in the schematic.** Refer to the Innoveda documentation for information about adding components to a schematic.

Refer to the SmartGen online help for additional information about using SmartGen.

# Generating an EDIF Netlist

This section describes the procedures for generating an EDIF netlist for your design. Use the EDIF netlist for place-and-route in Designer.

### *To generate an EDIF netlist from a schematic-based design:*

Select the Actel EDIF command from the Tools menu of ViewDraw. If you have not added the Actel EDIF command to the tools menu in ViewDraw, go to "Actel EDIF Command" on page 8 for the procedure.

### *To generate an EDIF netlist from a synthesis-based design:*

FPGA Express creates an EDIF file that you can import directly into Designer. No special procedure is required.

# Generating a Structural VHDL Netlist

You can generate a structural VHDL netlist from your EDIF netlist by either exporting it from Designer or by using the "edn2vhdl" program. The structural VHDL netlist generated by Designer and the "edn2vhdl" use std_logic for all ports. The bus ports are in the same bit order as they appear in the EDIF netlist.

### *To generate a structural VHDL netlist using Designer,*

1. **Invoke Designer.**
2. **Import your EDIF netlist.** Select the Import Netlist command from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC (or Innoveda if you are using a Innoveda synthesis tool) as the Edif Flavor, and VHDL as the Naming Style. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.
3. **Export a structural VHDL netlist.** Select the Export command from the File menu. The Export dialog box is displayed. Specify Netlist File as the File Type and VHDL as the Format. Click OK.

### *To generate a structural VHDL netlist using edn2vhdl,*

1. **Change to the directory that contains the EDIF netlist.**
2. **Type the following command at the prompt:**

```
edn2vhdl fam:<act_fam> <design_name>
```

# 4

# Simulation Using ViewSim®

This chapter describes the procedures for performing functional and timing simulations of your Actel design using the Innoveda ViewSim simulation tool.

Note: ViewSim will not be supported in future releases of Designer. A500K, APA, and AX devices are not supported at this time.

## Functional Simulation

Use the following procedure to perform a functional simulation of an Actel design:

1. **Select your Actel project in the Dashboard.** If you have not created or setup your project, go to "Project Setup" on page 11 for the procedure.
2. **Open the ViewSim Wirelister dialog box.** Invoke ViewVSM or, from ViewDraw, choose the Create Digital Netlist command from the Tools menu.
3. **Generate a simulation (.vsm) wirelist.** Type in the design name or use the Browse button. Click OK. A simulation wirelist is generated and the eProduct Designer window is displayed.
4. **Simulate the design.** Invoke ViewSim. Type in the design name in the Design Name box and click OK.

Refer to the Innoveda documentation for additional information about performing simulation with ViewSim.

## Timing Simulation

ViewSim timing simulation is no longer supported by Actel since the Innoveda back-annotate feature is not available in Actel Designer software anymore. To perform timing simulation:

1. Export a VHDL or Verilog netlist and *.sdf file from Actel Designer software.
2. Use the HDL netlist and *.sdf file to run timing simulation in other HDL based simulators.

## Multichip Simulation

System designs are typically divided into functional modules, which several Actel devices implement. To check the functionality of the system, you must simulate all Actel devices together. You can use ViewSim and Designer to perform multichip simulation. Use the following procedure to perform a multichip simulation of an Actel design:

Note: Because the viewdraw.ini file uses the same alias for all Actel families, you can only simulate multiple Actel devices of the same family.

1. **Create a top-level schematic and instantiate the individual chip designs.** This example assumes there are three designs with instance names “chip1,” “chip2,” and “chip3.” The name of the top-level schematic is “top.” Figure 4-6 depicts the directory structure for this example. Names written in normal text represent file names and those in bold text represent directory names.

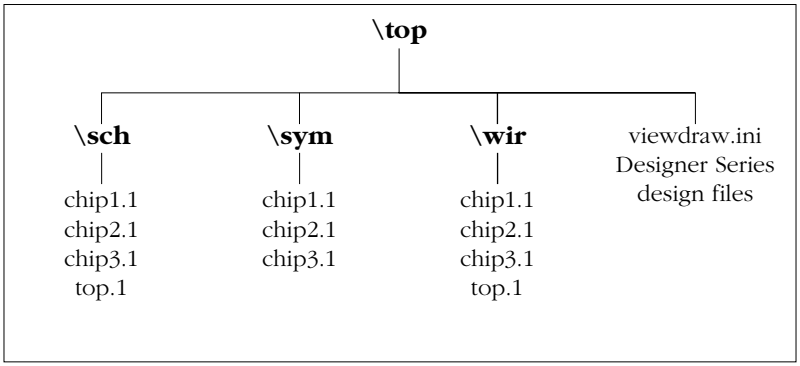


Figure 4-6. Directory Structure for Multichip Simulation

Note: This example only contains single-sheet schematics for each design. Similar procedures apply to multiple-sheet designs.

1. **Place-and-route your design in Designer.** Refer to the Designer User’s Guide for information about using Designer.
2. **Extract timing information for your design.** Choose the Export command from the File menu or click Back Annotate. The back-annotate dialog box is displayed. Create a “chip1.sdf” file by choosing the GENERIC option from the CAE pull-down menu. Click OK. Repeat for “chip2.sdf” and “chip3.sdf.”
3. **Back annotate your delays.** Make sure you are in the “\top” directory and type the following command at the prompt:

   ```
   del2vl chip1
   ```

   The application reads the “chip1.sdf” file and generates a “chip1.dtb” file and a “chip1.vsm” file. Repeat for the “chip2.sdf” and “chip3.sdf” files.
4. **Create a “top.dtb” file for the top-level schematic.** The top-level DTB file should include the following lines:

   ```
   .ba
   c chip1
   a dtb=chip1.dtb
   c chip2
   ```

```
a dtb=chip2.dtb
c chip3
a dtb=chip3.dtb
.ab
```

The "c" lines above specify instance names, such as "chip1." If you have not labeled an instance, you can use the default handle name of an instance, "$1I38" as it appears in your top-level schematic. Also, the individual DTB files should reside in the top-level design directory, "top."

5. **Run ViewVSM on "top.dtb."** Reference the "top.dtb" file in the VSM pop-up dialog box. The VSM program processes the DTB files for each chip and creates the "top.vsm" file with back-annotated postlayout timing delays.
6. **Simulate "top.vsm."** Invoke ViewSim from the Dashboard. Type "top.vsm" in the Design Name box and click OK.

Refer to the Innoveda documentation for additional information about performing simulation with ViewSim.

# 5

# Simulation Using SpeedWave™

This chapter describes the procedures for performing simulations on an Actel design using the Innoveda SpeedWave simulation tool.

## Behavioral Simulation

Use the following procedure to perform a behavioral simulation of an Actel design:

Note: When installing the Innoveda SpeedWave simulator, you have the option of installing a standard IEEE library or the Synopsys version.You must install the Synopsys libraries for compatibility with Actel VITAL libraries and you must include the Synopsys library in your invocations. The commands in this guide use the Synopsys version of the IEEE libraries.

1. **Create a working directory.** Type the following command at the prompt:

   ```
   vanlibcreate ./user.lib user
   ```

2. **Create a soft link to the synthesis library.** Type the following command at the prompt:

   ```
   ln -s $VANTAGE_VSS/pgm/libs/synopsys.lib synopsys
   ```

3. **Analyze your behavioral VHDL design files and testbench.** Type the following commands at the prompt:

   ```
   analyze -src <design_name>.vhd -lib user.lib -libieee -lib
   synopsys
   analyze -src <vhdl_test_bench>.vhd -lib user.lib -libieee
   -lib synopsys
   ```

4. **Map to the Actel VITAL and FPGA libraries.** If any Actel cores are instantiated in your VHDL source, you must add the following switches when analyzing your VHDL design files:

   ```
   analyze -src <design_name>.vhd -lib user.lib -lib $ALSDIR/lib/vtl/95/
   swave/<vhd_fam> -libieee -lib synopsys
   ```

   Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

   ```
   library <vhd_fam>;
   use <vhd_fam>.components.all;
   ```

5. **Simulate your design.** Type the following command at the prompt:

   ```
   vbsim -cfg <configuration_name> -until complete -lib user.lib -libieee -
   ```

```
lib synopsys
```

If any Actel cores are instantiated in your VHDL source, you must simulate using the compiled Actel VHDL library for that family. For example, to simulate a configuration named "cfg_tb_behavior" for a MX device, type the following command at the prompt:

```
vbsim -cfg cfg_tb_behavior -until complete -lib user.lib
-libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
```

Refer to the Innoveda documentation for additional information about performing simulation with SpeedWave.

# Structural Simulation

Use the following procedure to perform a structural simulation of an Actel design:

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.
2. **Analyze the structural VHDL netlist and the testbench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 21 for the procedure. Type the following commands at the prompt to analyze the VHDL netlist and testbench:

   ```
   analyze -src <design_name>.vhd -lib user.lib -lib $ALSDIR/lib/vtl/95/
   swave/<vhd_fam> -libieee -lib synopsys
   ```

   ```
   analyze -src <vhdl_test_bench>.vhd -lib user.lib -lib $ALSDIR/lib/vtl/
   95/swave/<vhd_fam> -libieee -lib synopsys
   ```

3. **Simulate your design.** Type the following command at the prompt:

   ```
   vbsim -cfg <configuration_name> -until complete
   -lib user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/
   <vhd_fam>
   ```

   For example, to simulate a configuration named "cfg_tb_structure" for a 40MX device, type the following command at the prompt:

   ```
   vbsim -cfg cfg_tb_structure -until complete -lib user.lib -libieee -lib
   synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
   ```

Refer to the Innoveda documentation for additional information about performing simulation with SpeedWave.

# Timing Simulation

SpeedWave timing simulation is no longer supported by Actel. To perform timing simulation:

1. Export a VHDL or Verilog netlist and *.sdf file from Actel Designer software
2. Use the HDL netlist and *.sdf file to run timing simulation in other HDL based simulators.

# A

# Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

## Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0)1276.401500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

## Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

## Actel Technical Support

Visit the Actel Customer Support (http://www.actel.com/kb/search.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

## Website

You can browse a variety of technical and non-technical information on Actel's home page, at www.actel.com.

# Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

## Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

## Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

**650.318.4460**
**800.262.1060**

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/contact/offices/index.html.

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