SX-A Frequently Asked Questions

Version 4.0

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I. ARCHITECTURE

I.1. CLOCK

1. How many clock pins are available in SX-A?

Ans. There is a hardwired clock pin (HCLK) plus two routed clock pins (CLKA, CLKB). For SX72A, there are four additional quadrant clock pins (QCLKA, B, C, and D).

2. How do the quadrant clocks work in SX-A?

Ans. 54SX72A offers four additional quadrant clocks (QCLKA, B, C, and D) at minimal die cost. These are routed clocks and can be driven from external pins or from internal logic signals within the device. Each of these clocks can individually drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The grouping processing is done automatically by Designer software. In addition to global RESET and PRESET networks driven by global clocks, QCLK can be used as a quadrant RESET and PRESET network. It can also drive any combinatorial gate or data input to a flip-flop. It can be used through QCLKBUF, QCLKBUFI, QCLKINT, QCLKINTI, QCLKBIBUF or QCLKBIBUFI macros. The macros are accessed through library elements similar to those traditional clock buffers in SX families. The QCLKBUFI, QCLKBIBUFI, and QCLKINTI are the new QCLK features that are only provided in the SX72A device.

3. Can QCLK in SX72A be used as I/O rather than as CLK?

Ans. In the SX72A, QCLK is a "clock-bibuf". In other words, QCLK is a "quadrantclock" input pin with an I/O buffer. Thus, QCLK can be used as a QCLK pin alone, or as an I/O, or as an I/O driving an internal QCLK net. When unused, this pin should be set low or high on the board to avoid power dissipation, but they can be left floating if required.

4. Can a pin that has QCLKBUF on it be used as a REGULAR INBUF or OUTBUF?

Ans. Yes, any unused QCLKBUF can be used as regular INBUF or OUTBUF.

5. Can unused clock pins be left floating?

Ans. For RTSX72S and SX72A, CLKA/B and QCLKA/B/C/D are Clock-IO pins (can be clock and/or IO). When these pins are not used, they should be tied to "high" or "low" on the board to avoid extra power dissipation but they can be left floating if desired. When unused, they will act as tristated outputs.

None of the other SXA or RT54SX32S parts have QCLKs and their CLKA/B pins are Clock only pins (not Clock-I/Os). Unused CLKA/B pins must not be left floating.

6. If CLKINT is used instead of CLKBUF, can I use the CLK pin as user I/O?
Ans. No, the CLK pin can be used for clock only. But the SX72A's clock pins can be used as regular I/Os. In case they are not used, Designer will tri-state them.
7. Can a pin that has HCLKBUF on it be used as a REGULAR INBUF or OUTBUF?
Ans. No, HCLKBUF can not be used as inbuf or outbuf for any device.
8. Can I use HCLK as an output?
Ans. No. You cannot use HCLK as an output; it is a DRC (design rule checking) violation. You can use other clock like CLKA/CLKB on SX72A devices for this purpose.

I.2. I/O

9. What are the new SX-A I/O features?
Ans. The SX-A devices have a variety of advanced I/O features that are not available in the SX devices. They include hot swapping, PCI Compliance, programmable input threshold voltage, configurable output slew-rate, and configurable output state during power-up. However 3.3V PCI device is not hot swappable and 5V tolerant.
10. What is "hot swapping"?
Ans. Hot swappable means that if an SX-A device is plugged into an electrically active system, the device reliability will not degrade and no damage to the host system will be caused.
11. What are the hot swap capabilities of SX-A?
Ans. SX-A device I/Os are specifically designed to be programmed for hot swapping applications. When the recommended power-up sequence is used (VCCA at the same time as or before VCCI), the entire device is tristated during power-up until the I/Os become active. For detailed information, see the app note: Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications.
12. What is the maximum capacitive load SX-A devices can drive?
Ans. There is no maximum capacitance as such. When we characterize, we specify different loading (35pf for 5v TTL and 10pf for 3.3v PCI). Users can customize the I/O loading for timing analysis in Designer software using the PinEdit tool.
13. For SX-A family, the Max. tr/tf is 10ns. What may happen if the input signal rise time exceeds this value, for example 200ns? Will that damage the device?
Ans. If the input signal stays in the trip point region of the input buffer for too long, it MAY causes the output of the input buffer to oscillate. The oscillation at the OUTPUT of the input buffer will stop once the slow input comes out of the transition region, however a functional failure may occur in your system because of this oscillation. It should be OK to sample the OUTPUT when it becomes stable.
The I/O transistors will limit the current while the input voltage stays in the trip point region. Damage is unlikely, but possible.
14. Does SX-A support LVDS (low voltage differential signaling)?
Ans. SX-A does not support LVDS.
15. What voltages do SX-A I/Os tolerate?
Ans. SX-A I/Os support 2.5V/3.3V/5V mixed voltage operation and are designed to tolerate 5-volt input in each case if TTL mode is selected. For PCI mode, I/Os support both 3.3V and 5V, but input voltage tolerance depends on V_{CCI}.
3.3V PCI operation:

Symbol	Parameter	Min.	Max.

V_{CCA}	Supply Voltage for Array	2.3v	2.7v
V_{CCI}	Supply Voltage for I/Os	3.0v	3.6v
V_{IH}	Input High Voltage	$0.5V_{CCI}$	V_{CCI} + 0.5
V_{IL}	Input Low Voltage	–0.5	$0.3V_{CCI}$

5V PCI operation:

Symbol	Parameter	Min.	Max.
V_{CCA}	Supply Voltage for Array	2.3v	2.7v
V_{CCI}	Supply Voltage for I/Os	4.75v	5.25v
V_{IH}	Input High Voltage	2.0v	V_{CCI} + 0.5
V_{IL}	Input Low Voltage	–0.5	0.8

16. Why the standby current of SX-A is higher than SX?

Ans. As Actel continues to reduce process geometry, the transistor leakage goes higher and causes the standby current to increase. The portion of the standby current due to antifuse leakage and charge pumps remains about the same.

Users may be concerned that this increase in standby current will increase the overall power consumption, but this is not the case since total power consumption is mainly dependent on dynamic power (Vcc * $I_{dynamic}$) and not static power (Vcc * $I_{standby}$). In addition, remember that SXA devices still have lower total power consumption than SX devices because SXA's operate at a core voltage of 2.5 V.

17. What are the drive capabilities of SX-A outputs?

Ans. The output drive strength of SX-A devices is dependent on the V_{CCI}. If V_{CCI} is 2.5V, the outputs' drive will be 2.5V, If V_{CCI} is 3.3V, the outputs' drive will be 3.3V. If V_{CCI} is 5V, the outputs' drive will be 5V.

18. If an I/O is configured at 2.5V, is it 3.3V or 5.0V tolerant?

Ans. The SX-A I/Os (inputs) are always 5V tolerant regardless of VCCI if LV/TTL mode is selected. However to configure an SX-A device to drive 5V with VCCI =3.3V, users can utilize an Open Drain configuration of the I/O cell with an array inverter cell and an external pull-up resistor to 5V. Please refer to "design tips" section of apps note: "Actel eX, SX-A and RT54SX-S I/Os". For PCI mode input tolerance depends on VCCI.

19. What's the state of unused I/Os on SX-A devices?

Ans. All of the unused I/Os are configured as tri-state out by the Designer software. Please see "Online Technical Support" keyword "unused" for details.

20. If JTAG I/Os are not configured as dedicated BST pins, can they be used as normal I/Os?

Ans. Yes, if JTAG I/Os (except TMS) are not programmed as dedicated JTAG I/Os, they can be used as normal I/Os. When the "Reserve JTAG" box is not selected (default setting in Designer software), the SX-A is placed in Flexible mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or BST pins. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logical low. Once the BST pins are in test mode they will remain in BST mode until the internal BST state machine reaches the "logic reset" state. At this point the BST pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set to logical HIGH. The

Program fuse determines whether the device is in Dedicated Test or Flexible mode. The default (fuse not programmed) is Flexible mode.
The functionality of each pin is described below: -

Program Fuse Blown (Dedicated JTAG Mode)	**Program Fuse Not Blown (Flexible Mode)**
TCK, TDI, TDO are Dedicated JTAG pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10K ohm on TMS

21. What happens to an SX-A chip when it is not powered up and voltages are applied to the I/Os?

Ans. All of the I/Os are tri-stated when it is not powered up. Therefore, no current flows into the SX-A chip when you apply voltages to the I/Os. This will not damage the SX-A chips. Voltage must not exceed maximum input voltage spec.

22. What slew rates are available for the SX-A I/O's?

Ans. There are two slew rates: high slew and low slew. The **typical** values are shown in the following table:

	High Slew	**Low Slew**
3V TTL Low to High	1.4 V/ns	1.4V/ns
3V TTL High to Low	2.5V/ns	0.7V/ns
5V TTL Low to High	2.8V/ns	2.8V/ns
5V TTL High to Low	3.9V/ns	1.4V/ns
3V PCI Low to High	2.4V/ns	N/A[1]
3V PCI High to Low	3.4V/ns	N/A
4V PCI Low to High	4.3V/ns	N/A
5V PCI High to Low	4.0V/ns	N/A

1 PCI standard does not enable low slew.

Note: Slew control affects only the falling edges, rising edges are not affected.

23. Do the I/Os have individual slew control?

Ans. Yes, there is a programmable fuse to control individual I/Os. This is performed in the I/O Attribute editor in Designer.

24. Can I interface the SX-A I/Os with LVTTL or LVCMOS?

Ans. Yes, SX-A is designed to support LVTTL and LVCMOS.

25. What I/O features are selectable on a pin-by-pin basis?

Ans. Designer version R1-2002 and newer will allow user to select I/O features on a pin by pin basis. These features include PCI, TTL, output tri-state at power-up, None/Weak/High resistor pull-up or pull-down for output tri-state at power-up, High slew or low slew. The default is high slew rate.

26. Are the IV curves available?

Ans. The IV curves can be derived from the IBIS Models on Actels website: http://www.actel.com/custsup/models/ibis.html.

27. What is the maximum source/sink current of SX-A devices?

Ans. The maximum source/sink current can be derived from IBIS model found on Actel website.

Following table lists these values for SX-A devices.

I/O Standard	**Max Source Current**		**Max Sink Current**	
	Min VOH	**I(mA)**	**Max VOL**	**I(mA)**

5V TTL	2.4V	-139	0.4V	46
	0.9Vcci	-35	0.1Vcci	56
3.3V LVTTL	2.4V	-43	0.4V	39
	0.9Vcci	-18	0.1Vcci	32
5V PCI	2.4V	-139	0.55V	61.5
3.3V PCI	0.9Vcci	-20	0.1Vcci	38
2.5V LVCMOS	1.7V	-30	0.7V	59
	2.0V	-21	0.4V	37
	2.1V	-17	0.2V	19

28. Can TRST pin be used as regular I/O?

Ans. Yes, The TRST pin will function as a user I/O when “Reserve JTAG Reset” box in Designer is not checked. The internal pull-up resistor will be disabled in this mode.

29. What is In-Rush current? What is the value for SX-A family?

Ans. The "In-Rush current " is what we call the Transient current spike during powerup. This spike is due to current on V_{CCA} and will increase with the size of the core. The values range from 45mA-557mA depending on ramp rate and the device and lasts for approx. 500ns on the V_{CC} plane. For more detail please refer to Transient current in Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications.

I.3. PCI

30. Are the SX-A I/Os PCI compliant?

Ans. Yes, the SX-A I/Os are 3.3/5V PCI compliant. To use this you must set the I/Os to PCI compliant mode in Designer.

31. Are hot swappable I/Os supported for SX-A's 3.3V PCI operation?

Ans. No. Because there are clamp diodes in those I/Os, that’s why it does not support hot swappable I/Os. However 5V PCI I/Os are hot swappable.

32. Does SX-A support 3.3V PCI I/Os when it is hot-inserted into a live system?

Ans. No. The SX-A 3.3v PCI I/O configuration is not designed for hot insertion. It is possible to damage the I/O's during a live insertion event.

33. What is the difference between LVTTL and PCI as far as the I/O attributes are concerned?

Ans. In SX-A, the 3.3v PCI I/O configuration is not Hot Swappable. Also, the PCI I/O input threshold voltage and fast output slew rate must be selected to comply with the 3.3v PCI spec. LVTTL I/O's are Hot Swap-able, with LVTTL input threshold voltage and the user may select fast or slow output slew. Both 3.3v PCI and LVTTL have an option of enabling a pull-up or pull down resistor which are active only during powerup.

34. Is mixed I/O standard (LVTTL and PCI) allowed?
Ans. Yes, mixed I/O standard is allowed. You can set the standards on an individual pin basis using the I/O attribute editor in Pin Edit. You need to perform layout again after changing the standards.

I.4. Power Supply

35. Some of the larger packages have multiple V_{CCA}, V_{CCI} pins. If one of the V_{CCI} pins is not connected (open) but all the other V_{CCI} are connected properly, does the FPGA operate normally? What about V_{CCA}?
Ans. It is important to have all the power supplies connected to the board. With larger package types you may be able to get away with only connecting some but we do not recommend or guarantee this. All power pins should be connected.

Our concern is that with smaller package types (PLCC 84) there is only one V_{CCA} and one V_{CCI} per side. If power is not supplied to each periphery of the device then there may not be sufficient drive to facilitate reliable operation.

36. If the voltage on V_{CCA} exceeds absolute maximum rating of 3.0 volts, what kind of damage will occur inside the chip?
Ans. This will stresses the gate oxide, generate hot electrons, break down some junctions and cause long terms reliability concerns or damage the chip immediately.
This is also outside of the timing range guaranteed for the device.

37. For the SX-A device, if input voltage applied is 5.0V when VCCI is 3.3V? What will be the case if 3.3 V PCI is selected?
Ans. The PCI specification for 3.3v PCI specifies that the maximum input voltage shall not exceed VCCI + 0.5v, or 3.8v for a VCCI of 3.3v. When 3.3v PCI I/Os is selected in Designer, a clamp diode is used between the input and the VCCI rail. This means that applying 5V to the input will forward-bias the clamp diode, drawing high amounts of current. This should NOT be done, but it is only applicable to 3.3v PCI operation. For other I/O options the user can apply 5v to the inputs with no problem.

38. Is the reference voltage Vccr required for SX-A?
Ans. SX-A does not require the reference voltage VCCR.

39. What's the logic core voltage supply for the SX-A family?
Ans. It always requires 2.5V.

40. How many supplies do I need for SX-A?
Ans. SX-A needs two power supplies, V_{CCA} (2.5V only) and V_{CCI} (2.5V, 3.3V, or 5V).

I.5. POWER-UP

41. What is the value of Pull-up or Pull-down resistors for SX-A, SX-S? To which supply voltage are they connected (V_{CCA} or V_{CCI})?
Ans. All A54SX-A devices are equipped with optional pull-up or pull-down resistors of about 50 KΩ that are enabled during power-up. They are connected to V_{CCA}. After complete power-up at 2.5V on VCCA (actually slightly before it reaches 2.5V), these resistors are disabled so the I/Os will behave normally.

42. At what voltages do the I/Os become active during power-up?
Ans. The I/Os of A54SX-A devices are tri-stated during power-up when the recommended power-up sequence is used, until the point where the I/Os become active and behave according to the design. The following table summarizes the V_{CCA} voltage at which the I/Os behave according to the user's design for all A54SX-A devices at room

temperature for various ramp-up rates. The data reported assumes a linear ramp-up profile to 2.5V.

Table V_{CCA} Voltage at which I/Os become Active (Volts)

Devices	Ramp rate(V/mS)							
	0.33	0.033	6.6	3.3	0.66	0.33	0.132	0.033
A54SX08A	2.5	2.4	1.72	1.62	1.37	1.34	1.29	1.27
A54SX16A	2.5	2.5	1.8	1.56	1.25	1.18	1.1	1.04
A54SX32A	2.5	2.5	2.28	1.86	1.41	1.29	1.21	1.16
A54SX72A	2.5	2.5	2.05	1.68	1.31	1.26	1.21	1.18

43. What's the status of SX-A I/Os during power-up?

Ans. During power-up/down (or partial power-up/down), all I/Os are tri-stated when VCCA is equal to or greater than VCCI during power-up. In addition, all outputs can be programmed at power-up time to have resister pull: None, High, or Low. This is performed in the I/O attribute editor in Designer. The power-up resistors are available for all I/O standards. We recommend that you only use this feature for output signals.

You are allowed to assign power-up state to inputs and that power-up state will be seen by inputs during power-up, but not after. Therefore, since the time at which the powerup state becomes disabled is variable, it is difficult to prevent a floating input condition, which can cause unknown values to be input through an I/O. For detail information please read: Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

I.6. Debugging

44. Does SX-A provide the JTAG reset pin TRST?

Ans. Yes, there is a JTAG reset TRST pin, which you can program as a dedicated JTAG reset pin or use as a regular I/O.

45. What's the pin number of the TRST pin?

Ans. It is package dependent. Here is the list:

Package	**Pin**
CQ256	Pin 30
PQ208	Pin 30
TQ100	Pin 16
TQ144	Pin 22
BG329	Pin N2
FG484	Pin R5

46. Can I use SX-A and Silicon Explorer under the following conditions?

GND = (-) 2.5V

VCCA = VCCI = 0V

Ans. Yes, you can use the device under these conditions as long as the inputs do not exceed (+) 2.5V (5V input tolerance). The Silicon Explorer II must be powered with at least 3.3V, so for this board, it should be connected to at least (+) 0.8V.

I.7. Misc.

47. Is the SX-A pin compatible with SX?

Ans. Yes. All the V_{CCR} pins in SX become no connect in SX-A. However, you cannot just drop in an SX-A device to replace the SX device because the power supply

requirements are different. Also, SX72A has different pin assignment compared to other SXA device (SX-A datasheet). For more detailed information, please refer to the application note: “SX to SX-A Design Migration”.

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