Power FAQs

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1. Which FPGA technology offers the lowest power?

Three basic technologies are used in FPGAs: Flash, antifuse, and SRAM. For a given process node, antifuse and Flash technologies offer the lowest static and dynamic power consumption. Both of these technologies have power characteristics similar to those of an ASIC. Unlike SRAM FPGAs, Flash and antifuse FPGAs have no power-up or configuration power components and are best for power-sensitive applications.

2. What can I do to reduce power consumption in FPGAs?

Flash and antifuse technologies offer the lowest power consumption at a technology node; therefore, choosing the FPGA technology that consumes the lowest power is a key decision for reducing system power. Additionally, Actel Flash products offer several low power modes that reduce power consumption to as low as 5 µW in Flash*Freeze™ mode. Actel antifuse technology also offers a low power mode. This feature allows the PLLs and some additional circuitry to be powered down. The low power mode also enables the user to power-down I/O banks individually, which further reduces power consumption.

3. What is the best way to estimate the power consumed in an FPGA?

FPGA manufacturers have both pre-design (power estimator) and post-design (SmartPower) tools available. The pre-design tool is typically a spreadsheet that calculates estimated power after you enter design assumptions. The post-design tools extract parameters from the netlist and estimate power consumption more accurately. Care must be used when comparing power estimates between different suppliers' tools. The underlying assumptions vary from manufacturer to manufacturer and can provide a user with misleading information. Actel tools are some of the most realistic and accurate power tools available.

4. How should I realistically estimate a device's power?

Many vendors provide "optimistic" power analysis tools that mislead designers to commit to their solution based on unrealistic data, or they make real data virtually impossible to obtain. An example of misleading information is specifying static current at a certain value but mentioning in the fine print that the power was measured on blank devices. Accounting for the total power consumption required by the FPGA and all additional support components (total system power) is something designers should look at carefully.

5. Is the lowest power FPGA the device with the lowest V_{CC}?

Lowering the V_{CC} contributes to lower power consumption (especially dynamic power). However, FPGA technology and architecture play a significant role in power consumption. This can result in a device with a higher V_{CC} having lower power consumption than a comparable device with lower V_{CC}. An example is the Actel ProASIC®3 family, a 1.5 V family that offers lower system power than competitors' 1.2 V families. The Actel IGLOO™ family can operate from a 1.2 V core voltage, reducing dynamic power further.

As processes move to 90 nm and below, power consumption begins to increase significantly. As a result, the static power component becomes the dominant factor due to high transistor leakage.

For example, SRAM-based FPGAs, fabricated at a 90-nm process node, can consume 10 times the static power of Actel Flash products such as ProASIC3/E and Fusion devices, and 1,000 times the static power of Actel IGLOO devices.

6. Does power consumption vary with the design in the FPGA?

The actual design and device utilization have an effect on power. Different designs consume different amounts of power. Architecture also plays an important role in power. One architecture may be better suited for a particular design. For the most part, the lowest power FPGA overall will be consistently lower in power for almost all designs. However, some designs may offer lower power when implemented in different architectures. Using enable flip-flops or clock regions and avoiding large numbers of switching I/Os can significantly impact power consumption. Design techniques can mitigate all of these issues.

7. I have plenty of power for my system. Why should I be concerned about power?

Power concerns go beyond availability. There is an economic concern in having to oversize the power supply. Also, higher power devices have higher heat dissipation requirements. Higher system heat requires more airflow and larger fans, enclosures, and/or heat sinks. Even if power is not a direct concern, the subsequent heat dissipation effect should be considered for system reliability. Cost-conservative estimates put a cost of $1 on each additional 1 W of power consumed on a board.

8. Does ambient temperature have an effect on my power consumption?

Ambient, and more importantly, operating junction temperatures do play a significant role in static power consumption. Again, this is more pronounced in different FPGA technologies. Antifuse and Flash technologies have relatively minor increases in power with temperature. SRAM-based FPGAs will see larger (exponential) increases in power consumption at higher temperatures. Designs may run hotter than the designer expected, leading to surprises in power consumption. Complex designs typically have junction temperatures far above ambient. If care is not taken to estimate maximum junction temperature, thermal runaway can occur in some SRAM FPGAs.

9. Can high power consumption lead to thermal runaway and device destruction?

Devices that consume high power are more susceptible to thermal runaway due to rise in temperature, which leads to runaway power consumption and device destruction. SRAM-based FPGAs may be affected by this recursive phenomenon, and measurements should be taken to resolve heat dissipation issues and monitor temperature and current limits continuously.

10. What are the top three trends in low power design?

The success of wireless and the proliferation of portable electronics have created a need for more power awareness in the industry. Certainly, system designers are more power conscious than ever. This can be attributed to tighter system power budgets, specifications, and standards that put a cap on the total power consumed by the system.

Growth for battery-operated applications such as wireless handhelds and multi-media players drives the demand for low power semiconductors and that trend will continue to drive semiconductors to the nano-amp range. Further, because of the short product life cycles and extreme competition in this marketplace, designers require a growing list of features and complexity, but not at the expense of draining the battery. This makes the reprogrammable, full-featured solutions such as Actel IGLOO FPGAs more attractive as an alternative to ASICs and CPLDs for portable applications.

11. What are the biggest challenges facing OEM companies in developing low power systems?

As planning begins for next-generation designs, power budgets rarely grow; instead they hold steady or decrease. Simultaneously, however, more features and more processing power are added to the list of "must haves." Not to be discounted is the effect of Moore's law on shrinking process geometries and the resulting hikes in static power consumption from high transistor leakage. Programmable semiconductor platforms are becoming preferred solutions as product life cycles shrink, market competition grows, and time to market has a significant impact on product success. For power-sensitive portable applications, for example, the challenge remains to find a low power programmable platform that can meet all other design requirements, including cost, performance, size and security. Low power, nonvolatile, single-chip FPGAs such as Actel IGLOO devices meet these requirements head on.

12. Where do you see the demand for low power FPGAs heading?

To more effectively target the rapidly changing consumer market, large ASIC consumers are looking for ways to employ FPGAs to rapidly produce and test-market products. Low power is a priority in the consumer market and battery-operated applications. Furthermore, the trend in industrial, medical, and military market segments is increasingly toward power-constrained devices such as handheld terminals and handsets.

13. What is Actel Flash*Freeze technology?

The new Actel Flash*Freeze technology allows Actel IGLOO low power FPGAs to quickly and easily enter and exit an ultra-low power mode within 1µs. Designers do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology allows the user to keep all power supplies, I/Os, and clocks connected to the device in normal operation. When the IGLOO device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

14. Why is the power-up spike in some FPGAs a concern?

The power-up spike on an SRAM FPGA can be as high as 2 Amperes. If insufficient current is available to support this high-current condition, the FPGA may not configure properly. Other devices on the board may also be affected due to brownout conditions. Sizing the power supply to meet this high current requirement at start-up adds unnecessary cost to the system. Some vendors offer to mitigate this phenomenon by adding power sequencing requirements, which adds cost to bill-of-materials and design complexity.

15. Historically, FPGAs have been considered to consume a lot of power. What has changed?

Over the years, FPGA technology has continued to evolve and become mainstream. Nonvolatile FPGAs have been able to approach and even match ASIC power numbers in recent history as a result of power-optimized design and process tweaks. These technical changes and innovations, such as the new Flash*Freeze technology, have enabled FPGAs to demonstrate dramatically lower static power consumption, making them an ideal solution for those applications that must also balance flexibility and ability to accommodate ever-changing end-product standards. The reduction of core voltage to 1.2 V has also resulted in a reduction in power. Combined with the staggering low static power numbers, this reduced dynamic power enables FPGAs to provide lower total system power than ASICs.

16. Does the power-up spike affect my battery-powered systems?

Yes, power spikes can greatly reduce battery life. Batteries last longest when subjected to current drain that is moderate compared to their overall capacity rating. Using an SRAM FPGA requires the battery to be sized properly to accommodate the power-up spike and dynamic power consumption. Failure to do so can lead to system-level problems caused by errors in the configuration process, as well as greatly reduced battery life. Battery life experiment shows that IGLOO devices extend battery life by five times when compared to other low power PLDs. In addition to the power-up spike, SRAM-based FPGAs and other "low power" PLDs have higher dynamic and static power consumption than Actel IGLOO Flash FPGAs, which reduces battery life dramatically.

For more information, visit our website at **http://www.actel.com**

www.actel.com

Actel Corporation

2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.

Dunlop House, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone +44 (0) 1276 401 450
Fax +44 (0) 1276 401 490

Actel Japan

www.jp.actel.com
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150, Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668

Actel Hong Kong

www.actel.com.cn
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488