MX Frequently Asked Questions

Version 3.0

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Table of Content

I. Architecture and Features

I.1. CLOCKS

1. How many clock pins are available in MX?

Ans. The 40MX device has one CLK pin and the 42MX has two clock pins (CLKA and CLKB). In addition, 42MX devices that contain SRAM modules (42MX36) have four additional quadrant clocks.

2. If I use a CLKINT buffer in 42MX device, are the CLKA and CLKB available as normal I/Os?

Ans. Yes, CLKA and CLKB can be used as normal I/Os, bypassing the clock network.

3. Can I drive the clock pins with voltages different than V_{CCI}?

Ans. See the Power Supply section for input tolerance levels

4. Can unused clock pins be left floating?

Ans. Clock pins that do not have any I/O assigned to them may be left floating. They will behave as unused I/O.

5. Can I use the clock pin to drive combinatorial cells?

Ans. Yes.

I.2. I/Os

6. What is the I/O Source/Sink Current for MX devices?

Ans. The exact value of source and sink current can be found in the I/V curve. Please refer to IBIS models and the readme file posted on Web at:
http://www.actel.com/support/support/support_ibis.html

7. What is the Maximum input capacitance for dedicated inputs like CLKA and CLKB?

Ans. Max input capacitance for ALL pins is 10pF. This includes clock pins.

8. What is the input impedance for MX devices?

Ans. I/O impedance of Actel devices can be determined from the equation:

$$Z = V/Ioz$$

Where Ioz = Tristate Output Leakage Current = +/- 10uA (very conservative)
and V = Vcc.

For a 5V part (assuming 4.5 V as worst case low voltage):

$$Z = 4.5V/10\_A = 450Kohm$$

This is a minimum value because the 10µA is the maximum specification for Ioz. For mixed voltage condition use VCCA.

9. If an I/O is configured to be input only, should I expect a lower capacitance value?

Ans. I/O capacitance will be the same, whether the I/O is configured as Input Only or Bi-directional.

10. What is the status of the MX I/Os during power-up?

Ans. The I/Os, regardless of whether they are programmed to be inputs, outputs, bibufs or tribufs during operation, can temporarily behave as outputs during power up. This behavior varies with the speed at which power is applied to the device.
Please refer to the “42MX Family Devices Power-up Behavior” app note for details:
http://www.actel.com/appnotes/MXPowerUpAN.pdf

11. What voltages do MX I/Os tolerate?

Ans. MX I/Os tolerate –0.5v to Vcci+0.5.

12. What is the state of unused I/Os?

Ans. Unused I/Os are configured as outputs driving low for 40MX families, and for 42MX09 and 42MX16 devices. For 42MX24 and 42MX36 devices, unused I/Os are tri-stated, but the input capability is not physically disconnected. Please see the following Guru document "What Happens to Unused I/Os and CLKs?":
http://www.actel.com/apps/guru/jul99/hw1625.htm

13. What happens to an MX chip under mixed voltage conditions when it's not powered up and voltages are applied to the I/Os?

Ans. When powering the device in the mixed voltage mode (V_{CCA} = 5.0V and V_{CCI} = 3.3V), V_{CCA} must be greater than or equal to V_{CCI} throughout the power-up sequence. If V_{CCI} is 0.5V greater than V_{CCA} when both are above 1.5V, then the I/Os input protection junction will be forward biased. This causes the I/Os to draw large amounts of current. When V_{CCA} and V_{CCI} are in the 1.5 to 2.0V region and V_{CCI} is greater than V_{CCA}, all I/Os shortly behave as outputs that are in logical high state and ICC rises to high levels. For power-down any sequence with V_{CCA} and V_{CCI} can be implemented.

Also, there was one known power-up problem in the old 42MX device. Please see the following Guru document "42MX Fast Power-Up Problem and Solution":
http://www.actel.com/apps/guru/apr99/ns845.html

14. Are the MX I/Os PCI compliant?

Ans. Only 42MX24 and 42MX36 are PCI compliant. Please see the following Guru document "Which Actel devices have PCI drivers and how do I enable them?" about how to enable them:
http://www.actel.com/apps/guru/dec99/hw1631.html

I.3. Power Supply

15. What operating voltage levels are available for MX Devices?

Ans. The 40MX FPGA operates in 5V only systems or 3.3V only systems.

Vcc	Input	Output
3.3V	3.3V	3.3V
5V	5V	5V

The 42MX FPGA operates in 5V only systems or 3.3V only systems, or mixed 5.0V/3.3V systems.

Vcca	Vcci	Input	Output
3.3V	3.3V	3.3V	3.3V
5V	3.3V	3.3V, 5V	3.3V
5V	5V	5V	5V

16. How many supplies do I need for MX?

Ans. The 40MX device requires only Vcc (3.3V or 5V) whereas the 42MX needs two power supplies, V_{CCA} (3.3V or 5V) and V_{CCI} (3.3V or 5V).

17. Is the reference voltage Vccr required for MX?

Ans. No, 42MX devices do not require the reference voltage V_{CCR}.

18. What is the logic core supply voltage (V_{CCA}) for the MX family?

Ans. It requires 3.3V or 5V.

19. Are the MX devices hot insertion compliant?

Ans. No.

20. How Can I Enable Low Power Mode on 42MX Devices?

Ans. To place the device in Low Power Mode, connect the LP pin to the logic HIGH. The device enters the low power mode 800ns after LP transitions to logic high. Normal operation resumes 200µs after the LP pin is returned to the logic LOW.

Please see the Guru document regarding Low Power mode "How to Enable Low Power Mode on 42MX Devices": http://www.actel.com/apps/guru/mar_298/hw1632.html

21. Do we have to connect power supply to all the Vcca/Vcci pins together?

Ans. All Vcca/Vcci are connected internally. But there is a transmission voltage drop. We recommend that you connect the power supply to all Vcca/Vcci pins.

22. Which 42MX devices have power-up limitations?

Ans. Some 42MX09, -16, -24, and -36 devices have special power-up conditions. You can get the necessary information from the following guru document "42MX Fast Power-Up Problem and Solution":
http://www.actel.com/apps/guru/apr99/ns845.html

23. How can I tell which 42MX devices have the power-up fix?

Ans. The following instructions enable you to tell whether you are using the 42MX device with the X39 die revision that has the power-up fix. The devices with the X39 die revision DO NOT say so on the packaging. Read the lot code of the questionable device. If the device lot code starts with...

"2ACU..." then it uses the X39 die revision.
"2ACR..." then it does not use the X39 die revision.
"2ACT..." then it might use the X39 die revision. To verify whether this device uses the X39 die revision, contact Tech Support

Any other wafer lot number is older material and does not use the X39 die revision. Please see the GURU document below "42MX Fast Power-Up Problem and Solution" for more information about the Power-up issue:
http://www.actel.com/apps/guru/apr99/ns845.html

I.4. Debugging and Migration

24. Are the MX devices JTAG compliant?

Ans. Only the MX24 and the MX36 are JTAG compliant. These devices support only the minimum feature set of JTAG (i.e. EXTEST, Preload/Sample, BYPASS).

25. If not used as a JTAG I/O, is a JTAG pin available as a normal I/O?

Ans. Yes, if JTAG I/Os are not programmed as dedicated JTAG I/Os, they can be used as normal I/Os except for TMS. The functionality of each pin is described below:

JTAG Fuse Blown (Dedicated JTAG Mode)	JTAG Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are Dedicated JTAG pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor For TMS	Use a pull-up resistor of 10K ohm on TMS

26. Do we have active reset (nTRST) pin in 42MX device?

Ans. No, there is no TRST pin in 42MX devices. However, the 42MX contain power-on circuitry that resets the JTAG BST circuitry upon power-on.

27. How can I migrate the design from ACT1 to 40mx device?

Ans. Migrating from ACT1 to 40MX is not automatic. In Designer, you must recompile and re-layout your design. Additionally, the conversion requires that you run timing analysis again since the die size is different for these devices.

I.5. Misc.

28. Do the 42MX24 plastic package devices have a ground plane?

Ans. Yes, all 42MX plastic packages have ground planes.

29. What is the FIT rate for all MX processes?

Ans. MX devices based on .45µm CMOS process have a FIT rate of 15.92.

30. Do we have open drain output in MX devices?

Ans. No.

31. Are the BSDL models available for MX devices?

Ans. Only 42MX devices have boundary scan circuitry. The generic BSDL models are available in the user page:

http://www.actel.com/user/BSDL/index.html

However, in Designer R1-2000 Service Pack 2 or above you can generate your own design-specific BSDL file. Go to File -> Export -> Auxiliary files, choose BSDL files option under the “Save as type” drop-down menu and click OK.

32. Do we have global set/reset pin in MX devices?

Ans. No, none of Actel's FPGA devices currently contains a built-in global set/reset pin that can be applied to all macro cells as an asynchronous reset.

33. What are Vil, Vih, Vol and Voh for MX device?

Ans. Please refer to the MX datasheet for information about the various I/O voltages: http://www.actel.com/docs/datasheets/MXDS.pdf .

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