Frequently Asked Questions
ModelSim Simulation

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About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- FAQ 4.1 was updated. For more information, see How do I get a free Libero License?, page 7.
- FAQ 4.2 was updated. For more information, see # Microsemi version supports only a single HDL # ** Error: (vsim-3039) / Why doesn't a mixed HDL simulation run?, page 7.
- FAQ 4.3 was added. For more information, see Is mixed language simulation supported in all the license types?, page 7.
- FAQ 4.4 was updated. For more information, see ModelSim license parallel port dongle: I had Libero v8.0 and upgraded to v8.3 but now ModelSim is no longer working; it throws a license checkout error message. Why?, page 7.
- FAQ 4.5 was updated. For more information, see How to fix the ModelSim License Error# ** Error: Failure to obtain a VHDL simulation license?, page 7.
- FAQ 4.6 was updated. For more information, see I installed Microsemi Libero. I am able to open the Libero project manager but cannot open ModelSim. It is not giving any warning or error. But if I click ModelSim from the project manager, it shows the ModelSim icon and then does not open anything. Why?, page 8.
- FAQ 5.1 was updated. For more information, see How do I set the simulation run time?, page 9.
- FAQ 5.2 was updated. For more information, see How do I set the time in ModelSim so it runs 6 ns?, page 9.
- FAQ 5.6 was updated. For more information, see How can I retain my radix in the wave window after I manually change them to a desired value for all simulations in a particular project?, page 10.
- FAQ 5.9 was updated. For more information, see ModelSim runs the simulation for the worst case temperature value. How can we simulate our design for both the best and worst case temperature values on ModelSim?, page 11.
- FAQ 7.1 was updated. For more information, see When I run ModelSim, my computer hangs, with vsimk.exe at 100% CPU usage. I cannot shut down ModelSim during this time. I must wait for 10 minutes until vsmik.exe stops running. Why?, page 16.
- FAQ 8.8 was updated. For more information, see In Libero IDE project manager settings there is a way to send extra command line arguments to the VSIM command. Is there a way to add a command line argument to the vlog command?, page 20

1.2 Revision 2.0

Revision 2.0 of the document had non-technical updates.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 ModelSim ME vs. ModelSim Full Version (SE/PE)

2.1 Can I use ModelSim SE/PE with Microsemi Libero IDE/SoC?

Standalone ModelSim does not include pre-compiled Microsemi libraries and does not set up the compiled library tree in the same manner, as the ModelSim Microsemi tool does.

To use the standalone version of ModelSim with Libero IDE, perform the following:
To simulate your design targeting Microsemi technology, you must have the VITAL or Verilog simulation library. Microsemi Libero IDE software includes two sets of VITAL and Verilog libraries, the source library and compiled library.

Source Library

You can install source VITAL and Verilog libraries during Libero IDE installation. After selection, the VITAL/Verilog libraries are installed in the following directory trees.

VITAL Library: *<Drive>:/Libero/Designer/lib/vtl/95*

Verilog Library: *<Drive>:/Libero/Designer/lib/vlog*

Full version of ModelSim users can compile the Microsemi library and map it during simulation. Microsemi does not recommend installing both ModelSim Microsemi and a full version of ModelSim on your system.

Compile Instructions for VITAL and Verilog libraries in ModelSim for Libero IDE/SoC:

ModelSim is integrated with Microsemi Libero IDE software in such a way that, if you run simulation from the Libero IDE Project Manager, it performs the following actions:

1. Automatically map the compiled VITAL (VHDL) or Verilog library
2. Compile the source code and testbench

In order to take advantage of this integration, you must compile the VITAL and/or Verilog library in a specific directory. Use the following instructions to specify a target directory.

These instructions compile the Microsemi VITAL library in the *<Drive>:/ModelSim_install/Microsemi/VHDL* directory.

1. Create a directory tree (*/Microsemi/Vhdl/src)* under the ModelSim installation directory. Copy the source library to the src directory
2. Invoke the ModelSim HDL simulator
3. Change directory to the *<Drive>:/ModelSim_install/Microsemi/VHDL* directory with the command: `cd <Drive>:/ModelSim_install/Microsemi/VHDL`
4. Create a <vhd_fam> family library directory for your simulator with the command: `vlib <vhd_fam>`
5. Map the Microsemi VITAL libray to the <vhd_fam> directory with the command: `vmap <vhd_fam> <Drive>:/ModelSim_install/Microsemi/VHDL/<vhd_fam>`
6. Compile the library with the command: `vcom -work <vhd_fam> src/<act_fam>.vhd`
   For example, to compile the axcelerator library for your simulator, type the following command: `vcom -work ex src/axcelerator.vhd`
7. Compile the migration library (optional). Perform this step only, if you are using the migration library. Use the command: `vcom-work <vhd_fam> src/<act_fam>_mig.vhd`

Compile Verilog Library (Verilog)

The following steps compile the Microsemi Verilog library in the *<Drive>:/ModelSim_install/Microsemi/vlog* directory

1. Create a directory tree (/Microsemi/vlog/src) under the ModelSim installation directory
2. Copy the source library to the src directory
3. Invoke the ModelSim HDL simulator
4. Change directory to *<Drive>:/ModelSim_install/Microsemi/vlog* directory with the command: `cd <Drive>:/ModelSim_install/Microsemi/vlog`
5. Create an <act_fam> family library directory for the simulator with the command: `vlib <act_fam>`
6. Compile the Microsemi library with the command: `vlog -work <act_fam> src/<act_fam>/*.v`
7. Compile the migration library (optional). Perform this step only, if you are using the migration library. Use the command: `vlog -work <act_fam> src/<act_fam>_mig/*.v`

Sample script for Pre-Synthesis simulation

```
# Run this script from simulation directory inside Libero IDE
# where add32.vhd is source code and add32_tb.vhd is testbench
# Libero IDE will not automatically run vsim command and so on
vmap work ./work_presynth
vcom -93 -work work_presyn ../hdl/add32.vhd
vcom -93 -work work_presyn ../stimulus/add32_tb.vhd
vsim work_presyn.testbench
add wave /testbench/*
run 1000ns
```

Sample script for Post-Synthesis simulation

```
# Run this script from simulation directory inside Libero IDE
# where add32.vhd is source code and add32_tb.vhd is testbench
# Libero IDE will not automatically run vsim command and so on
vlib work_postsynth
vmap work ./work_postsyn
vcom -93 -work work_postsyn ../designer/add32.vhd
vcom -93 -work work_postsyn ../stimulus/add32_tb.vhd
vsim work_postsyn.testbench
add wave /testbench/*
run 1000ns
```

Sample script for Post-layout simulation

```
# Run this script from simulation directory inside Libero IDE
# where add32.vhd, add32_tb.vhd and add32.sdf are source code,testbench and
sdf file
# respectively. add32_0 is the instance for add32 in testbench
# Libero IDE will not automatically run vsim command and so on
vlib work_postlayout
vmap work ./work_postlayout
vcom -93 -work work_postlayout ../designer/add32.vhd
vcom -93 -work work_postlayout ../stimulus/add32_tb.vhd
vsim -sdfmax /add32_0=../designer/add32.sdf work_postlayout.testbench
add wave /testbench/*
run 1000ns
```

Compiled Library

ModelSim Microsemi edition users must use pre-compiled Microsemi libraries for simulation. During installation of Libero IDE series software, there is a choice to select a library when installing ModelSim. After selection, the VITAL and/or Verilog libraries are installed in the following directory trees:

VITAL Library: <Libero_InstallPath>\Designer\lib\vtl\95
Verilog Library: <Libero_InstallPath>\Designer\lib\vlog

Where <fam> includes apa, axcelerator, ProASIC3, and ProASIC3e.

For IGLOO, IGLOO2, IGLOOe, Fusion, SmartFusion, SmartFusion2, and RTG4 only pre-compile libs are available. Pre-compiled libs are available at: http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#documents.

2.2 What is the difference between ModelSim ME and other versions of ModelSim (PE/SE and so on)?

ModelSim ME is functionally equivalent to ModelSim PE/SE. However, simulations may run slightly slower when compared with SE/PE.

The following list has some limitations of ModelSim ME when compared with SE/PE

- Advanced optimizations: Not supported
- Performance analyzer: Not supported
- C debugger: Not supported
- Dataflow window: Not supported
- Waveform comparison: Not supported
- Code coverage: Not supported
- Standalone viewer: Not Supported
- System C: Not supported
- Assertions (PSL): Not supported

For comparison between various ModelSim full versions, see *http://www.mentor.com/products/fv/modelsim/upload/ModelSimDE_Compare.pdf.*

2.3 Does ModelSim ME support the code coverage feature?

No, code coverage is a licensed option for ModelSim PE/SE. You need to purchase a license to use this feature.

Once you have a license, you need to set the code coverage option for compile and then load the design with coverage enabled and then the menus are enabled. The code coverage chapter of the *ModelSim User Manual* includes all the relevant information.

2.4 Is it true that ModelSim does not support the waveform save and comparison function?

Yes, ModelSim ME does not support waveform save and comparison function, for that you need ModelSim SE. In the Microsemi edition you can only export a bitmap (BMP) Image of the waveform.

2.5 Is there a way to force the primitive to not go X's in the simulation? In some silicon libraries, a nox notifier can be used? Is there something similar?

Our libraries are not set up to support the nox notifier. We do not have any way to do this in your simulation, if you have X values coming from a module, then we suggest that you initialize the module. Alternatively, you can use the force command, as shown in the following example.

Example: force signal_name 0 0, 1 200. It sets the signal to 0 at 0 ns and to 1 after 200 ns.

3 Library Issues

3.1 Where can I find the ModelSim simulation library for standalone users?

For Libero IDE v9.1 and later versions, the pre-compiled libraries are found in the folder:*<Libero9.1_install>\Designer\lib\modelsim\precompiled\vlog.*

Un-compiled libraries are under the folder *<Libero9.1_install>\Designer\lib\vtl\95\vlog.*

For Libero SoC, *<install_Folder>\Designer\lib\modelsim\precompiled.*

3.2 Do I need to add the specific family library statement into the VHDL source code for functional simulation?

If you have instantiated any Microsemi primitives in your VHDL source code, like HCLKBUF, then you need to add the specific family library statement in the source code for functional simulation.
For example:

```
library ieee;
use ieee.std_logic_1164.all;
library a54SXA; ----if your target device is a54SXA
entity Top is
```

3.3 When using ModelSim Standalone as part of the Libero IDE flow, how to fix the following error?

```
# -- Loading package standard
# -- Loading package std_logic_1164
# ** Error: (vcom-13) Recompile
```

If the preceding errors occur, you need to refresh the syncad_vhdl_lib library.

3.4 How can we use an older version of ModelSim with a newer version of Libero IDE/SoC or vice versa?

Whenever you use ModelSim versions, which differ by a number instead of a letter, you need to recompile the libraries. For example, ModelSim 10.3a and 10.3c can use the same pre-compiled libraries. However, if you move to ModelSim 10.4 then you need to recompile the libraries.

3.5 How to prevent the error ** Fatal: (vsim-3381) obsolete library format for design unit.

To prevent this error, right-click the relevant library in ModelSim and choose the refresh option. Re-compile the libraries if required.

3.6 Does Microsemi support ProASIC3 libraries for the Eagle EDA tool?

No, Microsemi does not support Eagle EDA.

3.7 The simulation file (ProASIC3.v) includes the register notify_reg. Is there any way to use this register? Also, if +notimingchecks switch with vsim is used in ModelSim, it disables all timing checks. So, can we mask some timing violations but not all?

notify_reg cannot be user-controlled. It is an optional register which does not change the behavior of the timing check.

This register is used to model the module behavior in the event of violations like setup/hold.

There is no way to disable the selected timing checks. Even if you change the value of that register, it does not disable the timing check.

3.8 When running Libero IDE/SoC on Linux, simulating the design using ModelSim results in the following error. How do we fix it?

```
# ** Error: (vsim-13)
Recompile /net/intsun03/export/home1/test_area/ModelSim_sol/modeltech/ac
tel/vhdl/ex.inbuf(vital_act) because
/net/intsun03/export/home1/test_area/ModelSim_sol/modeltech/sunos5acoem/../i
eee.vital_primitives has changed.
```

The technology libraries that are used for simulation are pre-compiled and need to be refreshed.

In ModelSim, go to the Library tab, right-click the technology library and choose refresh to fix this error.

4 License Issues

4.1 How do I get a free Libero License?

Perform the following the steps to install a free Libero license.

1. Go to the website: https://soc.microsemi.com/portal/default.aspx?r=1.
2. Enter your Customer Portal Login. If you don't have a portal login, create a new profile.
3. Once you login, click Request a Free License.
4. Select the Libero Evaluation or Silver Node Locked License for Windows.
5. Enter the Volume ID (DISK ID of the C: Drive).
6. Click Submit.

You receive new license file through the email address associated with your web portal profile with installation instructions.

4.2 # Microsemi version supports only a single HDL # ** Error: (vsim-3039) / Why doesn't a mixed HDL simulation run?

Microsemi supports ModelSim ME till Libero SoC v11.7 SP3, which can run simulation for either VHDL or Verilog HDL designs. Microsemi will support mixed language HDL simulation from Libero SoC v11.8 and later.

4.3 Is mixed language simulation supported in all the license types?

No, mixed language simulation is not supported in all the license types. For more information, see https://www.microsemi.com/products/fpga-soc/design-resources/licensing#overview.

4.4 ModelSim license parallel port dongle: I had Libero v8.0 and upgraded to v8.3 but now ModelSim is no longer working; it throws a license checkout error message. Why?

You need to install the updated driver from http://www.microsemi.com/products/fpga-soc/design-resources/licensing#downloads.

4.5 How to fix the Fatal License Error: Evaluation Error Code: 105

Check C:\Windows or C:\Windows\system32 folder for two files, mti_enc and mti_enc2 (ensure that the folder options are set to view hidden files/folder).

If the files are present, delete them and try Modelsim again.

4.6 How to fix the ModelSim License Error# ** Error: Failure to obtain a VHDL simulation license?

You may have merged another license with your Libero license, specifically one with server feature lines. Place these licenses individually to fix the error.

The system clock is set to a future date (system has files with future dates).

4.7 I installed Microsemi Libero. I am able to open the Libero project manager but cannot open ModelSim. It is not giving any warning or error. But if I click ModelSim from the project manager, it shows the ModelSim icon and then does not open anything. Why?

Redundant ModelSim license causes this issue.

Example:

```
LM_LICENSE_FILE or MGLS_LICENSE_FILE =
27008@10.100.33.206;27008@10.100.33.203;27008@10.100.33.205;C:\flexlm\Licens
e.dat;
```

Search in all drives in PC for license.dat and see whether it resides only in the following location: C:\flexlm\license.dat

If the file is present in some other location, then delete the duplicate.

Also, if you have the license file for the full version ModelSim, you need to delete it.

5 ModelSim Features

5.1 How do I set the simulation run time?

Libero automatically sets the simulation run time to 1000 ns.

5.2 How do I set the time in ModelSim so it runs 6 ns?

1. In Libero IDE project manager, right-click the ModelSim icon and choose Options.
2. Change the simulation runtime and click OK. The automatically generated `run.do` reflects your selected runtime.
3. In Libeo SoC, Project > Project Settings > DO file.

5.3 How do I turn off the warning message in ModelSim?

In ModelSim, select *Simulate>Runtime Options>Message Severity>Select Warning tab*

5.4 How can I turn off the ModelSim vital glitch warning during the post-layout simulation?

Use the +no_glitch_msg flag for the vsim command. Though it is not always recommended, it is useful to look at the real problem (setup or hold)

Example:

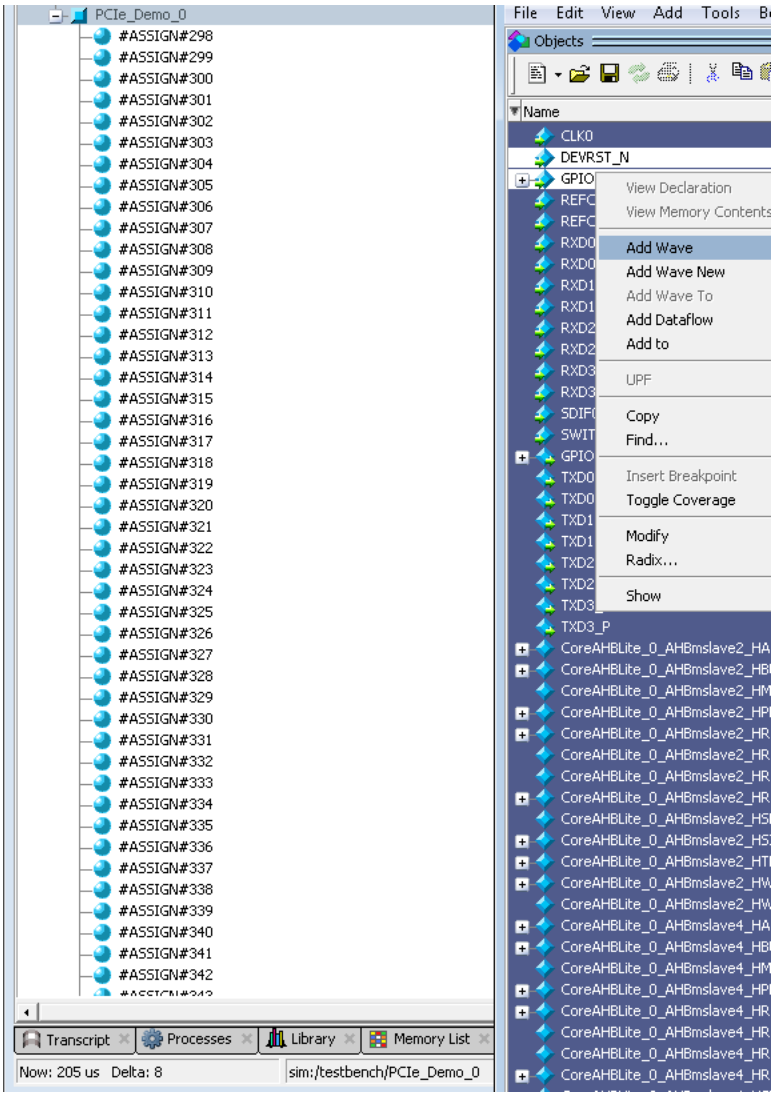
```
vsim +no_glitch_msg -L apa -L postlayout -t 1ps -sdfmax
/berkana_0=D:/FA/project_dir/TestVector/designer/impl1/berkana_ba.sdf
postlayout.testbench
```

5.5 How can I view the sub module signals in the ModelSim wave window?

You can add sub module signals by browsing through the hierarchy and selecting the sub module from the ModelSim command window, then select ViewSignals from ModelSim pull down menu.

In the Signal window, you can highlight the signals you want to add in the Wave window, then click, Add Wave to add the signals in the waveform, as shown in the following figure.

Figure 1 • **Signal Window**



Restart the simulation and run it again. If you want to save the wave format you have added into the wave window, use the command Save Format inside the Wave window.

5.6 How can I retain my radix in the wave window after I manually change them to a desired value for all simulations in a particular project?

If you want certain signals to have a different radix, then you need to set these manually and use the Save format menu to save these values to a `wave.do` file that you can execute with the do `wave.do` command.

In the Libero environment you need to change a line in the `run.do` file (include do `wave.do` command in the script) and save the `run.do` file as `run1.do`. In Project > Settings > Simulation use this `run1.do` instead of the default `run.do`.

5.7 How can we group a bus for viewing a simulation result?

Here is an example of grouping a signal in a `run.do` file:
virtual signal

```
{sim:/testbench/top_0/u1/\count[15] /Q &
sim:/testbench/top_0/u1/\count[14] /Q &
sim:/testbench/top_0/u1/\count[13] /Q &
sim:/testbench/top_0/u1/\count[12] /Q &
sim:/testbench/top_0/u1/\count[11] /Q &
sim:/testbench/top_0/u1/\count[10] /Q &
sim:/testbench/top_0/u1/\count[9] /Q &
sim:/testbench/top_0/u1/\count[8] /Q &
sim:/testbench/top_0/u1/\count[7] /Q &
sim:/testbench/top_0/u1/\count[6] /Q &
sim:/testbench/top_0/u1/\count[5] /Q &
sim:/testbench/top_0/u1/\count[4] /Q &
sim:/testbench/top_0/u1/\count[3] /Q &
sim:/testbench/top_0/u1/\count[2] /Q &
sim:/testbench/top_0/u1/\count[1] /Q &
sim:/testbench/top_0/u1/\count[0] /Q } count_vector
add wave -noupdate -format Literal -radix decimal
/testbench/top_0/u1/count_vector
```

5.8 How do I simulate with multiple SDF files?

To simulate with multiple SDF files, you can do the following modification in your `run.do` file:

```
vsim -L fusion -L postlayout  -t 1ps -sdfmax /Project_Dir/File1.sdf  -sdfmax
/Project_Dir/File2.sdf  -sdfmax /Project_Dir/File3.sdf postlayout.testbench
```

Ensure that each SDF file corresponds to a specific top-level module in your netlists.

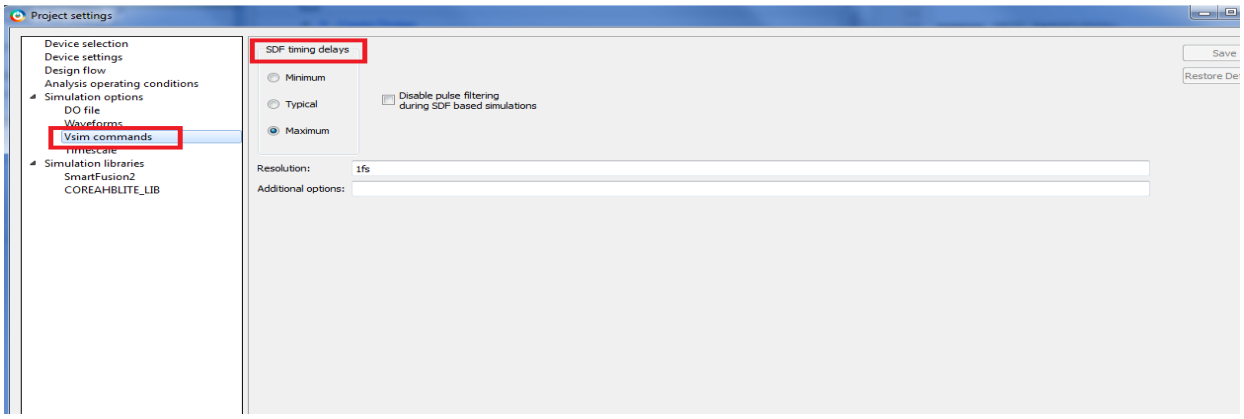
5.9 ModelSim runs the simulation for the worst case temperature value. How can we simulate our design for both the best and worst case temperature values on ModelSim?

For Libero SoC

Set the temperature values in the Libero SoC project manager before running the simulation in ModelSim.

Set this option in the project manager Project settings. Review the SDF timing delays. You can choose **Max** (worst case), **Typ** (nominal), and **Min** (best case).

Figure 2 • **Project Settings Window For SoC**



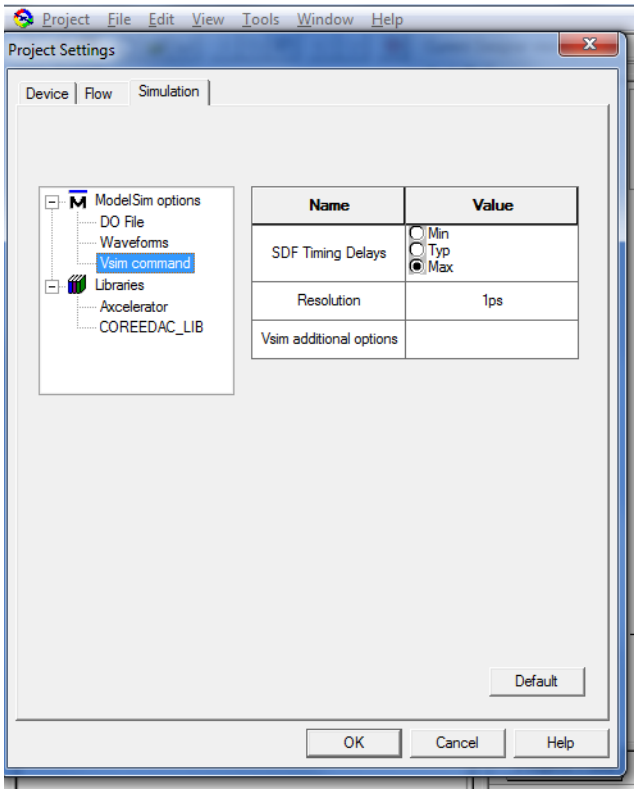
For Libero IDE

Set the temperature values in the Libero IDE project manager before running the simulation in ModelSim.

For Libero IDE, Project > Settings > Simulation.

Set this option in the project manager Project settings. Review the SDF timing delays. You can choose Max (worst case), Typ (nominal), and Min (best case).

Figure 3 • **Project Settings Window For Libero IDE**



5.10 Is it possible to simulate the JTAG interface within ModelSim?

Yes, it is possible to simulate the JTAG interface, if UJTAG macro is instantiated in the design. In this case, the simulation emulates some functionality of the JTAG interface as seen from the FPGA chip. Check the simulation library file (search for UJTAG): `~Designer\lib\vlog\igloo.v`

5.11 My post-synthesis simulation is different from my pre-synthesis simulation. Why?

Review the synthesis log. In some cases, your RTL code has some initialization or functions that are not used and may be removed during synthesis.

5.12 Pre synthesis simulation runs but post synthesis simulation displays all outputs in red. Why?

Check the Reset signal.
You may not have power on reset on the internal registers.
You need to apply reset. If it is floating, it causes the module to initialize to unknown and then it remains unknown forever.
This does not happen in silicon. In silicon, it is in a specific state (most likely all zeros). So, you can perform either of the following steps:

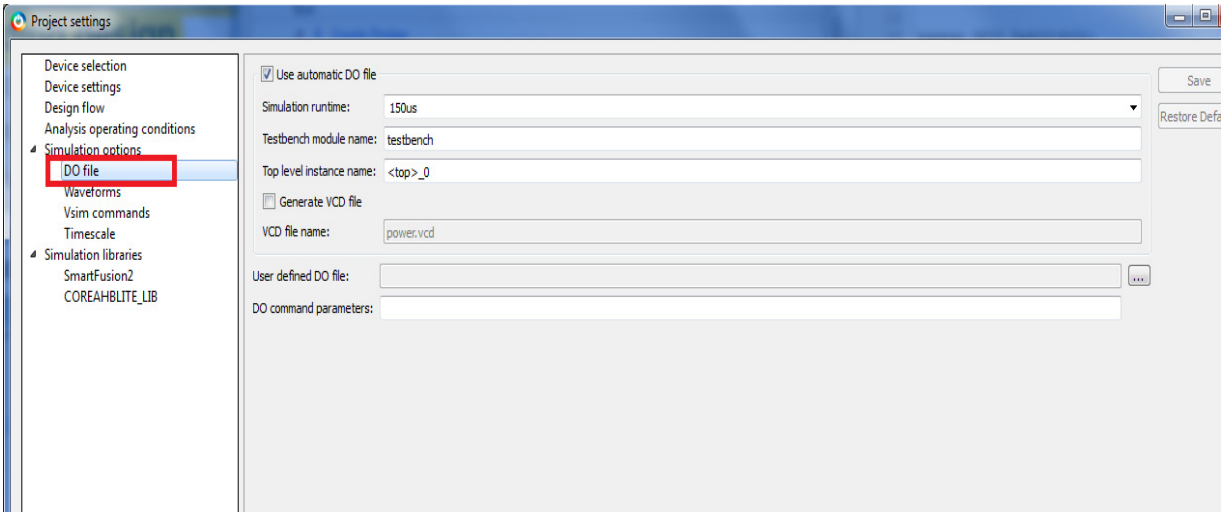
- Apply reset signal and change the code.
- Force the FFs/registers to reset by using the ModelSim force command.

5.13 **Error: (vsim-3170) Count not find "<Project_Dir>\simulation\presynth.testbench Error loading design

ModelSim simulation options must not have been set properly. Go to
Project Settings > ModelSim > Options and make the following changes (see the following figure):

1. Right-click the Simulation tab in the Project Flow window or select Project > Settings > Simulation.
2. Testbench module name: Specify your testbench module name.
3. Top-level instance name in the testbench: Instance name of the DUT.

Figure 4 • **ModelSim Simulation**



5.14 #error: (vsim-23) unable to change to directory path postsynth.test #No such file or directory (errno=ENOENT).

ModelSim simulation options must not have been set properly. Go to Project Settings > ModelSim > Options and make the following changes:

1. Right-click the Simulation tab in the Project Flow window or select Project > Settings > Simulation.
2. Testbench module name: Specify your testbench module name
3. Top-level instance name in the testbench: Instance name of the DUT

See Figure 4, page 13 for an example.

6 Post-Layout Simulation Errors

6.1 Why does the simulation show no violation of setup and hold times, but the simulator returns a warning?

This issue is caused by incorrect interpretation of the delays. Cross check if you are looking at the correct signals.

6.2 Why there is a difference between the results of the static timing analysis in the designer and post-layout simulation with ModelSim?

This issue is caused by incorrect interpretation of the delays. Cross check if you are looking at the correct internal signal.

6.3 How to fix the timing violation errors or warnings during post layout simulation?

For example see the following error message:

```
# ** Error:
C:/Microsemi/Libero_v9.2/Model/win32acoem/../../Designer/lib/modelsim/precom
piled/vlog/src/<fpga_fam>(8363): $setup (posedge D:30272700 ps, posedge CLK
&&& Enable1:30273400 ps, 900 ps);

#    Time: 30273400 ps Iteration: 1 Instance: /testbench/NJFPGA_0/\$1I255
/\$1I227
```

The error messages contained in the ModelSim simulation error log are actually timing violation errors, notifying you about timing violations in a post-layout back annotated timing simulation with respect to the setup, hold, and pulse width restrictions specified in the device library and in the SDF timing delay file for the design under test. You must evaluate each message and determine, if there is a legitimate timing issue with the design that causes the design not to function or if you can ignore certain errors.

The example error says that Instance /testbench/NJFPGA_0/\$1I255 /\$1I227 of the design shows a setup time violation on the positive edge of a flip-flop. It shows that the minimum setup time on the D port is 900 ps, but from the simulation, only 700 ps setup time is used (posedge of D at 30272700 ps, while posedge of CLK comes at 30273400 ps). These checks are coded into the device library source file and the delays for the specific instances of the design are in the SDF file. These messages may appear, if you are missing the timescale definition in the testbench but have defined in design files.

7 Known Issues

7.1 When I run ModelSim, my computer hangs, with vsimk.exe at 100% CPU usage. I cannot shut down ModelSim during this time. I must wait for 10 minutes until vsmik.exe stops running. Why?

This is a known issue with the co-existence of two versions of ModelSim (non Microsemi versions). Uninstall one version. Mentor tools conflict with each other, if same tool is installed twice.
You need to uninstall one of them. If you want to keep ModelSim that is not part of the Libero then in Libero tools profile, link it (link the modelsim.exe file location).

7.2 In PLL simulation (pre-synth, post-synth, and post route) some output frequencies do not show up as expected. Why?

This issue is for simulation only. The silicon does not have this problem.
This is caused by round-off in the PLL simulation model. For example, a PLL is generated with 25 MHz input, 300 MHz, and 100 MHz output. 25 MHz clock has a period of 40000 ps. In order to generate both 300 MHz and 100 MHz output clocks, the input clock period is first divided by 12 (to generate the 300 MHz clock) and then multiplied by three (for the 100 MHz clock). When 40000 ps is divided by 12, the result is 3333.333 ps. The model rounds this up to 3334 ps. When 3334 ps is then multiplied by three, the result is 10002 ps. This causes the 100 MHz and 300 MHz clocks to appear to drift relative to the 25MHz input clock.

7.3 Post-synthesis and post-layout simulation give invalid results for the INOUT bus. INOUT bus with initial value 'U' within netlist causes unknown in post-synthesis and post-layout simulation. How do I get a valid result?

1. If speed is not a critical design issue, then the turn off cross-boundary optimization in Synplify by using the syn_hier = hard attribute in synplicity to stop reconstruction of the hierarchy block, and to stop generating the INOUT bus. The corresponding HDL netlist generated by the designer, results in correct simulation.
2. If cross-boundary optimization is required to improve performance, post-synthesis and post-layout HDL netlists need manual modification. Add initial value Zs to the INOUT bus at the entity port declaration.
   For example:

Entity Remove_Unknown is Port (A: in std_logic; B: in std_logic; INOUT_BUS: inout std_logic_vector (7 downto 0) := (others => ‘Z’); - - <- Add initial value ‘Z’ here C: out std_logic); End Remove_Unknown;

After this modification, post-synthesis and post-layout simulation give valid results for the INOUT bus.

7.4 SmartPower does not annotate all pins when the VCD file generated by ModelSim is imported into designer. Why?

Close to 100% annotation can only be expected, if you are importing a post-layout VCD. If you import pre-synthesis and post-synthesis VCDs, the SmartPower netlist is different from the netlist that was simulated.

Remove all escaped characters in the VCD file manually. For example, if the VCD file is as follows:

```
$var wire 1 - \cnt_c[0]\ $end
$var wire 1 . \cnt_c[1]\ $end
$var wire 1 / \cnt_c[2]\ $end
$var wire 1 0 \cnt_c[3]\ $end
```

Modify the signal as:

```
$var wire 1 - cnt_c[0] $end
$var wire 1 . cnt_c[1] $end
$var wire 1 / cnt_c[2] $end
$var wire 1 0 cnt_c[3] $end
```

Re-import the modified VCD file into Designer.

8 Miscellaneous

8.1 Why does Modelsim exit with error code 211 for all the projects?

It may be related to anti-virus software, blocking the Modelsim. Disable the anti-virus, install the ModelSim and check if the tool passes the simulation (anti-virus should be disabled for the entire process).

8.2 How to fix the ModelSim Simulation Error #**Fatal:(vsim-3881)?

Check the vsim command line to ensure that the correct testbench is targeted.

8.3 How do I simulate two Microsemi field programmable gate arrays together in a system simulation?

Libero IDE cannot handle multiple designs at once, but ModelSim can. Create a top-level netlist with the two devices, then modify the inputs/outputs in the SDFs to take into account the delays between the two devices. Run ModelSim, simulate the new top-level, but load the SDFs for each device. (To specify a SDF for an instance within a design, see the *ModelSim SE-PE in Libero SoC User Guide*.

8.4 Failed to find instance # ERROR: C:/Designs/annotations/interface.sdf(15): Failed to find INSTANCE '/testbench/ramwrn_1' # ERROR: C:/Designs/annotations/interface.sdf(24): Failed to find INSTANCE '/testbench/block_1'

The problem is that the instance hierarchical path that is mentioned does not exist in the loaded design. By default, the hierarchical path is used in the top-level entity (testbench) concatenated with the instance path that exists in the SDF file (ramwrn_1). The top-level entity is thus considered the region, the level of hierarchy that is applied to the SDF file. This default region is used if no specific region is supplied. Excerpt from C:/Designs/annotations/interface.sdf file

```
(CELL
(CELLTYPE "BUF")
(INSTANCE ramwrn_1) // SDF file instance path
(DELAY
(ABSOLUTE
(IOPATH I0 O (20:20:20) (20:20:20) )
)
)
)
```

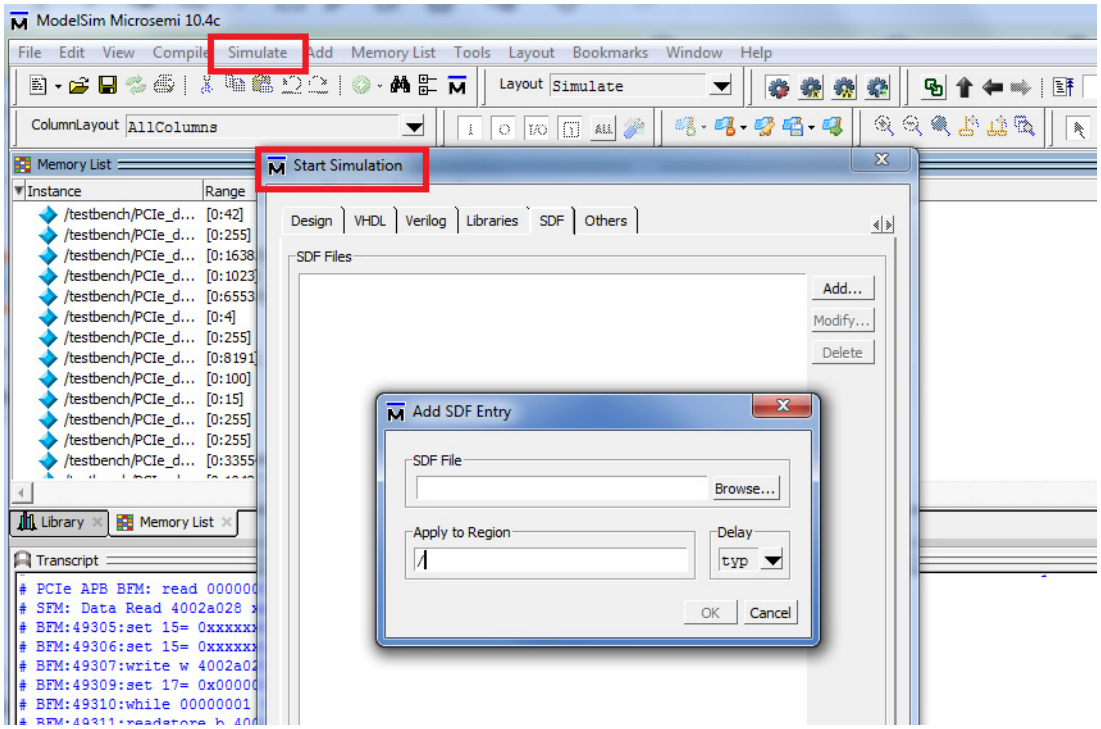
Typically, an SDF file is written without the knowledge of a top-level testbench in the design hierarchy and therefore the default path is incorrect. This is a very common scenario. There are other scenarios where you are only annotating data to a portion of the design and you need to specify the level of the hierarchy that is applied to the SDF file.

In the example, the correct region is the testbench entity name (testbench) and then the instantiation name of the design (dut) in the testbench architecture, not the design entity name. Therefore, the region would be "/testbench/dut".

To specify the region in ModelSim, from the command line type: -sdftyp <region>=<SDF file path/name>

Command line for this example: vsim -sdftyp /testbench/dut=./annotations/interface.sdf testbench

Figure 5 • **Add SDF Entry Window**



Note: This example uses the C:/Designs directory. The instance hierarchical path would now be /testbench/dut/ramwrn_1, which is a valid path in the design, and not the default /testbench/ramwrn_1.

If the default path does not work, you must ensure that the region concatenated with the instance path in the SDF file results in a valid hierarchical path that exists in the loaded design.

8.5 How to fix # Error: could not open socket: invalid argument Trouble making server

Check firewall, anti-spyware, and anti-virus settings to ensure that the `vish.exe` and `vsimk.exe` are allowed to run.

8.6 How to ** Error: (vsim-3174) Package 'D:\Microsemi\Libero_v9.1\Model\std.standard' requires a body?

If you get this message for the standard package, this package is corrupted and you need to uninstall and reinstall the ModelSim.

To do so, from the Start menu choose **All Programs > Microsemi Libero IDE v9.1 > Uninstall and Modify Libero IDE** and follow the instructions in Install shield to repair the ModelSim installation.

8.7 Why are the back annotated timing results different from what I can see in SmartTime?

Check the timescale defined at the top of the SDF file (usually set as timescale 100 ps). This means that 100 unit delay would actually mean a 10 ns delay.

8.8 In Libero IDE project manager settings there is a way to send extra command line arguments to the VSIM command. Is there a way to add a command line argument to the vlog command?

No, you cannot use the project manager GUI to add an argument to the vlog command.

You can modify the `run.do` script that Libero automatically generates and add your extra command line arguments to the vlog command in the `run.do` script.

In your Libero project simulation folder, there is an auto-generated `run.do` script (This script is auto-generated if any simulations are invoked from Libero IDE project manager). You can modify this `run.do` script to add your extra vlog arguments. Note that the project manager automatically generates the appropriate `run.do` script depending on whether a pre-synthesis, post-synthesis, or post-layout simulation is run (because the source files differ).

If you want to take manual control over this scripting process, after running each type of simulation, save a copy of the `run.do` script in your project's simulation folder are ensure you name it appropriately (that is `run_presyn.do`). Once you have a sample of the `run.do` script for each type of simulation, you modify the scripts as needed, then disable the automatic `run.do` script creation in project manager and manually specify which script must be used before each simulation using the **Project >Settings >Simulation tab**. You can find the vlog arguments listed in the ModelSim command reference at *ModelSim User Guide*.

8.9 What is the solution if the below error is observed ** Fatal: SDF files require Microsemi primitive library?

If the user is using pre-compile libs for Modelsim SE release, this error is observed. For Modelsim SE release, the user must use the source library files (not applicable for SmartFusion2 and IGLOO2). Compile the libs and use them in their design.