eX Frequently Asked Questions

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I. Architecture

I.1.Clocks

1. How many clock pins are available in eX?

Ans. There is one Hardwired clock pin and two Routed clock pins.

2. What is the difference between Hardwired and Routed clocks?

Ans. The Hardwired clock is connected directly to the Clock pin of all the Flip-Flops. For this connection there is no need for a fuse or a mux (that selects between the Pad and an internal node).
For an identical load (fanout), the Hardwired clock is faster than the Routed clock.

3. If not used, what do I have to do with the clock pins?

Ans. Unused clock pins must not be floating. You must tie them to GND or VCC. Actel recommends grounding them.

4. If I use a CLKINT buffer, are the CLKA and CLKB still available as normal IOs?

Ans. If you use one CLKINT buffer, only one more routed clock is available. If you use two CLKINTs, no routed clocks are available. Any unused external clock input pins must not float; Actel recommends grounding them.

5. Why is the Routed clock faster than the Hardwired clock in some cases?

Ans. This may happen if the loading of a Routed clock is very low when compared to the load or fanout of a Hardwired clock. But for a similar fanout, the Hardwired clock is normally faster.

6. What can the Routed clock network connect to?

Ans. The routed clock can be connected to the following. Please refer to Figure 3: *Cluster Organization* in the *eX Family FPGAs* datasheet.

A0, A1, B0 and B1	pins of a	C-cell
RCLK, S0, S1, PSETB, CLR	pins of a	R-cell
EN	pin of a	IO-cell

For all other connections, Designer automatically inserts a BUFF macro between the routed clock and the destination pin.

7. What signals can drive the R-Cell clock pin?

Ans. Any internal or external signal can drive the clock pin of an R-cell.

I.2.Reset

8. Is there any global reset in the eX devices?

Ans. Any of the routed clocks can be used as a global reset, but there is no built in reset circuitry in the device.

I.3.IOs

9. Are the eX IOs registered?

Ans. No. However, the combination of the IO with a core logic register allows a Clock-to-Out delay less than 4.6 ns.

10. What does the power-up pull-up/pull-down mean?

Ans. During power-up and only during this short time, the IOs are either pulled-up or down. But as soon as the charge pump is ON, the IOs pull-up/down goes away.

11. What is the value of the power-up pull-up and pull-down resistors?

Ans. Approximately 50KΩ.

12. Which eX IO features are individually selectable?

Ans. The slew-rate and Power-up Pull-up and Pull-down resistors are individually selectable.

13. Do the eX IOs have individual slew control?

Ans. Yes, there is a programmable fuse to control the slew of individual eX IOs, you can select the High or Low slew rate in PinEdit of Designer software on an individual I/O basis.

14. How can I get the max source/sink current for eX?

Ans. Please refer to the IBIS model on the Actel website:

http://www.actel.com/custsup/models/ibis.html#sxa (eX and SX-A are the same) and refer to the readme file http://www.actel.com/user/ibis/README.txt to get the max source/sink current.

I.4.Low-Power Mode

15. How long should the low-power mode pin/signal be asserted before it is recognized?

Ans. You have to set the LP pin to "1" for a period larger than 800 ns.

16. What's the status of the IOs and the core logic when the device is in low-power mode?

Ans. The IOs are tri-stated and the charge pump is disabled. The internal registers' values are lost. Clock pins should be stopped and should not float, otherwise they will draw current and burn power.

17. When the eX is in low power mode, can the IOs be driven?

Ans. Yes, the I/Os can be driven during LP mode. For details please refer to the *Design For Low Power in Actel Antifuse FPGAs* application note under the section *Using the LP Mode Pin on eX Devices:* http://www.actel.com/documents/Low_Power_AN.pdf

18. How long does it take an eX device to exit the low power mode?

Ans. It is equal to the time required by the charge pump to power up. A fair and safe period estimation is about 200 µs for the largest eX device. It is shorter for the smaller ones, but 200 µs is safe.

19. In eX low-power mode, are the power-up pull-up and pull-down resistors active?

Ans. No. This feature is active for a very short time during the normal power-up and not during the exit from the low-power mode.

20. How is the internal register reset done after a low-power mode?

Ans. Once LP is set to "0" for over 200 µs, initialization can take place. The eX family does not have a dedicated global reset pin, however, users can design one of the Routed clocks to be used as a global reset in the device.

21. What is the power-up sequence when exiting a low-power mode?

Ans. Set the LP pin to "0"; wait for the pumps to come-up (200 µs) and then start initialization.

II. Features

II.1.Hot Swap IOs

22. What are the hot swap capabilities of eX?

Ans. eX IOs are specifically designed to be programmed for hot swapping applications. During power-up/down (or partial power-up/down), all IOs are tri-stated. Please refer to the application note regarding hot-swapping silicon requirements *Actel SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications*: http://www.actel.com/documents/HotSwapColdSparing_AN.pdf

II.2.JTAG

23. If JTAG pin is not reserved, is a JTAG IO available as a normal IO?

Ans. If the JTAG is not reserved as dedicated test mode, then TCK, TDI and TDO are flexible and may be used as normal I/Os. TMS should be set HIGH through a pull-up resistor of 10KΩ.

24. Does eX provide the JTAG reset pin TRST?

Ans. Yes, there is a JTAG reset TRST pin, which you can program as a dedicated JTAG reset pin or use as a regular IO.

25. The *eX Family FPGAs* data sheet recommends a 10k pull-up resistor on TMS in flexible mode. Are there any resistor values recommended for pull-ups for TCK, TDI, TDO and pull-down for TRST?

Ans. The10K pull-up is what the IEEE JTAG specification recommended for TMS, TDI, and TRST pins (not TCK and TDO). In "flex" mode, only the TMS pin needs to have the pull-up resistor, TDI is a user IO in this mode.

As for the TRST pin, it is an "active low" pin. It needs a pull-up resistor rather than a pull-down resistor (pull-down forces the JTAG TAP controller to remain in the test-logic-reset state).

II.3.Voltages and Power-up Sequencing

26. What voltages do eX IOs tolerate?

Ans. The eX IOs are always 5V tolerant, regardless of V_{CCI}. Thus, even if they are configured at 2.5V or 3.3V, the I/Os are 5V max tolerant.

27. Is the reference voltage Vccr required for eX?

Ans. eX packages do not have such a pin. eX does not require the reference voltage V_{CCR}.

28. What's the logic core voltage supply for the eX family?

Ans. The core logic always requires 2.5V as supply.

29. How many supplies do I need for eX?

Ans. eX can run with 2.5V single supply for V_{CCA} and V_{CCI}. Elsewhere, it needs two power supplies, V_{CCA} (2.5V only) and V_{CCI} (3.3V or 5V).

30. What happens to an eX chip when it's not powered up and voltages are applied to the IOs?

Ans. All of the IOs are tri-stated when it is not powered up. Therefore, no current flows into the eX chip when you apply voltages to the IOs. This will not damage the eX devices.

31. The eX datasheet shows a large difference in the electrical specifications between 3.3V and 5.0V, such as 1.5mA max ICC @3.3V VCCI, and 15mA ICC @ 5.0V VCCI. Is this the real value?

Ans. These are the real MAX values that we test to. But it may be much lower in real application.

32. Is there power up/down sequence required for eX device?

Ans. There is no specific power up/down sequence requirement for eX device to avoid damage the device.

33. What's the status of eX IOs during power-up?

Ans. During power-up/down (or partial power-up/down), all IOs are tri-stated if VCCA ramps up within a diode drop of VCCI. In addition, all outputs can be programmed to have a weak resistor pull-up or a weak resistor pull-down for output tri-state at power-up. But if VCCA ramps up after VCCI and more than a diode drop below it, outputs

may drive to an unknown state for a short period of time during power up regardless of power-up resistor setting.

II.4.IO Features

34. What are the drive capabilities of eX outputs?

Ans. The drive capabilities of eX outputs are dependent on the V_{CCI} (as illustrated in the Table below.)

V_{CCI}	Output Drive
2.5V	2.5V
3.3V	3.3V
5V	5V

35. Can I interface the eX IOs with LVTTL or LVCMOS ?

Ans. Yes, eX is designed to interface with LVTTL and LVCMOS at 3.3V VCCI.

36. Are the eX IOs PCI compliant?

Ans. No. For PCI compliant feature, you need to use the SX-A family.

37. What's the state (status) of unused IOs?

Ans. All of the unused IOs are configured as tri-state out by Actel Designer software.

II.5.CC Macros and Latches

38. Can R-Cell implement a Latch?

Ans. No, Latches are made with two C-cells.

39. What are the timing attributes (T_{SUD}, T_{CC-CO}) of a CC-macro?

Ans. Based on 54SX-A family tests, the typical results reported by the timing engine of Designer for a "-3" speed grade are summarized in the table below.

Macro	Clk-to-Q (rising)	Clk-to-Q (falling)	Input Setup time
DF1	1.0 ns	1.1 ns	0.5 ns
DF1_CC	1.4 ns	1.4 ns	0.7 ns
DFC1B	1.0 ns	1.1 ns	0.5 ns

DFC1B_CC	1.4 ns	1.4 ns	0.7 ns
DFP1B	1.0 ns	1.1 ns	0.5 ns
DFP1B_CC	1.4 ns	1.4 ns	0.7 ns

40. What are the various FF configurations a CC macro can implement?

Ans. There are three (3) configurations that a CC macro can implement:

- DF1_CC D-type flip-flop
- DFC1B_CC D-type flip-flop with active low clear
- DFP1B_CC D-type flip-flop with active low preset

41. Can I use the hardwired clock to drive a CC macro?

Ans. No. Also, you need to be aware that you cannot replace R-cells driven by the HCLK by CC macros. This is because HCLK has dedicated routing connections to the clock inputs of regular R-cells and not to C-cells. However, you can use CLKA, CLKB, and internal generated signals to drive the clock pin of a CC macro.

III. Packaging & Speed Grades

42. What's a Chip Scale Package (CSP)?

Ans. Chip scale packaging was introduced in Japan in the early 1990s, and presented in the United States later in 1994. The argument was that CSP is a less expensive alternative to multi-chip modules (MCMs). Since then, the volume and the adoption of CSP have exploded. There are various package styles that fit the definition of a CSP, some being little more than the chip itself. Most demand for these shrinking parts comes from the personal appliance market, where more functions are being placed in smaller spaces.

The "adopted" definition of a CSP:

> CSP is a package that has a perimeter no more than 20% larger than the perimeter of the die. CSPs offer the same space and material savings and short signal paths as direct chip attach methods.

43. What are the advantages of CSP?

Ans. The advantages to using CSP over other packages are: easier handling, more protection for the chip and simpler board assembly.

44. What materials are used in Actel's CSP packages?

Ans. CSP - Chip Scale Package
* Substrate: BT (Bismaleimide Triazine) - laminate
* Die Attach Material: Ablebond 8510AA (Conductive)
* Filler Type: Ag
* Wire Type: 1.0 mil Au
* Composition: 99.99% Au
* Mold Material: Nitto HC100-XGA
* Solder Ball Composition: 62%Sn/36%Pb/2.0%Ag
* Ball Pitch: 0.8 mm

45. What are the differences between the CSP, FBGA and BGA packages?

Ans. The ball pitch for the CSP is 0.8 mm, for the FBGA is 1.0mm and for the BGA is 1.27mm. The smallest CSP in the eX family, the CS49, will have a body size of only 7mm x 7mm. The CS128 will be 11mm x11mm versus the FG144 at 13mm x 13mm. One cost barrier to wide adoption of CSPs is productivity at assembly and test. With assembly capabilities currently available, the largest productivity barrier is testing.

IV. eX vs. SX-A

46. How is eX different from SX-A?

Ans. eX extends Actel advanced 0.22 micron antifuse technology to lower densities and adds a Low Power Mode as well as chip-scale packages. eX does not support PCI and has different speed grades.
SX-A supports a larger set of Clock buffer macros than eX.

47. How do the eX speed grades compare with SX-A speed grades?

Ans. The eX speed grades match with the SX-A ones as follows:
- eX STD is 5% faster than the SX-A STD
- eX -F is 5% faster than an SX-A -F.
- eX -P is equal to SX-A –3

48. What are the SX-A macros that are not supported for eX?

Ans. The following macros are NOT supported for the eX family:
- CLKBIBUF
- CLKBIBUFI
- QCLKBUF
- QCLKBUFI
- QCLKBIBUF

- QCLKBIBUFI
- QCLKINT
- QCLKINTI

49. Can I retarget an SX08-A design to eX?

Ans. Yes. However you must make sure that if your design does not use PCI compliant IOs and you must ground the Low-Power mode pin.
Also, you have to check the list of QCLK* and CLKBIBUF* macros listed in the previous question as they are not supported for eX.

50. Is the eX pin compatible with SX-A?

Ans. Only the TQ100 package is common to eX and SX08A/SX16A.Please notice the highlighted differences in the following table.

	eX128-TQ100	SX08A-TQ100		eX128-TQ100	SX08A-TQ100
Pin #	**Function**	**Function**	**Pin #**	**Function**	**Function**
1	GND		51	GND	
2	TDI, I/O		**52**	**NC**	**I/O**
3	**NC**	**I/O**	**53**	**NC**	**I/O**
4	**NC**	**I/O**	**54**	**NC**	**I/O**
5	**NC**	**I/O**	55	I/O	
6	I/O		56	I/O	
7	TMS		57	VCCA	
8	VCCI		58	VCCI	
9	GND		59	I/O	
10	I/O		60	I/O	
11	I/O		61	I/O	
12	I/O		62	I/O	
13	I/O		63	I/O	
14	I/O		64	I/O	
15	I/O		65	I/O	
16	TRST, I/O		66	I/O	
17	I/O		67	VCCA	
18	I/O		**68**	**LP/GND**	**GND**
19	I/O		69	GND	
20	VCCI		70	I/O	
21	I/O		71	I/O	
22	I/O		72	I/O	
23	**NC**	**I/O**	**73**	**NC**	**I/O**
24	**NC**	**I/O**	**74**	**NC**	**I/O**
25	I/O		**75**	**NC**	**I/O**
26	I/O		76	I/O	
27	I/O		77	I/O	
28	I/O		78	I/O	
29	I/O		79	I/O	
30	I/O		80	I/O	
31	I/O		81	I/O	

32	I/O	
33	I/O	
34	PRB, I/O	
35	VCCA	
36	GND	
37	NC	
38	I/O	
39	HCLK	
40	I/O	
41	I/O	
42	I/O	
43	I/O	
44	VCCI	
45	I/O	
46	I/O	
47	I/O	
48	I/O	
49	TDO, I/O	
50	I/O	

82	VCCI	
83	I/O	
84	I/O	
85	I/O	
86	I/O	
87	CLKA	
88	CLKB	
89	NC	
90	VCCA	
91	GND	
92	PRA, I/O	
93	I/O	
94	I/O	
95	I/O	
96	I/O	
97	I/O	
98	I/O	
99	I/O	
100	TCK, I/O	