

NEC

TFT COLOR LCD MODULE

NL3224BC35-20

13.9cm (5.5 Type)

QVGA

DATA SHEET

(5th edition)

PRELIMINARY

All information is subject to change without notice.

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Display Device Operations Unit
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INTRODUCTION

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Anti-radioactive design is not implemented in this product.

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1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

NL3224BC35-20 module is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight unit.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a color-filter glass substrate.

Color (Red, Green, Blue) data signals from a host system (e.g. PC, signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Color images are created by regulating the amount of transmitted light through the TFT array of red, green and blue dots.

1.2 APPLICATIONS

- Industrial PC
- Display terminal for control system
- POS (Point of sale) terminal

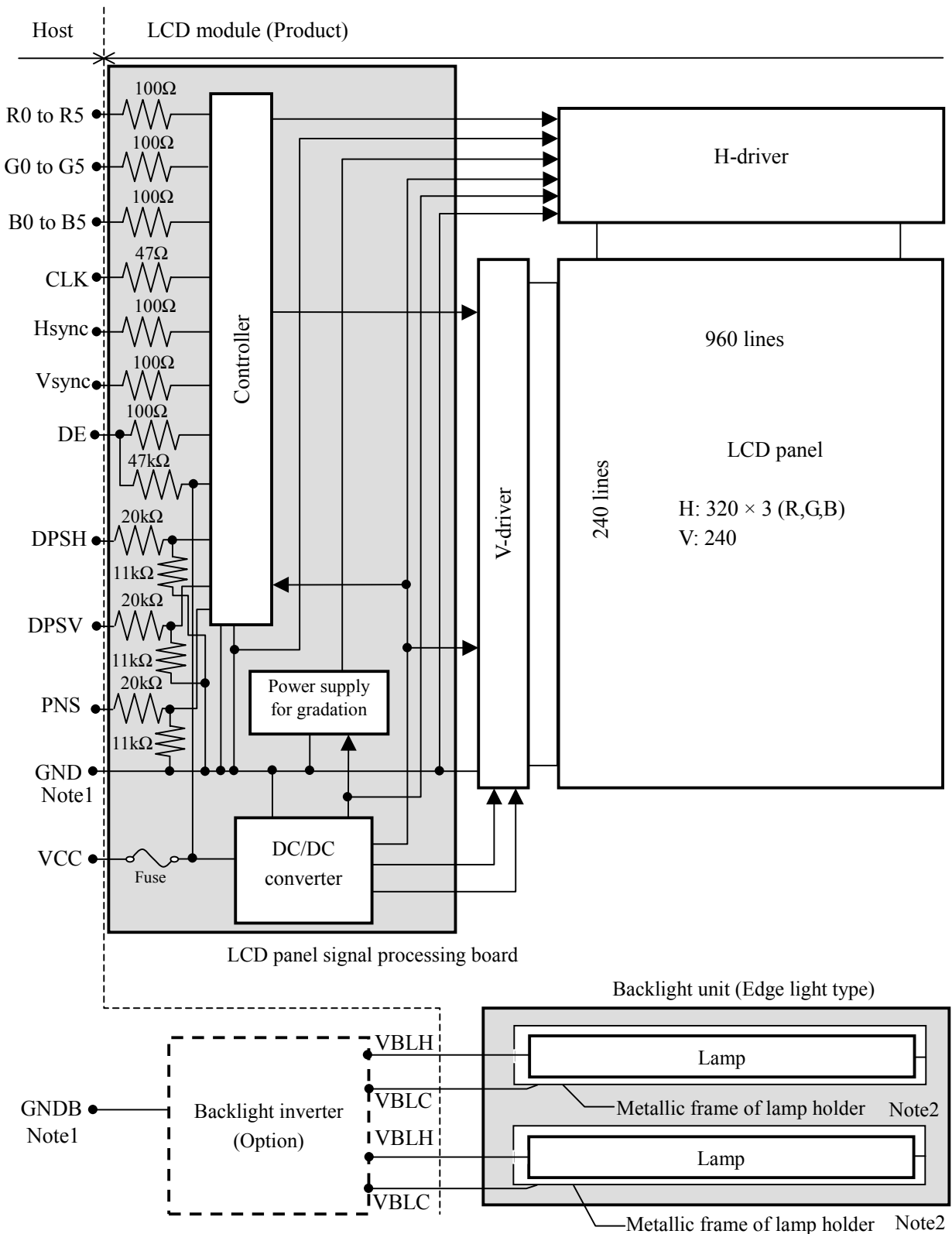
1.3 FEATURES

- High luminance
- High color gamut
- Wide viewing angle
- Low reflection
- 6-bit digital RGB signals
- Reversible-scan direction
- Edge light type
- Replaceable lamp for backlight unit (Inverter less)

2. GENERAL SPECIFICATIONS

Display area	111.4 (W) × 83.5 (H) mm (typ.)
Diagonal size of display	13.9 cm (5.5 inches)
Drive system	a-Si TFT active matrix
Display color	262,144 colors
Pixel	<i>At QVGA display mode</i> 320 (H) × 240 (V) pixels <i>At VGA display mode</i> 640 (H) × 480 (V) pixels
Pixel arrangement	RGB (Red dot, Green dot, Blue dot) vertical stripe
Dot pitch	0.1160 (W) × 0.3480 (H) mm
Pixel pitch	0.3480 (W) × 0.3480 (H) mm
Module size	134.0 (W) × 104.5 (H) × 12.5 (D) mm (typ.)
Weight	215 g (typ.)
Contrast ratio	400:1 (typ.)
Viewing angle	<i>At the contrast ratio 10:1</i> • Horizontal: Left side 65° (typ.), Right side 65° (typ.) • Vertical: Up side 65° (typ.), Down side 40° (typ.)
Designed viewing direction	<i>At DPSH: normal scan and DPSV: normal scan</i> • Viewing direction without image reversal: up side (12 o'clock) • Viewing direction with contrast peak: down side 5° to 10° (6 o'clock) • Viewing angle with optimum grayscale ($\gamma=2.2$): normal axis
Polarizer surface	Antiglare treatment
Polarizer pencil-hardness	3H (min.) [by JIS K5400]
Color gamut	<i>At LCD panel center</i> 50 % (typ.) [against NTSC color space]
Response time	5 ms (typ.)
Luminance	<i>At 5.0mAmps / lamp</i> 400 cd/m ² (typ.)
Signal system	6-bit digital signals for data of RGB colors, Dot clock (CLK), Data enable (DE), Horizontal synchronous signal (Hsync), Vertical synchronous signal (Vsync)
Power supply voltage	LCD panel signal processing board: 3.3V or 5.0V
Backlight	Edge light type: 2 cold cathode fluorescent lamps [Replaceable parts • Lamps for backlight unit: Type No. 55LHS11] [Recommended inverter (Option) • Inverter: Type No. 55PW131]
Power consumption	<i>At maximum luminance and checkered flag pattern</i> 4.1 W (typ.)

3. BLOCK DIAGRAM



Note1: GND and GNDB (Backlight inverter ground) should be connected together in customer equipment.

Note2: The metallic frame of lamp holder is used to a transmission line for VBLC.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	134.0 ± 0.5 (W) $\times$ 104.5 ± 0.5 (H) $\times$ 12.5 ± 0.5 (D) Note1	mm
Display area	111.4 ± 0.5 (W) $\times$ 83.5 ± 0.5 (H) Note1	mm
Weight	215 (typ.), 220 (max.)	g

Note1: See "7. OUTLINE DRAWINGS".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal board		VCC	-0.3 to +6.5	V	Ta = 25°C
	Lamp	High voltage side (Hot) Note1	VBLH	1,500	Vrms	
		Low voltage side (Cold) Note2	VBLC	42.4	Vrms	
Input voltage for signals	Display signals Note3		VD	-0.3 to VCC+0.3	V	
	Function signals Note4		VF	-0.3 to VCC+0.3	V	
Storage temperature			Tst	-30 to +80	°C	-
Operating temperature		Front surface	TopF	-10 to +70	°C	
		Rear surface	TopR	TBD	°C	
Relative humidity Note5			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40 < Ta ≤ 50°C
				≤ 70	%	50 < Ta ≤ 55°C
				≤ 60	%	55 < Ta ≤ 60°C
				≤ 50	%	60 < Ta ≤ 65°C
				≤ 42	%	65 < Ta ≤ 70°C
Absolute humidity Note5			AH	≤ 78 Note6	g/m³	Ta > 70°C

Note1: "VBLH" is the voltage value between low voltage terminal (Cold) and high voltage terminal (Hot).

Note2: "VBLC" is the voltage value between backlight inverter ground (GNDB) and low voltage terminal (Cold).

Note3: Display signals are CLK, Hsync, Vsync, DE and DATA (R0 to R5, G0 to G5, B0 to B5).

Note4: Function signals are DPSH, DPSV and PNS.

Note5: No condensation

Note6: Ta = 70°C, RH = 42%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 Driving for LCD panel signal processing board

(Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply voltage	VCC	3.0	3.3	3.6	V	for 3V system
		4.75	5.00	5.25	V	for 5V system
Power supply current	ICC	-	180 Note1	250	mA	VCC = 3.3V Note2
		-	120 Note1	165	mA	VCC = 5.0V Note2
Logic input voltage for display signals	Low	VDLL	0	-	0.3Vcc	CMOS level
	High	VDLH	0.7Vcc	-	Vcc	
Input voltage for DPSH or DPSV signals	Low	VFDL	0	-	0.3Vcc	
	High	VFDH	0.7Vcc	-	Vcc	
Input voltage for PNS signal	Low	VFPL	0	-	0.3Vcc	
	High	VFPH	0.7Vcc	-	Vcc	

Note1: Checkered flag pattern [by EIAJ ED-2522]

Note2: At QVGA display mode (PNS: Low)

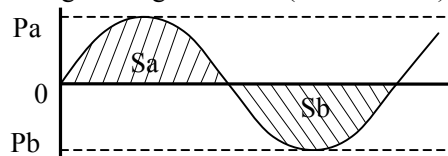
4.3.2 Working for backlight lamp

5

Parameter	Symbol	Ta	Min.	Typ.	Max.	Unit	Remarks
Starting voltage	VS	0°C	720	-	-	Vrms	Note1
		25°C	570	-	-	Vrms	
Power supply voltage	VBLH	25°C	-	350	-	Vrms	Note1, Note2
Power supply current	IBL	25°C	4.5	5.0	5.5	mArms	Note2
Oscillation frequency	FO	25°C	39	43	47	kHz	Note3

Note1: The power supply voltage cycle between lamps should be kept on a same phase. "VS" and "VBLH" are the voltage value between low voltage side (Cold) and high voltage side (Hot).

Note2: The asymmetric ratio of working waveform for lamps (Power supply voltage peak ratio, power supply current peak ratio and waveform space ratio) should be less than 5 % (See the following figure.). If the waveform is asymmetric, DC (Direct current) element apply into the lamp. In this case, a lamp lifetime may be shortened, because a distribution of a lamp enclosure substance inclines toward one side between low voltage terminal (Cold terminal) and high voltage terminal (Hot terminal).



$$\frac{|Pa - Pb|}{Pb} \times 100 \leq 5\%$$

$$\frac{|Sa - Sb|}{Sb} \times 100 \leq 5\%$$

Pa: Supply voltage/current peak for positive, Pb: Supply voltage/current peak for negative

Sa: Waveform space for positive part, Sb: Waveform space for negative part

Note3: In case "FO" is not the recommended value, beat noise may display on the screen, because of interference between "FO" and "1/th". Recommended value of "FO" is as following.

$$FO = \frac{1}{4} \times \frac{1}{th} \times (2n-1)$$

th: Horizontal synchronous cycle (See "4.9.7 Timing characteristics for QVGA display mode" or "4.9.8 Timing characteristics for VGA display mode".)

n: Natural number (1, 2, 3)

4.3.3 Power supply voltage ripple

This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Parameter	Power supply voltage	Ripple voltage (Measure at input terminal of power supply)	Note1 Unit
VCC	3.3 V	≤ 100	mVp-p
	5.0 V	≤ 100	mVp-p

Note1: The permissible ripple voltage includes spike noise.

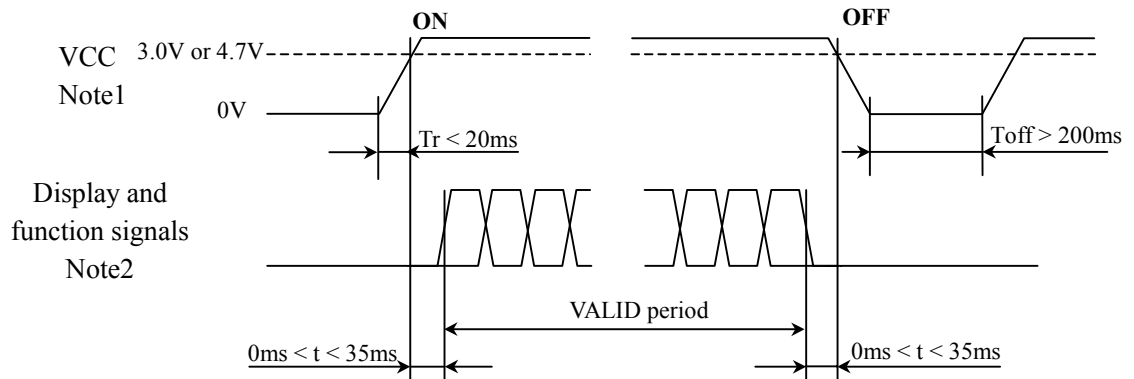
4.3.4 Fuses

Fusing line	Fuse		Rating	Unit	Remark
	Type	Supplier			
VCC	ICP-S1.8	ROHM Co., Ltd.	4.0	A	Current fusing Note1
			50	V	-

Note1: The power capacity should be more than the fusing current rating. If the power capacity is less than the criteria value, the fuse may not blow, and then nasty smell, smoking and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 Sequence for LCD panel signal processing board

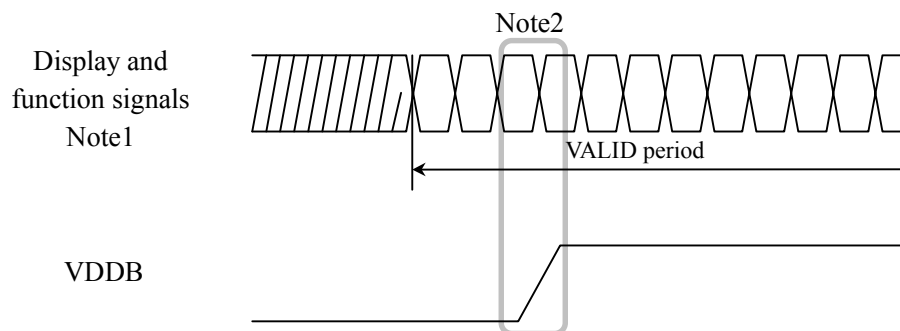


Note1: In terms of voltage variation (voltage drop) while VCC rising edge is below 3.0V in "VCC = 3.3V" or 4.7V in "VCC = 5.0V", a protection circuit may work, and then this product may not work.

Note2: Display (CLK, Hsync, Vsync, DE, R0 to R5, G0 to G5, B0 to B5) and function (DPSH, DPSV, PNS) signals must be Low or High-impedance, exclude the VALID period (See above sequence diagram), in order to avoid that internal circuits is damaged.

If some of display and function signals of this product are cut while this product is working, even if the signal input to it once again, it might not work normally. If customer stops the display and function signals, they should be cut VCC.

4.4.2 Sequence for backlight inverter (Option)



Note1: These are display and function signals for LCD panel signal processing board.

Note2: The backlight inverter voltage (VDDDB) should be inputted within the valid period of display and function signals, in order to avoid unstable data display.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

4.5.1 LCD panel signal processing board

5

CN1 socket (LCD module side): 08-6210-033-340-800 (Kyocera Elco Corp.)

Adaptable plug: TW-VF-33-0.035 TA-200-A4.0BB-P0.5-HBL8 (Fujikura Ltd.)

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	-
2	CLK	Dot clock	
3	Hsync	Horizontal synchronous	
4	Vsync	Vertical synchronous	
5	GND	Ground	
6	R0	Red data (LSB)	Least significant bit
7	R1	Red data	-
8	R2	Red data	
9	R3	Red data	
10	R4	Red data	
11	R5	Red data (MSB)	Most significant bit
12	GND	Ground	-
13	G0	Green data (LSB)	Least significant bit
14	G1	Green data	-
15	G2	Green data	
16	G3	Green data	
17	G4	Green data	
18	G5	Green data (MSB)	Most significant bit
19	GND	Ground	-
20	B0	Blue data (LSB)	Least significant bit
21	B1	Blue data	-
22	B2	Blue data	
23	B3	Blue data	
24	B4	Blue data	
25	B5	Blue data (MSB)	Most significant bit
26	GND	Ground	-
27	DE	Select of DE / Fixed mode	DE mode: Data enable signal, Fixed mode: Open
28	VCC	Power supply	-
29	VCC	Power supply	
30	DPSH	Select of scan direction (Horizontal)	Normal scan: Low or Open, Reverse scan: High Note1
31	DPSV	Select of scan direction (Vertical)	
32	PNS	Select of pixel number	QVGA mode: Low or Open, VGA mode: High Note1
33	GND	Ground	-

Note1: See "4.8 SCANNING DIRECTIONS".

CN1: Figure of socket

1 2 3 -----31 32 33

4.5.2 Backlight lamp

CN2 socket: BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)

Adaptable plug: SM03 (4.0) B-BHS-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Pink cable
2	NC	Non connection	-
3	VBLC	Low voltage (Cold)	Gray cable

CN2: Figure of socket

1	2	3
---	---	---

CN3 socket: BHR-03VS-1 (J.S.T Mfg. Co., Ltd.)

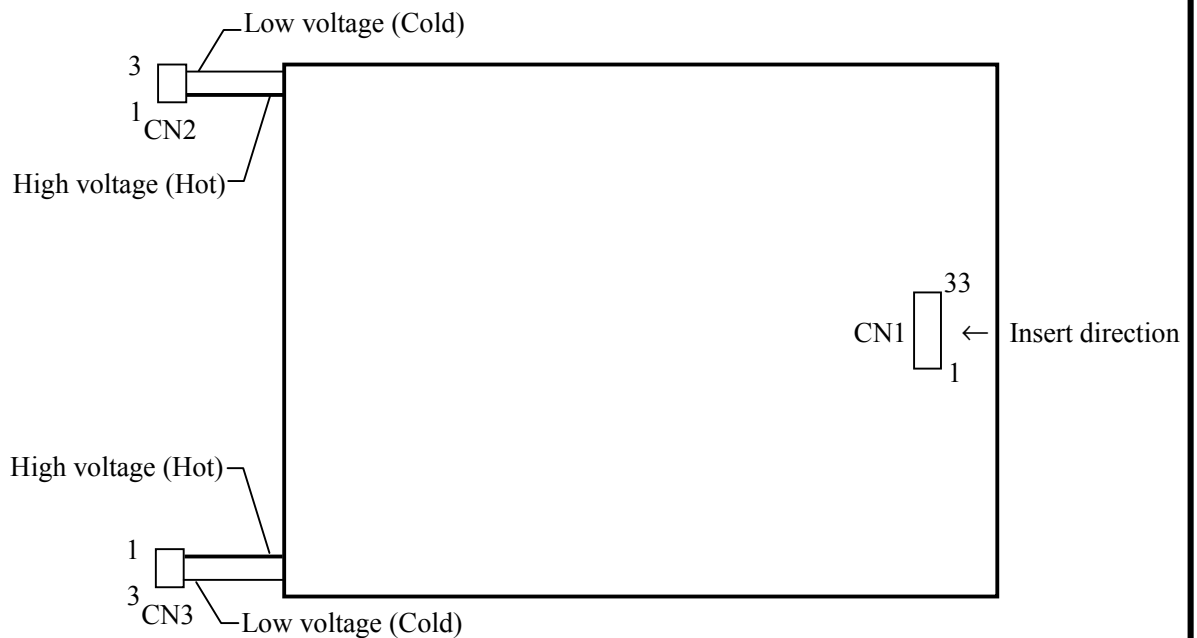
Adaptable plug: SM03 (4.0) B-BHS-TB (J.S.T Mfg. Co., Ltd.)

Pin No.	Symbol	Signal	Remarks
1	VBLH	High voltage (Hot)	Pink cable
2	NC	Non connection	-
3	VBLC	Low voltage (Cold)	Gray cable

CN3: Figure of socket

1	2	3
---	---	---

4.5.3 Positions of sockets



4.6 DISPLAY COLORS AND INPUT DATA SIGNALS

This product can display in equivalent to 262,144 colors in 64 scale. Also the relation between display colors and input data signals is as the following table.

Display colors		Data signal (0: Low level, 1: High level)																	
		R 5	R 4	R 3	R 2	R 1	R 0	G 5	G 4	G 3	G 2	G 1	G 0	B 5	B 4	B 3	B 2	B 1	B 0
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑				:					:						:			
	↓				:					:						:			
	bright	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Green scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	↑				:					:						:			
	↓				:					:						:			
	bright	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
Blue scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	↑				:					:						:			
	↓				:					:						:			
	bright	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

4.7 DISPLAY POSITIONS

The following table is the coordinates per pixel (See figure of "4.8 SCANNING DIRECTIONS").

C(0, 0)	C(1, 0)	...	C(X, 0)	...	C(318, 0)	C(319, 0)
C(0, 1)	C(1, 1)	...	C(X, 1)	...	C(318, 1)	C(319, 1)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0, Y)	C(1, Y)	...	C(X, Y)	...	C(318, Y)	C(319, Y)
⋮	⋮	⋮	⋮	⋮	⋮	⋮
C(0,238)	C(1,238)	...	C(X,238)	...	C(318,238)	C(319,238)
C(0,239)	C(1,239)	...	C(X,239)	...	C(318,239)	C(319,239)

4.8 SCANNING DIRECTIONS

4.8.1 QVGA display mode

The following figures are seen from a front view. Also the arrow shows the direction of scan.

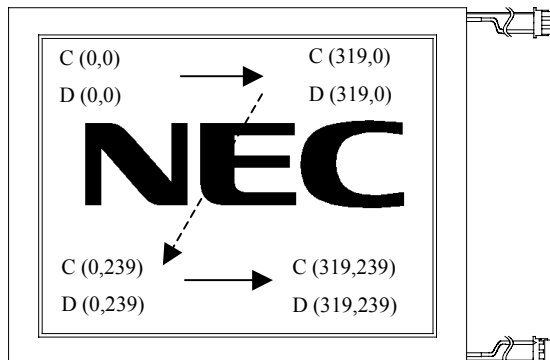


Figure 1. DPSH: Normal scan, DPSV: Normal scan

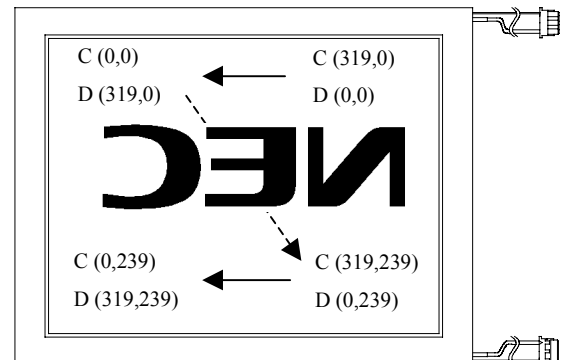


Figure 2. DPSH: Reverse scan, DPSV: Normal scan

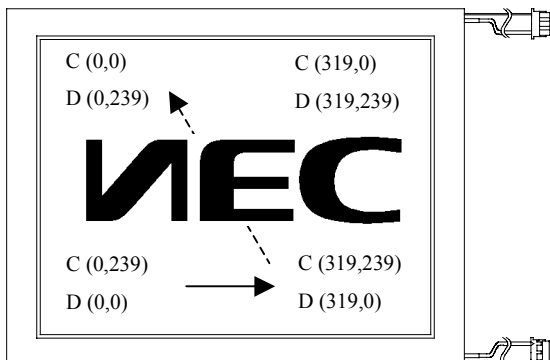


Figure 3. DPSH: Normal scan, DPSV: Reverse scan

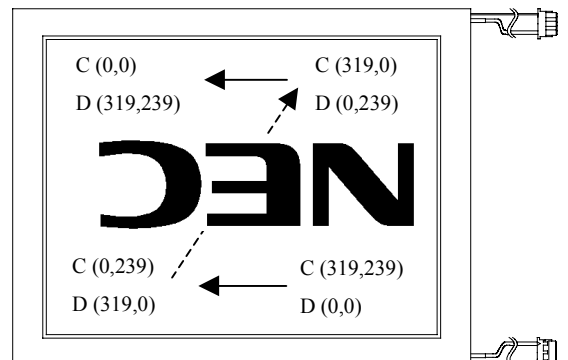


Figure 4. DPSH: Reverse scan, DPSV: Reverse scan

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "4.7 DISPLAY POSITIONS".)

D (X, Y): The data number of QVGA input signal for LCD panel signal processing board

Note2: Normal scan: Low or Open, Reverse scan: High

4.8.2 VGA display mode

The following figures are seen from a front view. Also the arrow shows the direction of scan, and a dotted line is a virtual display domain. In this display mode, only quarter domains of virtual display are displayed on the screen.

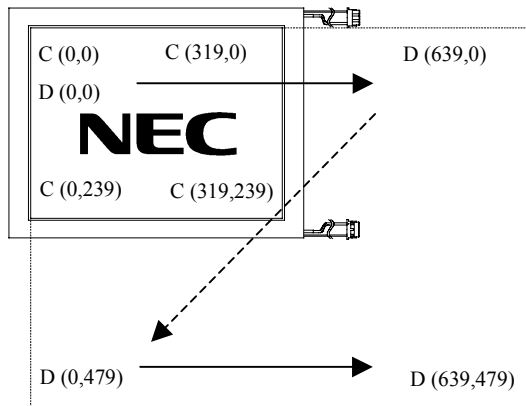


Figure 1. DPSH: Normal scan, DPSV: Normal scan

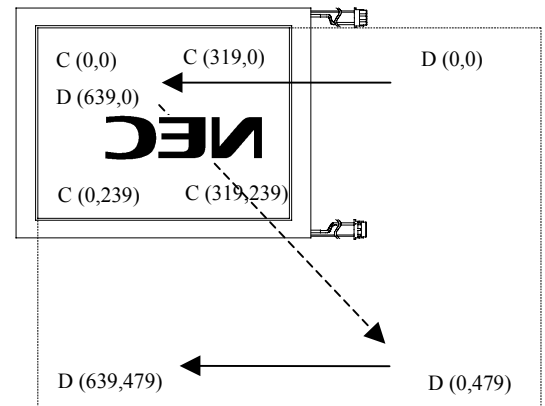


Figure 2. DPSH: Reverse scan, DPSV: Normal scan

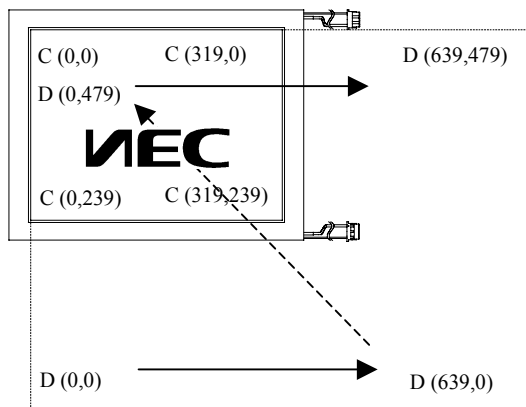


Figure 3. DPSH: Normal scan, DPSV: Reverse scan

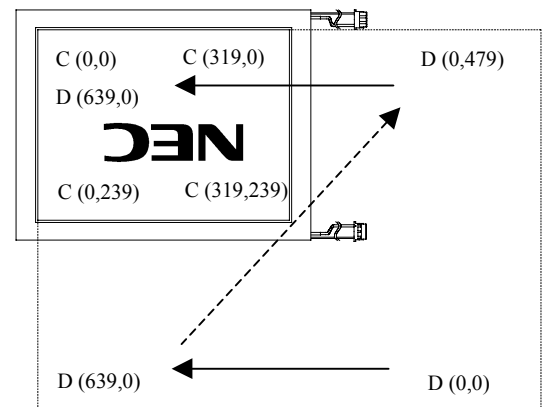


Figure 4. DPSH: Reverse scan, DPSV: Reverse scan

Note1: Meaning of C (X, Y) and D (X, Y)

C (X, Y): The coordinates of the display position (See "4.7 DISPLAY POSITIONS".)

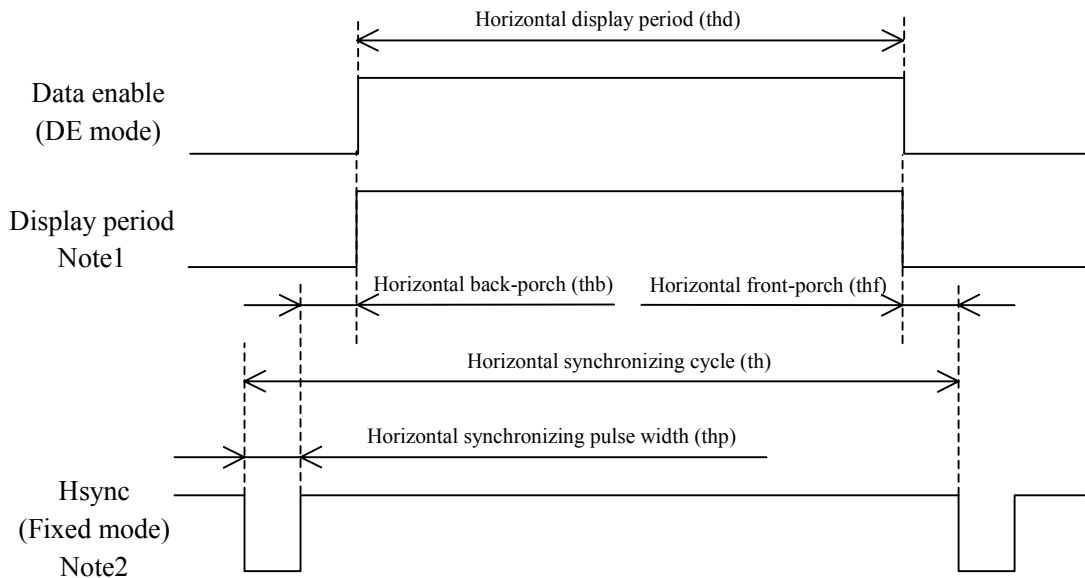
D (X, Y): The data number of VGA input signal for LCD panel signal processing board

Note2: Normal scan: Low or Open, Reverse scan: High

4.9 INPUT SIGNAL TIMINGS FOR LCD PANEL SIGNAL PROCESSING BOARD

4.9.1 Outline of QVGA input signal timings

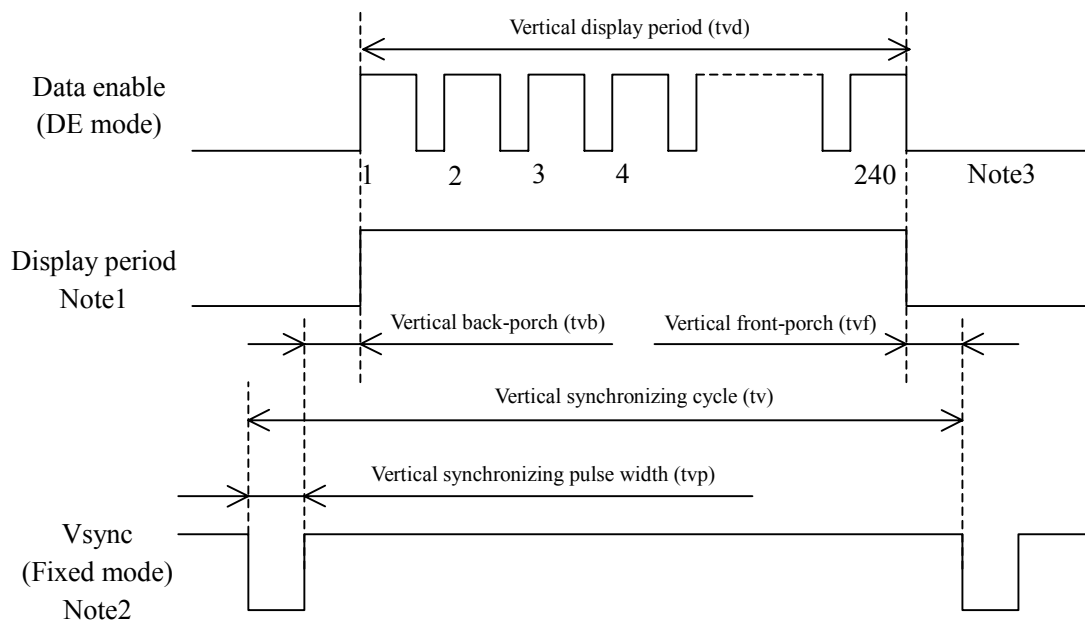
• Horizontal signal



Note1: This diagram indicates virtual signal for set up to timing.

Note2: Fixed mode cannot be used while working of DE mode.

• Vertical signal



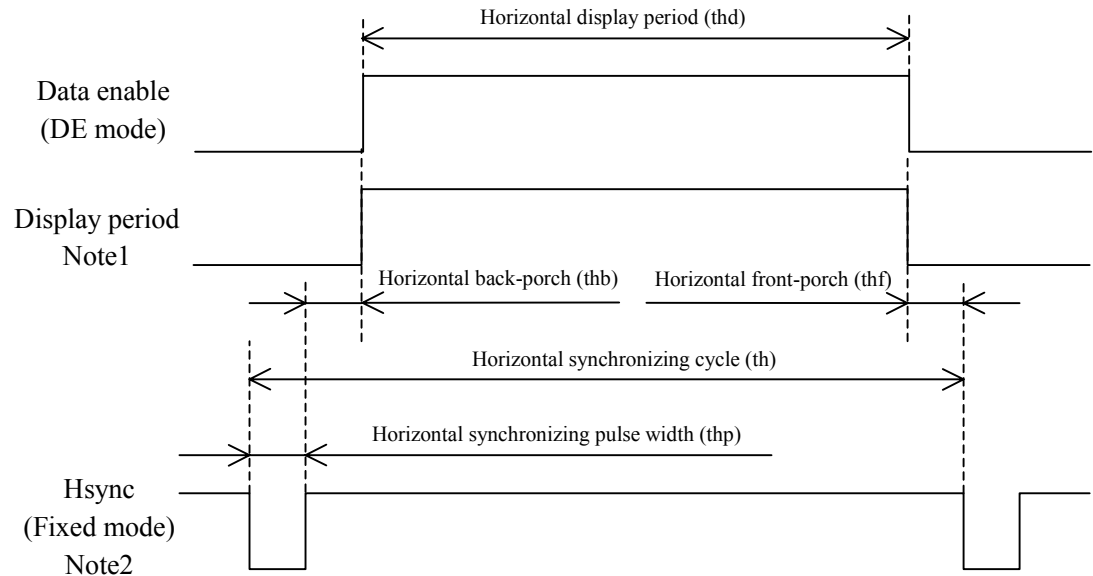
Note1: This diagram indicates virtual signal for set up to timing.

Note2: Fixed mode cannot be used while working of DE mode.

Note3: See "4.9.3 Detailed QVGA input signal timing chart for DE mode" and "4.9.4 Detailed QVGA input signal timing chart for fixed mode" for numeration of pulse.

4.9.2 Outline of VGA input signal timings

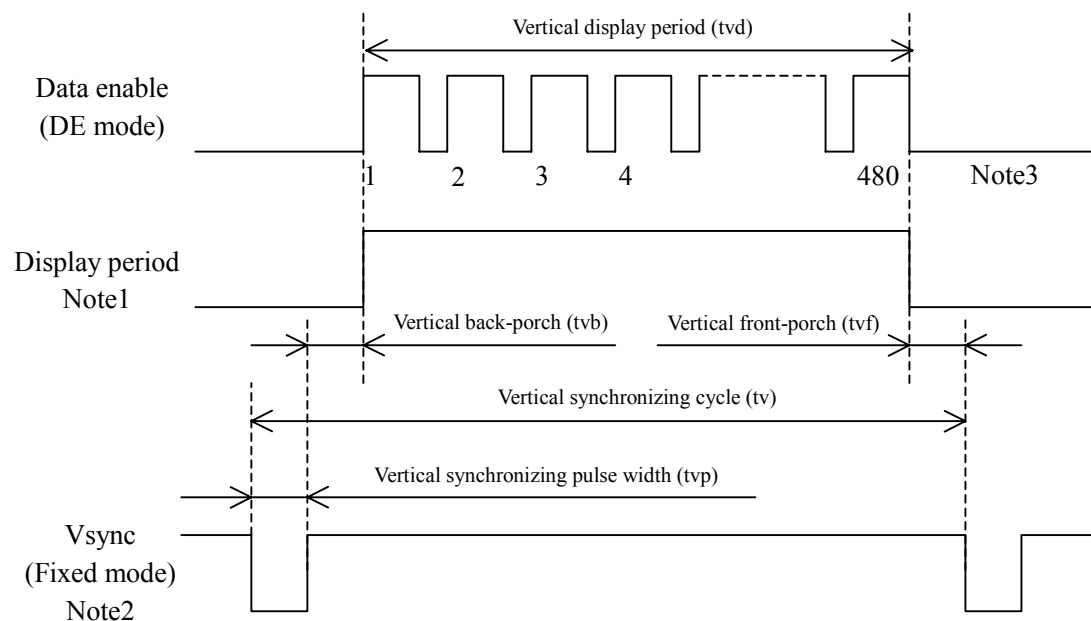
- Horizontal signal



Note1: This diagram indicates virtual signal for set up to timing.

Note2: Fixed mode cannot be used while working of DE mode.

- Vertical signal



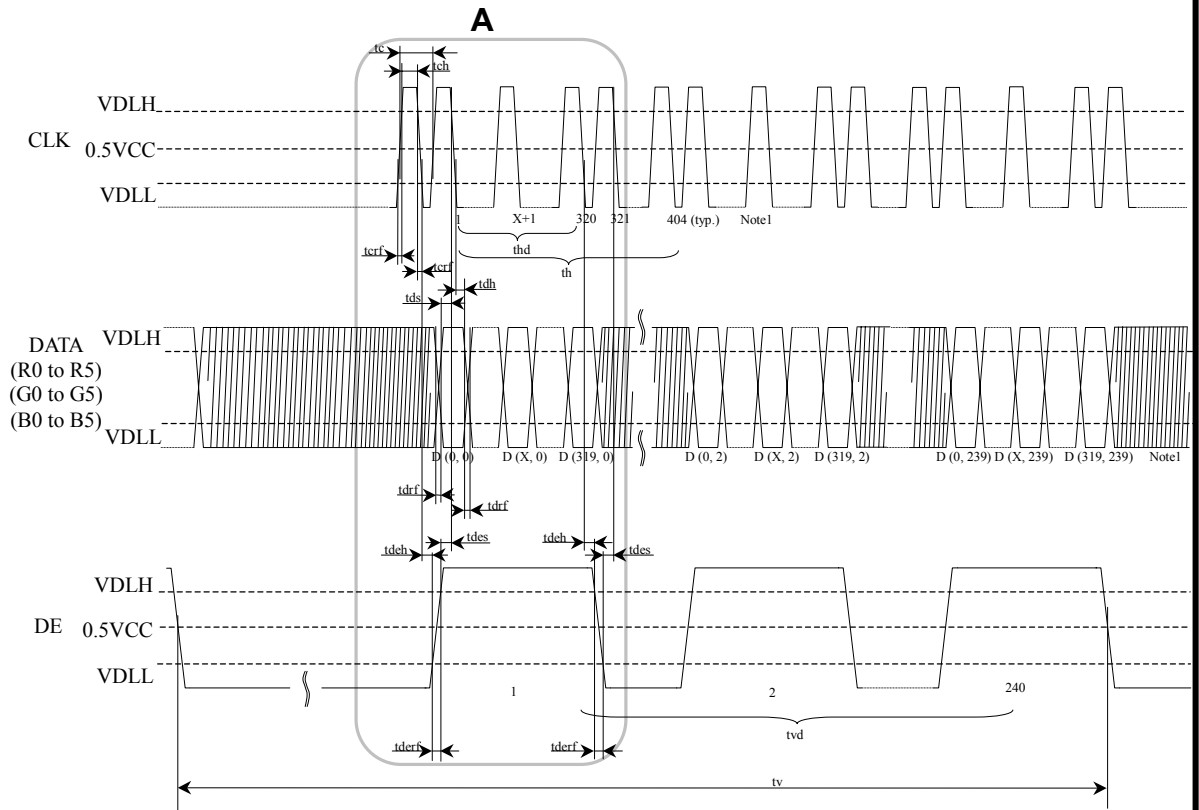
Note1: This diagram indicates virtual signal for set up to timing.

Note2: Fixed mode cannot be used while working of DE mode.

Note3: See "4.9.5 Detailed VGA input signal timing chart for DE mode" and "4.9.6 Detailed VGA input signal timing chart for fixed mode" for numeration of pulse.

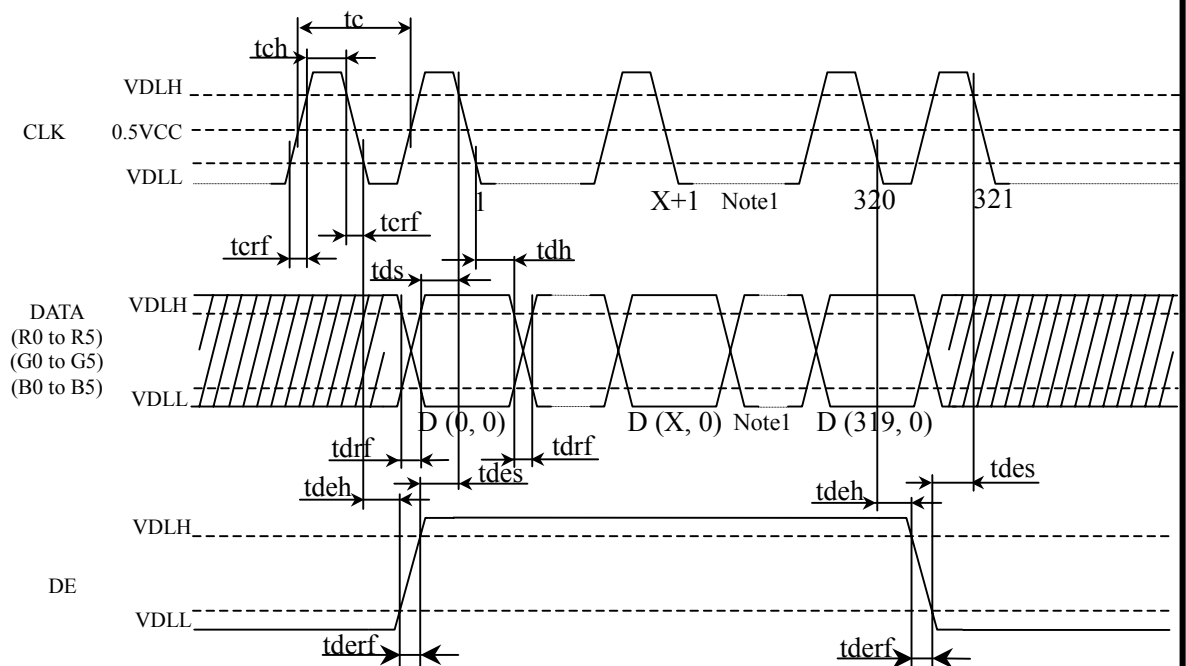
4.9.3 Detailed QVGA input signal timing chart for DE mode

- Outline chart



Note1: X is data number from 1 to 318. See "4.8.1 QVGA display mode".

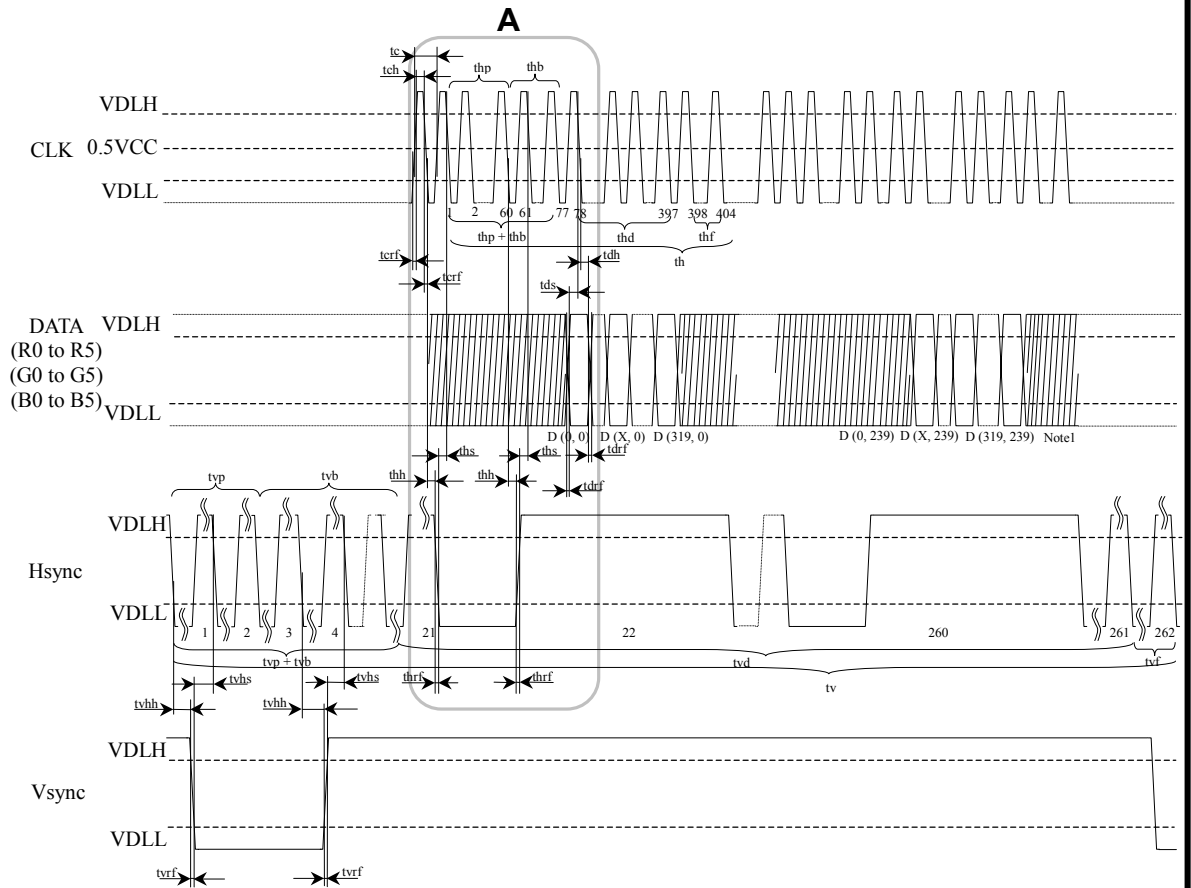
- Detail of **A** part



Note1: X is data number from 1 to 318. See "4.8.1 QVGA display mode".

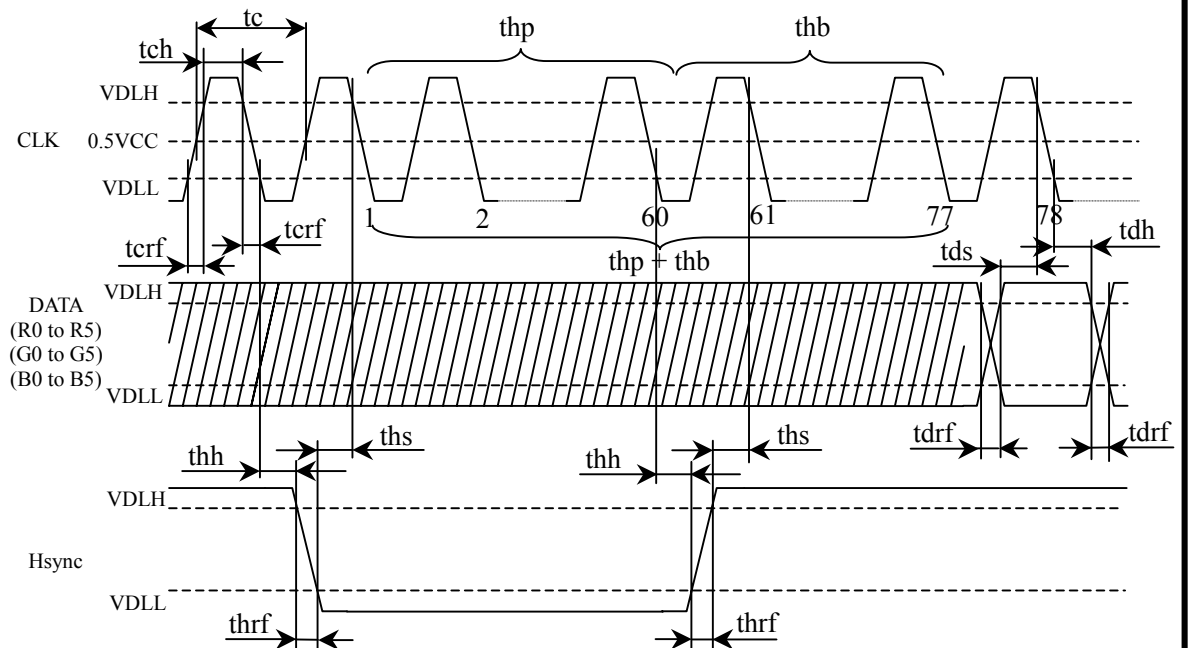
4.9.4 Detailed QVGA input signal timing chart for fixed mode

- Outline chart

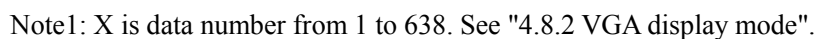


Note1: X is data number from 1 to 318. See "4.8.1 QVGA display mode".

- Detail of **A** part



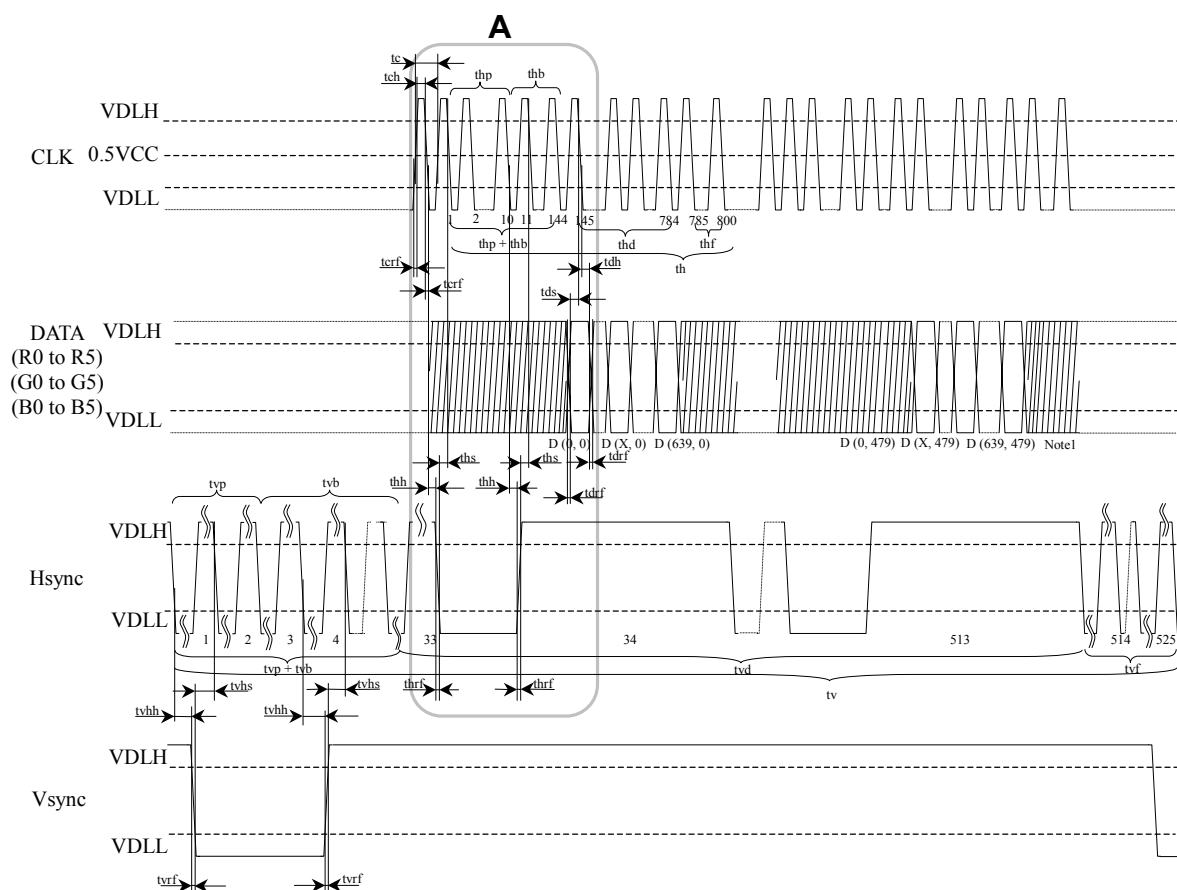
- Outline chart



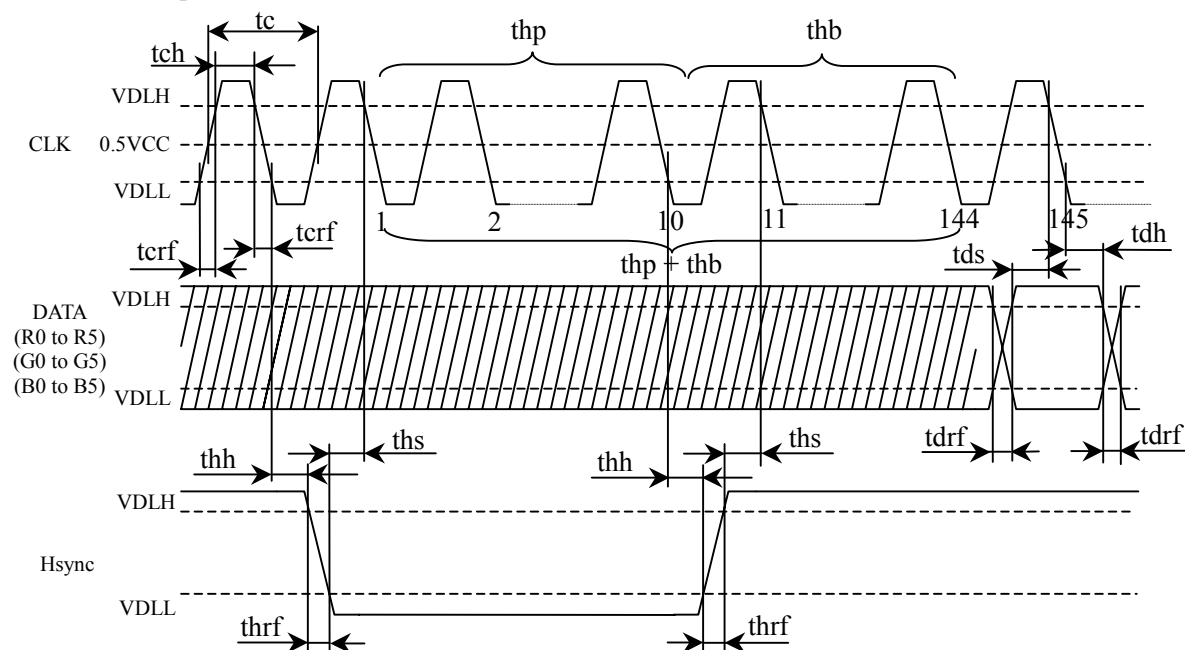
The timing diagram illustrates the relationship between the clock (CLK), data bus (DATA), and data enable (DE) signals. The clock signal (CLK) is shown as a trapezoidal wave with levels VDLH, 0.5VCC, and VDLL. The data bus (DATA) is divided into two sections: (R0 to R5) (G0 to G5) and (B0 to B5). The data enable signal (DE) is also shown as a trapezoidal wave with levels VDLH and VDLL. The diagram includes several timing parameters: t_{ch} (clock high time), t_c (clock period), t_{crf} (clock rise/fall time), t_{ds} (data setup time), t_{dh} (data hold time), t_{drf} (data rise/fall time), t_{deh} (data enable high time), t_{des} (data enable setup time), and t_{derf} (data enable rise/fall time). The data bus is shown with specific data values: D(0, 0), D(X, 0) Note1, and D(639, 0). The data bus is also shown with a shaded region indicating a high-impedance state.

NEC Corporation

- Outline chart



Detail of **A** part



4.9.7 Timing characteristics for QVGA display mode

- Common to DE mode and fixed mode

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	tcf	5.0	6.4	7.0	MHz	157.5 ns (typ.) Note1
	Duty	tcd	0.4	-	0.6	-	Note1
	Rise time, Fall time	tcrf	-	-	10	ns	-
DATA	CLK-DATA	Setup time	tds	5	-	-	
		Hold time	tdh	10	-	-	
	Rise time, Fall time	tdrf	-	-	10	ns	

Note1: Definition of parameters is as follows.

$$tcf = 1/tc, tcd = tch/tc = tch \times tcd$$

- DE mode

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
DE	Horizontal	Cycle	th	331	404	-	Note1
		Display period	thd	320		CLK	
	Vertical (One frame)	Cycle	tv	224	262	-	
		Display period	tvd	240		H	
	CLK-DE	Setup time	tdes	5	-	-	-
		Hold time	tdeh	10	-	-	
	Rise time, Fall time		tderf	-	-	10	

Note1: Definition of parameters is as follows.

$$tc = 1CLK, th = 1H$$

- Fixed mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
Hsync	Cycle		th	57.7	63.5	80.8	μ s	15.7 kHz (typ.)
				404			CLK	Note1
	Display period		thd	320			CLK	
	Front-porch		thf	7			CLK	
	Pulse width		thp	3	-	76	CLK	
	Back-porch		thb	1	-	74	CLK	
	Total of pulse width and back-porch		thp + thb	77			CLK	Note1, Note2
	CLK- Hsync	Setup time	ths	5	-	-	ns	-
		Hold time	thh	10	-	-	ns	
Rise time, Fall time		thrf	-	-	10	ns		
Vsync	Cycle		tv	15.1	16.6	21.2	ms	60.1 Hz (typ.)
				262			H	Note1
	Display period		tvd	240			H	
	Front-porch		tvf	1			H	
	Pulse width		tvp	2	-	20	H	
	Back-porch		tvb	1	-	19	H	
	Total of pulse width and back-porch		tvp + tvb	21			H	Note1, Note2
	Vsync-Hsync	Setup time	tvhs	1	-	-	CLK	Note1
		Hold time	tvhh	10	-	-	ns	
	Rise time, Fall time		tvrf	-	-	10	ns	-

Note1: Definition of parameters is as follows.

$$tc = 1CLK, th = 1H$$

Note2: Keep $tvp + tvb$ and $thp + thb$ within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

4.9.8 Timing characteristics for VGA display mode

- Common to DE mode and fixed mode

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK	Frequency	tcf	-	25.2	-	MHz	39.7 ns (typ.) Note1
	Duty	tcd	-	0.5	-	-	Note1
	Rise time, Fall time	tcrf	-	-	-	ns	-
DATA	CLK-DATA	Setup time	-	-	-	ns	
		Hold time	-	-	-	ns	
	Rise time, Fall time	tdrf	-	-	-	ns	

Note1: Definition of parameters is as follows.

$$tcf = 1/tc, tcd = tch/tc = tch \times tcd$$

- DE mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
DE	Horizontal	Cycle	th	-	800	-	CLK	Note1
		Display period	thd	640			CLK	
	Vertical (One frame)	Cycle	tv	-	525	-	H	
		Display period	tvd	480			H	
	CLK-DE	Setup time	tdes	-	-	-	ns	-
		Hold time	tdeh	-	-	-	ns	
	Rise time, Fall time		tderf	-	-	-	ns	

Note1: Definition of parameters is as follows.

$$tc = 1CLK, th = 1H$$

- Fixed mode

Parameter			Symbol	Min.	Typ.	Max.	Unit	Remarks
Hsync	Cycle		th	-	31.8	-	μ s	31.4 kHz (typ.)
				800			CLK	Note1
	Display period		thd	640			CLK	
	Front-porch		thf	16			CLK	
	Pulse width		thp	-	-	-	CLK	
	Back-porch		thb	-	-	-	CLK	
	Total of pulse width and back-porch		thp + thb	144			CLK	Note1, Note2
	CLK- Hsync	Setup time	ths	-	-	-	ns	-
		Hold time	thh	-	-	-	ns	
Rise time, Fall time			thrf	-	-	-	ns	
Vsync	Cycle		tv	-	16.7	-	ms	59.9 Hz (typ.)
				525			H	Note1
	Display period		tvd	480			H	
	Front-porch		tvf	12			H	
	Pulse width		tvp	-	-	-	H	
	Back-porch		tvb	-	-	-	H	
	Total of pulse width and back-porch		tvp + tvb	33			H	Note1, Note2
	Vsync-Hsync	Setup time	tvhs	-	-	-	CLK	Note1
		Hold time	tvhh	-	-	-	ns	-
Rise time, Fall time			tvrf	-	-	-	ns	

Note1: Definition of parameters is as follows.

$$tc = 1CLK, th = 1H$$

Note2: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down.

4.10 OPTICS

4.10.1 Optical characteristics

5

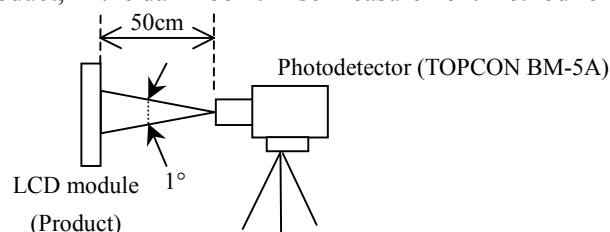
The following characteristics are only applied to QVGA display mode.

Parameter	Note1	Condition	Symbol	Min.	Typ.	Max.	Unit	Remarks
Contrast ratio		White/Black at center $\theta_R = 0^\circ, \theta_L = 0^\circ, \theta_U = 0^\circ, \theta_D = 0^\circ$	CR	320	400	-	-	Note2
Luminance		White at center $\theta_R = 0^\circ, \theta_L = 0^\circ, \theta_U = 0^\circ, \theta_D = 0^\circ$	L	320	400	-	cd/m ²	-
Luminance uniformity		-	LU	-	1.25	1.35	-	Note3
Chromaticity	White	x coordinate	Wx	-	0.310	-	-	Note4
		y coordinate	Wy	-	0.330	-	-	
	Red	x coordinate	Rx	-	0.600	-	-	
		y coordinate	Ry	-	0.350	-	-	
	Green	x coordinate	Gx	-	0.320	-	-	
		y coordinate	Gy	-	0.560	-	-	
	Blue	x coordinate	Bx	-	0.150	-	-	
		y coordinate	By	-	0.130	-	-	
Color gamut		$\theta_R = 0^\circ, \theta_L = 0^\circ, \theta_U = 0^\circ, \theta_D = 0^\circ$ at center, against NTSC color space	C	-	50	-	%	
Response time		White to black	Ton	-	5	15	ms	Note5
		Black to white	Toff	-	25	50	ms	Note6
Viewing angle	Right	$\theta_U = 0^\circ, \theta_D = 0^\circ, CR = 10$	θ_R	-	65	-	°	Note7
	Left	$\theta_U = 0^\circ, \theta_D = 0^\circ, CR = 10$	θ_L	-	65	-	°	
	Up	$\theta_R = 0^\circ, \theta_L = 0^\circ, CR = 10$	θ_U	-	40	-	°	
	Down	$\theta_R = 0^\circ, \theta_L = 0^\circ, CR = 10$	θ_D	-	65	-	°	

Note1: Measurement conditions are as follows.

Ta = 25°C, VCC = 3.3V, IBL = 5.0mAmps/lamp, DPSH: Low, DPSV: Low, PNS: Low

Optical characteristics are measured at luminance saturation after 20minutes from working the product, in the dark room. Also measurement method for luminance is as follows.



Note2: See "4.10.2 Definition of contrast ratio".

Note3: See "4.10.3 Definition of luminance uniformity".

Note4: These coordinates are found on CIE 1931 chromaticity diagram.

Note5: Product surface temperature: TopF = 32.5°C

Note6: See "4.10.4 Definition of response times".

Note7: See "4.10.5 Definition of viewing angles".

4.10.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

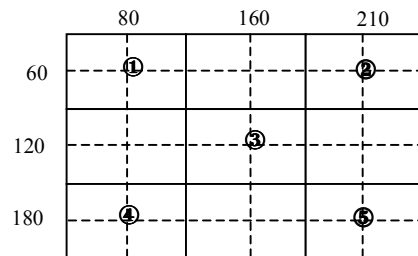
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

4.10.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

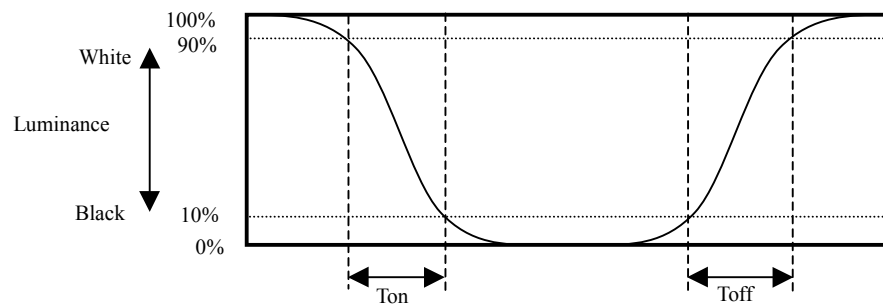
$$\text{Luminance uniformity (LU)} = \frac{\text{Maximum luminance from ① to ⑤}}{\text{Minimum luminance from ① to ⑤}}$$

The luminance is measured at near the 5 points shown below.

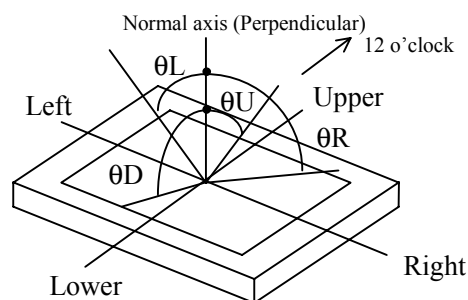


4.10.4 Definition of response times

Response time is measured, the luminance changes from "white" to "black", or "black" to "white" on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 90% down to 10%. Also Toff is the time it takes the luminance change from 10% up to 90% (See the following diagram.).



4.10.5 Definition of viewing angles



5. RELIABILITY TESTS

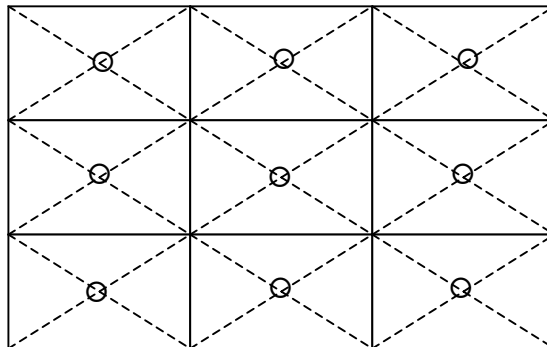
5

The result for reliability tests is only applied to QVGA display mode.

Test item	Condition	Judgement
High temperature and humidity (Operation)	① $55 \pm 2^{\circ}\text{C}$, RH = 85%, 240hours ② Display data is black.	No display malfunctions Note1
High temperature (Operation)	① $70 \pm 2^{\circ}\text{C}$, 240hours ② Display data is black.	
Heat cycle (Operation)	① $-10 \pm 3^{\circ}\text{C}$...1hour $70 \pm 3^{\circ}\text{C}$...1hour ② 50cycles, 4hours/cycle ③ Display data is black.	
Thermal shock (Non operation)	① $-30 \pm 3^{\circ}\text{C}$...30minutes $80 \pm 3^{\circ}\text{C}$...30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
ESD (Operation)	① 150pF, 150Ω, $\pm 10\text{kV}$ ② 9 places on a panel surface Note2 ③ 10 times each places at 1 sec interval	
Dust (Operation)	① Sample dust: No. 15 (by JIS-Z8901) ② 15 seconds stir ③ 8 times repeat at 1 hour interval	
Vibration (Non operation)	① 5 to 200Hz, 29.4m/s^2 ② 10 minute/cycle ③ X, Y direction...2hours ④ Z direction...4hours	No display malfunctions Note1 No physical damages
Mechanical shock (Non operation)	① 980m/s^2 , 11ms ② $\pm X$, $\pm Y$, $\pm Z$ direction ③ 3 times each directions	

Note1: Display functions are checked under the same conditions as product inspection.

Note2: See the following figure for discharge points.



6. PRECAUTIONS

6.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "6.2 CAUTIONS", after understanding this contents!**



This sign has the meaning that customer will be injured by himself, if customer has wrong operations.

6.2 CAUTIONS



- * Pay attention to burn injury for the working backlight! It may be over 35°C from ambient temperature.**
- * Do not shock and press the LCD panel and the backlight! Danger of breaking, because they are made of glass. (Shock: To be not greater 980m/s² and to be not greater 11ms, Pressure: To be not greater 19.6N)**

6.3 ATTENTIONS

6.3.1 Handling of the product

- ① Take hold of both ends without touch the circuit board when customer pulls out products (LCD modules) from inner packing box. If customer touches it, products may be broken down or out of adjustment, because of stress to mounting parts.
- ② Do not hook cables nor pull connection cables such as flexible cable and so on, for fear of damage.
- ③ If customer puts down the product temporarily, the product puts on flat subsoil as a display side turns down.
- ④ Take the measures of electrostatic discharge such as earth band, ionic shower and so on, when customer deals with the product, because products may be damaged by electrostatic.
- ⑤ The torque for mounting screws must never exceed 0.29N·m. Higher torque values might result in distortion of the bezel.
- ⑥ Do not press or rub on the sensitive display surface. If customer clean on the panel surface, NEC Corporation recommends using the cloth with ethanolic liquid such as screen cleaner for LCD.
- ⑦ Do not push-pull the interface connectors while the product is working, because wrong power sequence may break down the product.

6.3.2 Environment

- ① Do not operate in dewdrop atmosphere and corrosive gases.
- ② Do not operate or store in high temperature or high humidity atmosphere. Keep the product in antistatic pouch in room temperature, because of avoidance for dusts and sunlight, if customer stores the product.
- ③ Do not operate in high magnetic field. Circuit boards may be broken down by it.
- ④ Use an original protection sheet on the product surface (polarizer). Adhesive type protection sheet should be avoided, because it may change color or properties of the polarizer.

6.3.3 Characteristics

The following items are neither defects nor failures.

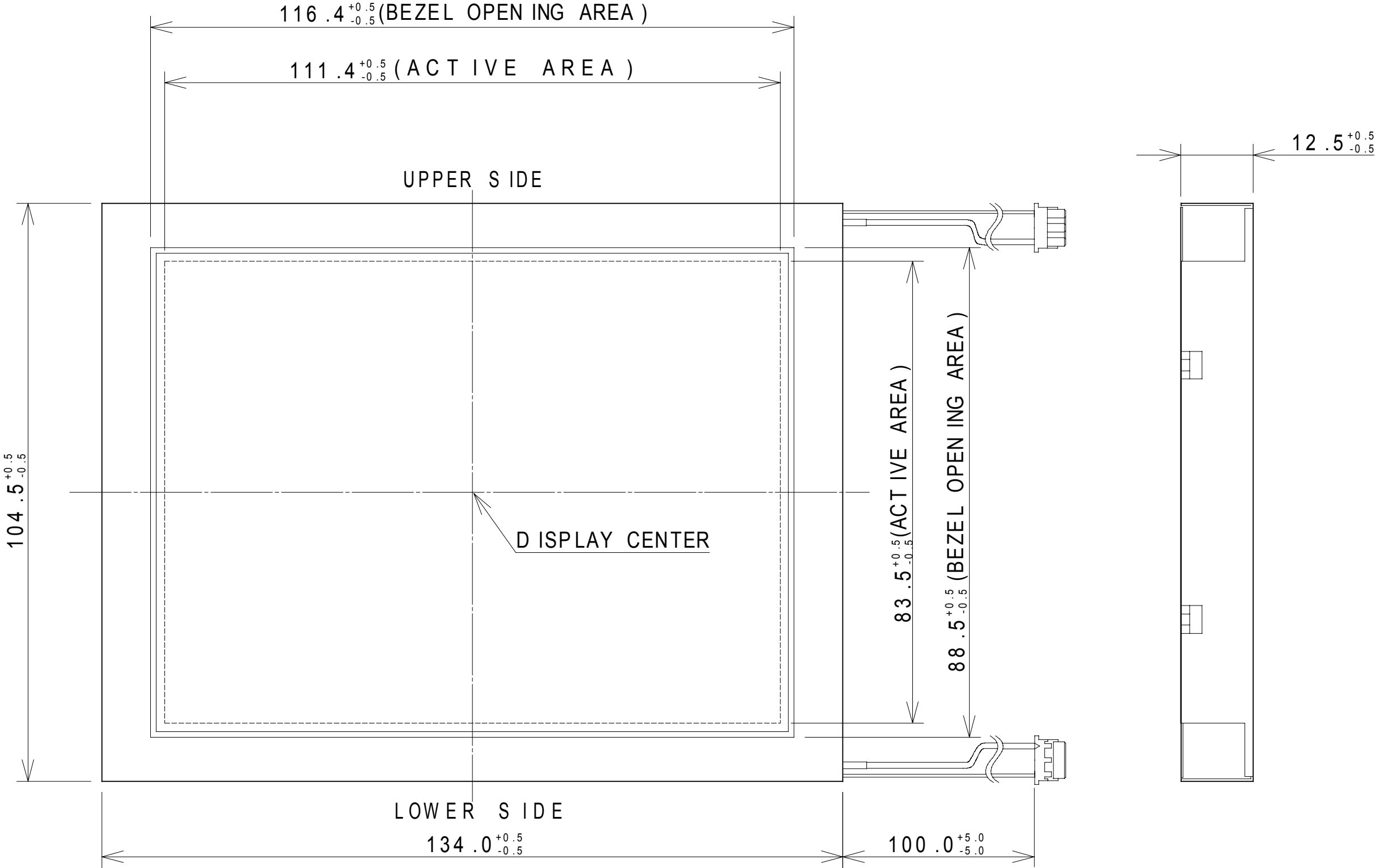
- ① Response time, luminance and color may be changed by ambient temperature.
- ② The LCD may be seemed luminance non-uniformity, flicker, vertical seam or small spot by display patterns.
- ③ Optical characteristics (e.g. luminance, display uniformity, etc.) gradually is going to change depending on operating time, and especially low temperature, because the LCD has cold cathode fluorescent lamps.
- ④ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
- ⑤ The display color may be changed by viewing angle because of the use of condenser sheet in the backlight unit.
- ⑥ Optical characteristics may be changed by input signal timings.
- ⑦ The interference noise of input signal frequency for this product's signal processing board and luminance control frequency of customer's backlight inverter may appear on a display. Set up luminance control frequency of backlight inverter so that the interference noise does not appear.

6.3.4 Other

- ① All GND, backlight inverter ground (GNDB), VCC and backlight inverter power supply voltage (VDDB) terminals should be used without a non-connected line.
- ② Do not disassemble a product or adjust volume without permission of NEC Corporation.
- ③ See "REPLACEMENT MANUAL FOR LAMPHOLDER", if customer would like to replace backlight lamps.
- ④ Pay attention not to insert waste materials inside of products, if customer uses screwdrivers.
- ⑤ Pack the product with original shipping package, because of avoidance of some damages during transportation, when customer returns it to NEC Corporation for repair and so on.

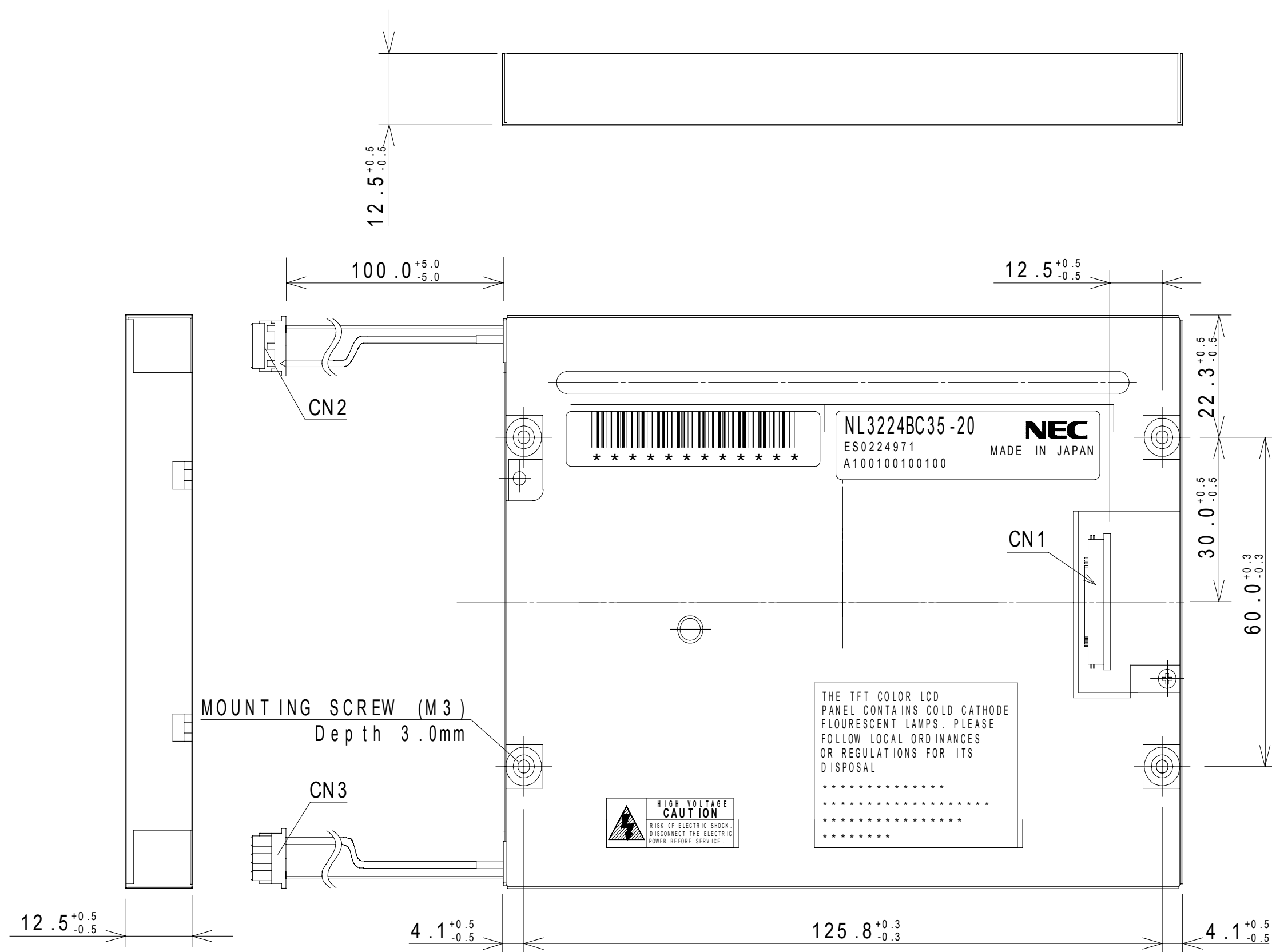
7. OUTLINE DRAWINGS

7.1 FRONT VIEW



Unit: mm

7.2 REAR VIEW



Unit: mm

REVISION HISTORY

The inside of latest specifications is revised to the clerical error, undecided mater (TBD, etc.) and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Document number	Prepared date	Revision contents and writer
1st edition	DOD - N - 0155	May. 11, 2001	Revision contents New issue Writer Approved by H. MORIYAMA Checked by Prepared by T. KUSANAGI
2nd edition	DOD - M - 0577	Aug. 27, 2001	Revision contents • Change part (Before-1st edition → After-2nd edition) (1) page 5/24 5. OUTLINE OF CHARACTERISTICS (at room temperature) Weight TBD g (Typ.) Response time TBD ms (Typ., "white" to "black") Backlight Edge light type: a cold cathode fluorescent lamp in each holder [Replaceable parts] • Lamp holders (Parts No. TBD) Power consumption 4.35W (Typ. at 3.3V, IL=5.0mA_{rms}) → page 6/35 2. GENERAL SPECIFICATIONS Weight 215 g (typ.) Response time 3 ms (typ.) Backlight Edge light type: 2 cold cathode fluorescent lamps Replaceable parts • Lamps for backlight unit: Type No. 55LHS11 Recommended inverter (Option) • Inverter: Type No. 55PW131 Power consumption At maximum luminance and checkered flag pattern 4.1W (typ.) (2) page 7/24 7.1 GENERAL SPECIFICATIONS Weight TBD (MAX.) g → page 8/35 4.1 MECHANICAL SPECIFICATIONS Weight 215 (typ.), 220 (max.) g

REVISION HISTORY

Edition	Document number	Prepared date	Revision contents and writer																																																																							
2nd edition	DOD - M - 0577	Aug. 27, 2001	(3) page 7/24 7.2 ABSOLUTE MAXIMUM RATINGS																																																																							
			<table><tr><th>Parameters</th><th>Symbols</th><th>Ratings</th><th>Units</th><th>Remarks</th></tr><tr><td>Supply voltage</td><td>VCC</td><td>-0.3 to +6.5</td><td>V</td><td rowspan="2">Ta=25℃</td></tr><tr><td>Logic Input voltage</td><td>VI</td><td>-0.3 to VCC+0.3</td><td>V</td></tr><tr><td>Lamp voltage</td><td>VL</td><td>TBD</td><td>Vrms</td><td>—</td></tr><tr><td>Storage temp.</td><td>Tst</td><td>-30 to +80</td><td>℃</td><td>—</td></tr><tr><td>Operation temp.</td><td>Top</td><td>-10 to +70</td><td>℃</td><td>module surface Note 1</td></tr><tr><td rowspan="2">Relative humidity Note 2</td><td rowspan="2"></td><td>≤95</td><td>%</td><td>Ta ≤ 40 ℃</td></tr><tr><td>≤85</td><td>%</td><td>40< Ta ≤ 50 ℃</td></tr><tr><td>Absolute humidity Note 2</td><td></td><td>Absolute humidity shall not exceed Ta=50℃, RH= 85% level</td><td>g/m³</td><td>Ta > 50 ℃</td></tr></table>	Parameters	Symbols	Ratings	Units	Remarks	Supply voltage	VCC	-0.3 to +6.5	V	Ta=25℃	Logic Input voltage	VI	-0.3 to VCC+0.3	V	Lamp voltage	VL	TBD	Vrms	—	Storage temp.	Tst	-30 to +80	℃	—	Operation temp.	Top	-10 to +70	℃	module surface Note 1	Relative humidity Note 2		≤95	%	Ta ≤ 40 ℃	≤85	%	40< Ta ≤ 50 ℃	Absolute humidity Note 2		Absolute humidity shall not exceed Ta=50℃, RH= 85% level	g/m³	Ta > 50 ℃																													
			Parameters	Symbols	Ratings	Units	Remarks																																																																			
			Supply voltage	VCC	-0.3 to +6.5	V	Ta=25℃																																																																			
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			Lamp voltage	VL	TBD	Vrms	—																																																																			
			Storage temp.	Tst	-30 to +80	℃	—																																																																			
			Operation temp.	Top	-10 to +70	℃	module surface Note 1																																																																			
			Relative humidity Note 2		≤95	%	Ta ≤ 40 ℃																																																																			
					≤85	%	40< Ta ≤ 50 ℃																																																																			
Absolute humidity Note 2		Absolute humidity shall not exceed Ta=50℃, RH= 85% level	g/m³	Ta > 50 ℃																																																																						
→ page 8/35 4.2 ABSOLUTE MAXIMUM RATINGS																																																																										
<table><tr><th colspan="3">Parameter</th><th>Symbol</th><th>Rating</th><th>Unit</th><th>Remarks</th></tr><tr><td>Supply voltage</td><td colspan="2">LCD panel signal board and driver</td><td>VCC</td><td>-0.3 to +6.5</td><td>V</td><td rowspan="5">Ta = 25℃</td></tr><tr><td rowspan="4">Input voltage</td><td rowspan="2">LCD panel signal board</td><td>Display signals Note1</td><td>ViD</td><td>-0.3 to VCC+0.3</td><td>V</td></tr><tr><td>Function signals Note2</td><td>ViF</td><td>-0.3 to VCC+0.3</td><td>V</td></tr><tr><td rowspan="2">Lamp</td><td>High voltage side (Hot) Note3</td><td>ViBLH</td><td>TBD</td><td>Vrms</td></tr><tr><td>Low voltage side (Cold) Note4</td><td>ViBLC</td><td>TBD</td><td>Vrms</td></tr><tr><td colspan="3">Storage temperature</td><td>Tst</td><td>-30 to +80</td><td>℃</td><td rowspan="3">-</td></tr><tr><td rowspan="2">Operating temperature</td><td colspan="2">Front surface</td><td>TopF</td><td>-10 to +70</td><td>℃</td></tr><tr><td colspan="2">Rear surface</td><td>TopR</td><td>TBD</td><td>℃</td></tr><tr><td colspan="3" rowspan="4">Relative humidity Note5</td><td rowspan="4">RH</td><td>≤ 95</td><td>%</td><td>Ta ≤ 40℃</td></tr><tr><td>≤ 85</td><td>%</td><td>40 < Ta ≤ 50℃</td></tr><tr><td>≤ 60</td><td>%</td><td>50 < Ta ≤ 60℃</td></tr><tr><td>≤ 42</td><td>%</td><td>60 < Ta ≤ 70℃</td></tr><tr><td colspan="3">Absolute humidity Note5</td><td>-</td><td>≤ 78 Note6</td><td>g/m³</td><td>Ta > 70℃</td></tr></table>	Parameter			Symbol	Rating	Unit	Remarks	Supply voltage	LCD panel signal board and driver		VCC	-0.3 to +6.5	V	Ta = 25℃	Input voltage	LCD panel signal board	Display signals Note1	ViD	-0.3 to VCC+0.3	V	Function signals Note2	ViF	-0.3 to VCC+0.3	V	Lamp	High voltage side (Hot) Note3	ViBLH	TBD	Vrms	Low voltage side (Cold) Note4	ViBLC	TBD	Vrms	Storage temperature			Tst	-30 to +80	℃	-	Operating temperature	Front surface		TopF	-10 to +70	℃	Rear surface		TopR	TBD	℃	Relative humidity Note5			RH	≤ 95	%	Ta ≤ 40℃	≤ 85	%	40 < Ta ≤ 50℃	≤ 60	%	50 < Ta ≤ 60℃	≤ 42	%	60 < Ta ≤ 70℃	Absolute humidity Note5			-	≤ 78 Note6	g/m³	Ta > 70℃
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(4) page 8/24 (2) Backlight																																																																										
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→ page 9/35 4.3.2 Working for backlight																																																																										
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2nd edition	DOD - M - 0577	Aug. 27, 2001	(5) page 9/24 (1) Interface signals, power supply Module side connector CN1 socket: IL-FPR-33S-HF (Supplier: Japan Aviation Electronics Industry limited (JAE)) Adaptable FPC plug TBD (Supplier: TBD) <table><tr><th>Pin No.</th><th>Symbols</th><th>Functions</th><th>Pin No.</th><th>Symbols</th><th>Functions</th></tr><tr><td>1</td><td>GND</td><td>Ground</td><td>19</td><td>GND</td><td>Ground</td></tr><tr><td>2</td><td>CLK</td><td>Dot clock</td><td>20</td><td>B0</td><td>Blue data (LSB)</td></tr><tr><td>3</td><td>Hsync</td><td>Horizontal sync.</td><td>21</td><td>B1</td><td>Blue data</td></tr><tr><td>4</td><td>Vsync</td><td>Vertical sync.</td><td>22</td><td>B2</td><td>Blue data</td></tr><tr><td>5</td><td>GND</td><td>Ground</td><td>23</td><td>B3</td><td>Blue data</td></tr><tr><td>6</td><td>R0</td><td>Red data (LSB)</td><td>24</td><td>B4</td><td>Blue data</td></tr><tr><td>7</td><td>R1</td><td>Red data</td><td>25</td><td>B5</td><td>Blue data (MSB)</td></tr><tr><td>8</td><td>R2</td><td>Red data</td><td>26</td><td>GND</td><td>Ground</td></tr><tr><td>9</td><td>R3</td><td>Red data</td><td>27</td><td>DE</td><td>Data enable Note 2</td></tr><tr><td>10</td><td>R4</td><td>Red data</td><td>28</td><td>VCC</td><td>Power supply Note 1</td></tr><tr><td>11</td><td>R5</td><td>Red data (MSB)</td><td>29</td><td>VCC</td><td>Power supply Note 1</td></tr><tr><td>12</td><td>GND</td><td>Ground</td><td>30</td><td>R/L</td><td>Mode select signal Note 3</td></tr><tr><td>13</td><td>G0</td><td>Green data (LSB)</td><td>31</td><td>U/D</td><td>Mode select signal Note 3</td></tr><tr><td>14</td><td>G1</td><td>Green data</td><td>32</td><td>GND</td><td>Ground</td></tr><tr><td>15</td><td>G2</td><td>Green data</td><td>33</td><td>GND</td><td>Ground</td></tr><tr><td>16</td><td>G3</td><td>Green data</td><td></td><td></td><td></td></tr><tr><td>17</td><td>G4</td><td>Green data</td><td></td><td></td><td></td></tr><tr><td>18</td><td>G5</td><td>Green data (MSB)</td><td></td><td></td><td></td></tr></table> → page 12/35 4.5.1 LCD panel signal processing board CN1 socket (LCD module side): 08-6210-033-340-800 (Kyocera Elco Corp.) Adaptable plug: Flexible cable <table><tr><th>Pin No.</th><th>Symbol</th><th>Signal</th><th>Remarks</th></tr><tr><td>1</td><td>GND</td><td>Ground</td><td rowspan="4">-</td></tr><tr><td>2</td><td>CLK</td><td>Dot clock</td></tr><tr><td>3</td><td>Hsync</td><td>Horizontal synchronous</td></tr><tr><td>4</td><td>Vsync</td><td>Vertical synchronous</td></tr><tr><td>5</td><td>GND</td><td>Ground</td><td></td></tr><tr><td>6</td><td>R0</td><td>Red data (LSB)</td><td>Least significant bit</td></tr><tr><td>7</td><td>R1</td><td>Red data</td><td rowspan="4">-</td></tr><tr><td>8</td><td>R2</td><td>Red data</td></tr><tr><td>9</td><td>R3</td><td>Red data</td></tr><tr><td>10</td><td>R4</td><td>Red data</td></tr><tr><td>11</td><td>R5</td><td>Red data (MSB)</td><td>Most significant bit</td></tr><tr><td>12</td><td>GND</td><td>Ground</td><td>-</td></tr><tr><td>13</td><td>G0</td><td>Green data (LSB)</td><td>Least significant bit</td></tr><tr><td>14</td><td>G1</td><td>Green data</td><td rowspan="4">-</td></tr><tr><td>15</td><td>G2</td><td>Green data</td></tr><tr><td>16</td><td>G3</td><td>Green data</td></tr><tr><td>17</td><td>G4</td><td>Green data</td></tr><tr><td>18</td><td>G5</td><td>Green data (MSB)</td><td>Most significant bit</td></tr><tr><td>19</td><td>GND</td><td>Ground</td><td>-</td></tr><tr><td>20</td><td>B0</td><td>Blue data (LSB)</td><td>Least significant bit</td></tr><tr><td>21</td><td>B1</td><td>Blue data</td><td rowspan="4">-</td></tr><tr><td>22</td><td>B2</td><td>Blue data</td></tr><tr><td>23</td><td>B3</td><td>Blue data</td></tr><tr><td>24</td><td>B4</td><td>Blue data</td></tr><tr><td>25</td><td>B5</td><td>Blue data (MSB)</td><td>Most significant bit</td></tr><tr><td>26</td><td>GND</td><td>Ground</td><td>-</td></tr><tr><td>27</td><td>DE</td><td>Select of DE / Fixed mode</td><td>DE mode: Data enable signal, Fixed mode: Open</td></tr><tr><td>28</td><td>VCC</td><td>Power supply</td><td rowspan="2">-</td></tr><tr><td>29</td><td>VCC</td><td>Power supply</td></tr><tr><td>30</td><td>DPSH</td><td>Select of scan direction (Horizontal)</td><td rowspan="2">Normal scan: Low or Open, Reverse scan: High Note1</td></tr><tr><td>31</td><td>DPSV</td><td>Select of scan direction (Vertical)</td></tr><tr><td>32</td><td>PNS</td><td>Select of pixel number</td><td>QVGA mode: High, VGA mode: Low or Open Note1</td></tr><tr><td>33</td><td>GND</td><td>Ground</td><td>-</td></tr></table>	Pin No.	Symbols	Functions	Pin No.	Symbols	Functions	1	GND	Ground	19	GND	Ground	2	CLK	Dot clock	20	B0	Blue data (LSB)	3	Hsync	Horizontal sync.	21	B1	Blue data	4	Vsync	Vertical sync.	22	B2	Blue data	5	GND	Ground	23	B3	Blue data	6	R0	Red data (LSB)	24	B4	Blue data	7	R1	Red data	25	B5	Blue data (MSB)	8	R2	Red data	26	GND	Ground	9	R3	Red data	27	DE	Data enable Note 2	10	R4	Red data	28	VCC	Power supply Note 1	11	R5	Red data (MSB)	29	VCC	Power supply Note 1	12	GND	Ground	30	R/L	Mode select signal Note 3	13	G0	Green data (LSB)	31	U/D	Mode select signal Note 3	14	G1	Green data	32	GND	Ground	15	G2	Green data	33	GND	Ground	16	G3	Green data				17	G4	Green data				18	G5	Green data (MSB)				Pin No.	Symbol	Signal	Remarks	1	GND	Ground	-	2	CLK	Dot clock	3	Hsync	Horizontal synchronous	4	Vsync	Vertical synchronous	5	GND	Ground		6	R0	Red data (LSB)	Least significant bit	7	R1	Red data	-	8	R2	Red data	9	R3	Red data	10	R4	Red data	11	R5	Red data (MSB)	Most significant bit	12	GND	Ground	-	13	G0	Green data (LSB)	Least significant bit	14	G1	Green data	-	15	G2	Green data	16	G3	Green data	17	G4	Green data	18	G5	Green data (MSB)	Most significant bit	19	GND	Ground	-	20	B0	Blue data (LSB)	Least significant bit	21	B1	Blue data	-	22	B2	Blue data	23	B3	Blue data	24	B4	Blue data	25	B5	Blue data (MSB)	Most significant bit	26	GND	Ground	-	27	DE	Select of DE / Fixed mode	DE mode: Data enable signal, Fixed mode: Open	28	VCC	Power supply	-	29	VCC	Power supply	30	DPSH	Select of scan direction (Horizontal)	Normal scan: Low or Open, Reverse scan: High Note1	31	DPSV	Select of scan direction (Vertical)	32	PNS	Select of pixel number	QVGA mode: High, VGA mode: Low or Open Note1	33	GND	Ground	-
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			7.10. OPTICAL CHARACTERISTICS																																																																																														
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			Parameters	Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks	Luminance	Lumax	Note 3	320	400	—	cd/m ²	Note 2	Contrast ratio	CR	Note 3	TBD	300	—	—	Note 4	Luminance uniformity	—	Max. / Min.	—	TBD	TBD	—	Note 7																																																															
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			Luminance uniformity	—	Max. / Min.	—	TBD	TBD	—	Note 7																																																																																							
			Reference data																																																																																														
			Ta = 25°C, Note1																																																																																														
Items	Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks	Color gamut	C	At center, to NTSC	TBD	50	—	%	—	Chromaticity coordinate	W	White (x,y) Note 3	TBD	TBD	TBD	—	—	R	Red (x,y) Note 3	—	TBD	—	—	G	Green (x,y) Note 3	—	TBD	—	—	B	Blue (x,y) Note 3	—	TBD	—	—	Viewing angle range	Horizontal	θx+	CR > 5, θy=±0°	TBD	65	—	deg.	Note 5	θx-	CR > 5, θy=±0°	TBD	65	—	deg.	Vertical	θy+	CR > 5, θx=±0°	TBD	40	—	deg.	θy-	CR > 5, θx=±0°	TBD	65	—	deg.	Response time	Ton	White to Black	(100%→10%)	—	TBD	30	ms	Note 6	Black to White	(90%→10%)	—	TBD	—	—	Toff	Black to White	(0%→90%)	—	TBD	60	ms	White to Black	(10%→90%)	—	TBD	—	—
Items	Symbols	Conditions	Min.	Typ.	Max.	Units	Remarks																																																																																										
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4.10.1 Optical characteristics																																																																																																	
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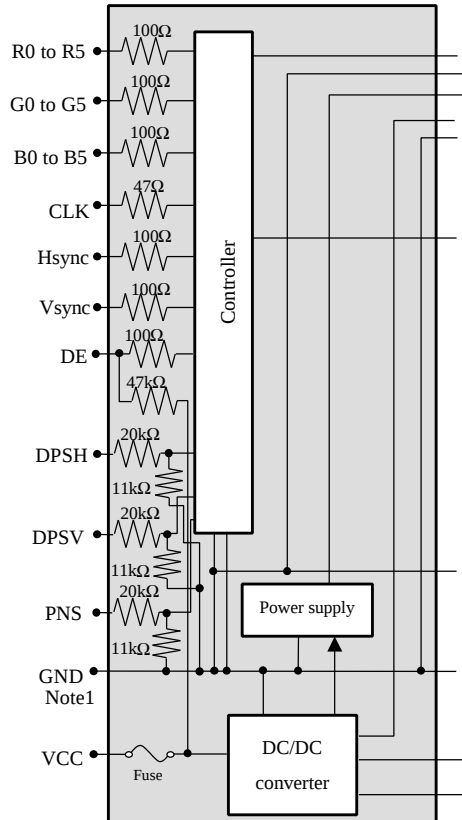
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3rd edition	DOD - M - 0625	Sep. 18, 2001	Revision contents • Change part (Before-2nd edition → After-3rd edition) (1) page 8/35 4.2 ABSOLUTE MAXIMUM RATINGS VBLH TBD Vrms VBLC TBD Vrms → page 8/37 4.2 ABSOLUTE MAXIMUM RATINGS VBLH 1,500 Vrms VBLC 42.4 Vrms (2) page 9/35 4.3.1 Driving for LCD panel signal processing board <table><tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remarks</th></tr><tr><td>Supply voltage</td><td>VCC</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td><td>-</td></tr><tr><td>Supply current</td><td>ICC</td><td>-</td><td>180 Note1</td><td>250</td><td>mA</td><td>VCC = 3.3V</td></tr><tr><td rowspan="2">Logic input voltage for display signals</td><td>Low</td><td>ViDLL</td><td>0</td><td>-</td><td>0.3Vcc</td><td>V</td></tr><tr><td>High</td><td>ViDLH</td><td>0.7Vcc</td><td>-</td><td>Vcc</td><td>V</td></tr><tr><td rowspan="2">Input voltage for DPSH or DPSV signals</td><td>Low</td><td>ViFDL</td><td>0</td><td>-</td><td>0.3Vcc</td><td>V</td></tr><tr><td>High</td><td>ViFDH</td><td>0.7Vcc</td><td>-</td><td>Vcc</td><td>V</td></tr><tr><td rowspan="2">Input voltage for PNS signal</td><td>Low</td><td>ViFPL</td><td>0</td><td>-</td><td>0.3Vcc</td><td>V</td></tr><tr><td>High</td><td>ViFPH</td><td>0.7Vcc</td><td>-</td><td>Vcc</td><td>V</td></tr></table> → page 9/37 4.3.1 Driving for LCD panel signal processing board <table><tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remarks</th></tr><tr><td rowspan="2">Supply voltage</td><td rowspan="2">VCC</td><td>3.0</td><td>3.3</td><td>3.6</td><td>V</td><td>for 3V system</td></tr><tr><td>4.7</td><td>5.0</td><td>5.3</td><td>V</td><td>for 5V system</td></tr><tr><td rowspan="2">Supply current</td><td rowspan="2">ICC</td><td>-</td><td>180 Note1</td><td>250</td><td>mA</td><td>VCC = 3.3V</td></tr><tr><td>-</td><td>120 Note1</td><td>165</td><td>mA</td><td>VCC = 5.0V</td></tr><tr><td rowspan="2">Logic input voltage for display signals</td><td>Low</td><td>VDLL</td><td>0</td><td>-</td><td>0.3Vcc</td><td>V</td></tr><tr><td>High</td><td>VDLH</td><td>0.7Vcc</td><td>-</td><td>Vcc</td><td>V</td></tr><tr><td rowspan="2">Input voltage for DPSH or DPSV signals</td><td>Low</td><td>VFDL</td><td>0</td><td>-</td><td>0.3Vcc</td><td>V</td></tr><tr><td>High</td><td>VFDH</td><td>0.7Vcc</td><td>-</td><td>Vcc</td><td>V</td></tr><tr><td rowspan="2">Input voltage for PNS signal</td><td>Low</td><td>VFPL</td><td>0</td><td>-</td><td>0.3Vcc</td><td>V</td></tr><tr><td>High</td><td>VFPH</td><td>0.7Vcc</td><td>-</td><td>Vcc</td><td>V</td></tr></table> (3) page 10/35 4.3.4 Fuses <table><tr><th colspan="2">Fuse</th><th rowspan="2">Rating Note1</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Type</th><th>Supplier</th></tr><tr><td rowspan="2">ICP-S1.8</td><td rowspan="2">ROHM Co., Ltd.</td><td>1.8</td><td>A</td><td rowspan="2">VCC (for LCD panel signal processing board)</td></tr><tr><td>50</td><td>V</td></tr></table> Note1: The power capacity should be more than twice of fuse current ratings. If the power capacity is less than the criteria value, the fuse may not blow, and then nasty smell, smoking and so on may occur. (This part continues to the next page.)	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks	Supply voltage	VCC	3.0	3.3	3.6	V	-	Supply current	ICC	-	180 Note1	250	mA	VCC = 3.3V	Logic input voltage for display signals	Low	ViDLL	0	-	0.3Vcc	V	High	ViDLH	0.7Vcc	-	Vcc	V	Input voltage for DPSH or DPSV signals	Low	ViFDL	0	-	0.3Vcc	V	High	ViFDH	0.7Vcc	-	Vcc	V	Input voltage for PNS signal	Low	ViFPL	0	-	0.3Vcc	V	High	ViFPH	0.7Vcc	-	Vcc	V	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks	Supply voltage	VCC	3.0	3.3	3.6	V	for 3V system	4.7	5.0	5.3	V	for 5V system	Supply current	ICC	-	180 Note1	250	mA	VCC = 3.3V	-	120 Note1	165	mA	VCC = 5.0V	Logic input voltage for display signals	Low	VDLL	0	-	0.3Vcc	V	High	VDLH	0.7Vcc	-	Vcc	V	Input voltage for DPSH or DPSV signals	Low	VFDL	0	-	0.3Vcc	V	High	VFDH	0.7Vcc	-	Vcc	V	Input voltage for PNS signal	Low	VFPL	0	-	0.3Vcc	V	High	VFPH	0.7Vcc	-	Vcc	V	Fuse		Rating Note1	Unit	Remarks	Type	Supplier	ICP-S1.8	ROHM Co., Ltd.	1.8	A	VCC (for LCD panel signal processing board)	50	V
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks																																																																																																																																													
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3rd edition	DOD - M - 0625	Sep. 18, 2001	(This part continues from the front page.) → page 10/37 4.3.4 Fuses <table><tr><th rowspan="2">Fusing line</th><th colspan="2">Fuse</th><th rowspan="2">Rating</th><th rowspan="2">Unit</th><th rowspan="2">Remark</th></tr><tr><th>Type</th><th>Supplier</th></tr><tr><td rowspan="2">VCC</td><td rowspan="2">ICP-S1.8</td><td rowspan="2">ROHM Co., Ltd.</td><td>4.0</td><td>A</td><td>Note1, Note2</td></tr><tr><td>50</td><td>V</td><td>-</td></tr></table> Note1: This current rating is a fusing current. Note2: The power capacity should be more than the fusing current rating. If the power capacity is less than the criteria value, the fuse may not blow, and then nasty smell, smoking and so on may occur. Writer Approved by Checked by Prepared by T. ITO A. SAWADA	Fusing line	Fuse		Rating	Unit	Remark	Type	Supplier	VCC	ICP-S1.8	ROHM Co., Ltd.	4.0	A	Note1, Note2	50	V	-
Fusing line	Fuse		Rating		Unit	Remark														
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VCC	ICP-S1.8	ROHM Co., Ltd.	4.0	A	Note1, Note2															
			50	V	-															
4th edition	DOD - M - 0664	Oct. 2, 2001	Revision contents • Change part (Before-3rd edition → After-4th edition) (1) page 7/37 3. BLOCK DIAGRAM LCD panel signal processing board FG Note1 (This part continues to the next page.)																	

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Edition	Document number	Prepared date	Revision contents and writer																												
4th edition	DOD - M - 0664	Oct. 2, 2001	(This part continues from the front page.) → page 7/42 3. BLOCK DIAGRAM  LCD panel signal processing board (2) page 10/37 4.3.3 Power supply voltage ripple <table><tr><th>Parameter</th><th>Supply voltage</th><th>Ripple voltage (Measure at input terminal of power supply)</th><th>Note1</th><th>Unit</th></tr><tr><td rowspan="2">VCC</td><td>3.3 V</td><td>≤ 100</td><td></td><td>mVp-p</td></tr><tr><td>5.0 V</td><td>≤ TBD</td><td></td><td>mVp-p</td></tr></table> → page 10/42 4.3.3 Power supply voltage ripple <table><tr><th>Parameter</th><th>Power supply voltage</th><th>Ripple voltage (Measure at input terminal of power supply)</th><th>Note1</th><th>Unit</th></tr><tr><td rowspan="2">VCC</td><td>3.3 V</td><td>≤ 100</td><td></td><td>mVp-p</td></tr><tr><td>5.0 V</td><td>≤ 100</td><td></td><td>mVp-p</td></tr></table>	Parameter	Supply voltage	Ripple voltage (Measure at input terminal of power supply)	Note1	Unit	VCC	3.3 V	≤ 100		mVp-p	5.0 V	≤ TBD		mVp-p	Parameter	Power supply voltage	Ripple voltage (Measure at input terminal of power supply)	Note1	Unit	VCC	3.3 V	≤ 100		mVp-p	5.0 V	≤ 100		mVp-p
Parameter	Supply voltage	Ripple voltage (Measure at input terminal of power supply)	Note1	Unit																											
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4th edition	DOD - M - 0664	Oct. 2, 2001	(3) page 23/37 4.9.7 Timing characteristics for QVGA display mode • Common to DE mode and fixed mode <table><tr><th colspan="2">Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remarks</th></tr><tr><td rowspan="3">CLK</td><td>Frequency</td><td>tcf</td><td>TBD</td><td>6.4</td><td>7.0</td><td>MHz</td><td>157.5 ns (typ.) Note1</td></tr><tr><td>Duty</td><td>tcd</td><td>0.4</td><td>-</td><td>0.6</td><td>-</td><td>Note1</td></tr><tr><td>Rise time, Fall time</td><td>tcrf</td><td>-</td><td>-</td><td>10</td><td>ns</td><td rowspan="4">-</td></tr><tr><td rowspan="3">DATA</td><td rowspan="2">CLK-DATA</td><td>Setup time</td><td>tds</td><td>2</td><td>-</td><td>-</td><td>ns</td></tr><tr><td>Hold time</td><td>tdh</td><td>3</td><td>-</td><td>-</td><td>ns</td></tr><tr><td>Rise time, Fall time</td><td>tdrf</td><td>-</td><td>-</td><td>10</td><td>ns</td></tr></table> Note1: Definition of units is as follows. tcf = 1/tc, tcd = tch/tc = tch×tcd • DE mode <table><tr><th colspan="2">Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remarks</th></tr><tr><td rowspan="8">DE</td><td rowspan="2">Horizontal</td><td>Cycle</td><td>th</td><td>TBD</td><td>404</td><td>-</td><td>CLK</td><td rowspan="4">Note1</td></tr><tr><td>Display period</td><td>thd</td><td></td><td>320</td><td></td><td>CLK</td></tr><tr><td rowspan="2">Vertical (One frame)</td><td>Cycle</td><td>tv</td><td>TBD</td><td>262</td><td>-</td><td>H</td></tr><tr><td>Display period</td><td>tvd</td><td></td><td>240</td><td></td><td>H</td></tr><tr><td rowspan="2">CLK-DE</td><td>Setup time</td><td>tdes</td><td>2</td><td>-</td><td>-</td><td>ns</td><td rowspan="2">-</td></tr><tr><td>Hold time</td><td>tdeh</td><td>3</td><td>-</td><td>-</td><td>ns</td></tr><tr><td colspan="2">Rise time, Fall time</td><td>tderf</td><td>-</td><td>-</td><td>10</td><td>ns</td></tr></table> Note1: Definition of units is as follows. tc = 1CLK, th = 1H • Fixed mode <table><tr><th colspan="2">Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remarks</th></tr><tr><td rowspan="11">Hsync</td><td rowspan="2">Cycle</td><td>th</td><td>50.0</td><td>63.6</td><td>TBD</td><td>ms</td><td>31.4 kHz (typ.)</td></tr><tr><td></td><td></td><td>404</td><td></td><td>CLK</td><td rowspan="5">Note1</td></tr><tr><td>Display period</td><td>thd</td><td></td><td>320</td><td></td><td>CLK</td></tr><tr><td>Front-porch</td><td>thf</td><td></td><td>TBD</td><td></td><td>CLK</td></tr><tr><td>Pulse width</td><td>thp</td><td>TBD</td><td>TBD</td><td>-</td><td>CLK</td></tr><tr><td>Back-porch</td><td>thb</td><td>-</td><td>TBD</td><td>TBD</td><td>CLK</td></tr><tr><td colspan="2">Total of pulse width and back-porch</td><td>thp + thb</td><td></td><td>TBD</td><td></td><td>CLK</td><td>Note1, Note2</td></tr><tr><td rowspan="2">CLK- Hsync</td><td>Setup time</td><td>ths</td><td>2</td><td>-</td><td>-</td><td>ns</td><td rowspan="2">-</td></tr><tr><td>Hold time</td><td>thh</td><td>3</td><td>-</td><td>-</td><td>ns</td></tr><tr><td colspan="2">Rise time, Fall time</td><td>thrf</td><td>-</td><td>-</td><td>10</td><td>ns</td><td></td></tr><tr><td rowspan="10">Vsync</td><td rowspan="2">Cycle</td><td>tv</td><td>TBD</td><td>16.7</td><td>17.2</td><td>ms</td><td>59.9 Hz (typ.)</td></tr><tr><td></td><td></td><td>525</td><td></td><td>H</td><td rowspan="5">Note1</td></tr><tr><td>Display period</td><td>tvd</td><td></td><td>480</td><td></td><td>H</td></tr><tr><td>Front-porch</td><td>tvf</td><td></td><td>1</td><td></td><td>H</td></tr><tr><td>Pulse width</td><td>tvp</td><td>1</td><td>-</td><td>TBD</td><td>H</td></tr><tr><td>Back-porch</td><td>tvb</td><td>TBD</td><td>-</td><td>TBD</td><td>H</td></tr><tr><td colspan="2">Total of pulse width and back-porch</td><td>tvp + tvb</td><td></td><td>TBD</td><td></td><td>H</td><td>Note1, Note2</td></tr><tr><td rowspan="2">Vsync-Hsync</td><td>Setup time</td><td>tvhs</td><td>2</td><td>-</td><td>-</td><td>ns</td><td>Note1</td></tr><tr><td>Hold time</td><td>tvhh</td><td>3</td><td>-</td><td>-</td><td>CLK</td><td></td></tr><tr><td colspan="2">Rise time, Fall time</td><td>tvrf</td><td>-</td><td>-</td><td>10</td><td>ns</td><td>-</td></tr></table> Note1: Definition of units is as follows. tc = 1CLK, th = 1H Note2: Keep tvp + tvb and thp + thb within the table. If it is out of specification, display position will be shifted to right/left side or up/down. (This part continues to the next page.)	Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks	CLK	Frequency	tcf	TBD	6.4	7.0	MHz	157.5 ns (typ.) Note1	Duty	tcd	0.4	-	0.6	-	Note1	Rise time, Fall time	tcrf	-	-	10	ns	-	DATA	CLK-DATA	Setup time	tds	2	-	-	ns	Hold time	tdh	3	-	-	ns	Rise time, Fall time	tdrf	-	-	10	ns	Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks	DE	Horizontal	Cycle	th	TBD	404	-	CLK	Note1	Display period	thd		320		CLK	Vertical (One frame)	Cycle	tv	TBD	262	-	H	Display period	tvd		240		H	CLK-DE	Setup time	tdes	2	-	-	ns	-	Hold time	tdeh	3	-	-	ns	Rise time, Fall time		tderf	-	-	10	ns	Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks	Hsync	Cycle	th	50.0	63.6	TBD	ms	31.4 kHz (typ.)			404		CLK	Note1	Display period	thd		320		CLK	Front-porch	thf		TBD		CLK	Pulse width	thp	TBD	TBD	-	CLK	Back-porch	thb	-	TBD	TBD	CLK	Total of pulse width and back-porch		thp + thb		TBD		CLK	Note1, Note2	CLK- Hsync	Setup time	ths	2	-	-	ns	-	Hold time	thh	3	-	-	ns	Rise time, Fall time		thrf	-	-	10	ns		Vsync	Cycle	tv	TBD	16.7	17.2	ms	59.9 Hz (typ.)			525		H	Note1	Display period	tvd		480		H	Front-porch	tvf		1		H	Pulse width	tvp	1	-	TBD	H	Back-porch	tvb	TBD	-	TBD	H	Total of pulse width and back-porch		tvp + tvb		TBD		H	Note1, Note2	Vsync-Hsync	Setup time	tvhs	2	-	-	ns	Note1	Hold time	tvhh	3	-	-	CLK		Rise time, Fall time		tvrf	-	-	10	ns	-
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REVISION HISTORY

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4th edition	DOD - M - 0664	Oct. 2, 2001	(This part continues from the front page.) → page 23/42 4.9.7 Timing characteristics for QVGA display mode • Common to DE mode and fixed mode <table><tr><th colspan="2">Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th>Remarks</th></tr><tr><td rowspan="3">CLK</td><td>Frequency</td><td>tcf</td><td>5.0</td><td>6.4</td><td>7.0</td><td>MHz</td><td>157.5 ns (typ.) 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Note1		800			CLK	Display period	thd	640			CLK	Front-porch	thf	16			CLK	Pulse width	thp	10	96	-	CLK	Back-porch	thb	-	48	134	CLK	Note1, Note2	Total of pulse width and back-porch	thp + thb	144			CLK	CLK- Hsync	Setup time	ths	8	-	-	ns	-	Hold time	thh	12	-	-	ns	Rise time, Fall time	thrf	-	-	10	ns	Vsync	Cycle	tv	16.1	16.7	17.2	ms	59.9 Hz (typ.)	Note1		525			H	Display period	tvd	480			H	Front-porch	tvf	12			H	Pulse width	tvp	1	-	2	H	Back-porch	tvb	31	-	32	H	Note1, Note2	Total of pulse width and back-porch	tvp + tvb	33			H	Vsync-Hsync	Setup time	tvhs	1	-	-	CLK	Note1	Hold time	tvhh	30	-	-	ns	-	Rise time, Fall time	tvrf	-	-	10	ns
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Unit	Remarks	Hsync	Cycle	th	27.6	31.8	38.1	ms	31.4 kHz (typ.)	800			CLK	Note1	Display period	thd	640			CLK	Front-porch	thf	16			CLK	Pulse width	thp	10	-	127	CLK	Back-porch	thb	17	-	134	CLK	Total of pulse width and back-porch		thp + thb	144			CLK	Note1, Note2	CLK- Hsync	Setup time	ths	8	-	-	ns	-	Hold time	thh	12	-	-	ns	Rise time, Fall time		thrf	-	-	10	ns	Vsync	Cycle	tv	14.5	16.7	20.0	ms	59.9 Hz (typ.)	525			H	Note1	Display period	tvd	480			H	Front-porch	tvf	12			H	Pulse width	tvp	2	-	29	H	Back-porch	tvb	4	-	31	H	Total of pulse width and back-porch		tvp + tvb	33			H	Note1, Note2	Vsync-Hsync	Setup time	tvhs	1	-	-	CLK	Note1	Hold time	tvhh	15	-	-	ns	Rise time, Fall time		tvrf	-	-	10	ns	-
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REVISION HISTORY

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5th edition	DOD - M - 0788	Nov. 28, 2001	Revision contents																
			• Change part (Before-4th edition → After-5th edition)																
			(1) <i>page 6/42</i>																
			2. GENERAL SPECIFICATIONS																
			<i>Contrast ratio</i> 300:1 (typ.)																
			<i>Response time</i> 3 ms (typ.)																
			→																
			<i>page 6/44</i>																
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(2) <i>page 9/42</i>																			
4.3.2 Working for backlight lamp																			
<table><tr><td>Power supply current</td><td>IBL</td><td>25°C</td><td>3.0</td><td>5.0</td><td>5.5</td><td>mArms</td><td>Note2</td></tr><tr><td>Oscillation frequency</td><td>FO</td><td>25°C</td><td>40</td><td>45</td><td>50</td><td>kHz</td><td>Note3</td></tr></table>	Power supply current	IBL	25°C	3.0	5.0	5.5	mArms	Note2	Oscillation frequency	FO	25°C	40	45	50	kHz	Note3			
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(3) <i>page 12/42</i>																			
4.5.1 LCD panel signal processing board																			
PNS QVGA mode: High, VGA mode: Low or Open																			
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(4) <i>page 23/42</i>																			
4.9.7 Timing characteristics for QVGA display mode																			
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