Two-Way Mixed-Voltage Interfacing of Actel's SX FPGAs

Introduction

In the past, bipolar circuits with a 5V standard power supply voltage dominated digital system designs. CMOS IC manufacturers adopted this power supply voltage, and most system components are still available in the 5V version. In order to achieve even higher speeds and densities at a lower cost and with lower power consumption, the CMOS IC manufacturers have developed advanced deep-submicron fabrication, thinner gate oxides, and process geometries as small as 0.25 µm, with 0.18 µm expected in the future.

The disadvantage of designing submicron devices using a 5V power supply voltage is the high-field-effect failure resulting from hot-carrier injection. To decrease these failures, a lower supply voltage was needed to power up these new devices, leading to the introduction of the 3.3V standard power supply voltage devices. This necessitated two-way mixed-voltage interfacing to support the existing 5V standard power supply system designs.

This Application Note describes the two-way mixed-voltage interfacing specifications available in Actel's SX family of FPGAs. SX devices support I/Os that can be used as either regular I/Os or as PCI compliant I/Os. With specific I/O designs, the 54SX16P can meet the two-way mixed-voltage interfacing design requirement. Furthermore, the 54SX16P can be configured to meet the PCI compliant specification. Table 2, Table 3, and Table 4 on page 2 list the DC electrical characteristics of the SX FPGAs.

TTL Interface Levels

Figure 1 shows the standard TTL (5V) and LVTTL (3.3V) DC interface levels. Both standards use the same interface voltage levels.

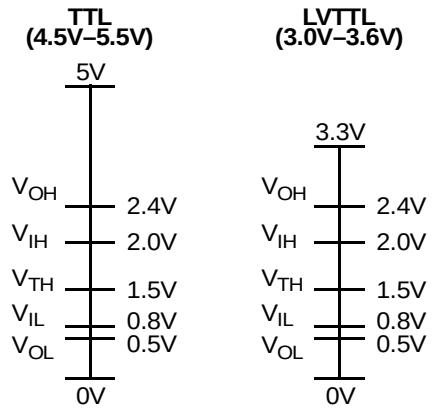

Figure 1 • *5V (TTL) and 3.3V (low-voltage TTL) Interfaces*

54SX08, 54SX16, and 54SX32 Operating Mode

To ensure that the 54SX08, 54SX16, and 54SX32 devices can be utilized in different systems, they have been designed to meet various system interface requirements. Table 1 shows the required V_{CCA}, V_{CCI}, and V_{CCR} operating voltages.

The 54SX08, 54SX16, and 54SX32 devices accept LVTTL/TTL signals on all inputs, and the outputs can drive any LVTTL/TTL devices. The V_{CCA} and V_{CCI} pins must be suplied with 3.3V, while the V_{CCR} pin must be supplied with 5V. The outputs are only driven up to 3.3V. Figure 2 shows the operating configuration that is intended for mixed LVTTL/TTL systems.

Table 1 • *SX Operating Configuration*

Description	V_{CCA}	V_{CCI}	V_{CCR}	Input Voltage Tolerance	Output Voltage (Max)
LVTTL/TTL	3.3V	3.3V	5V	3.3V/5V	3.3V

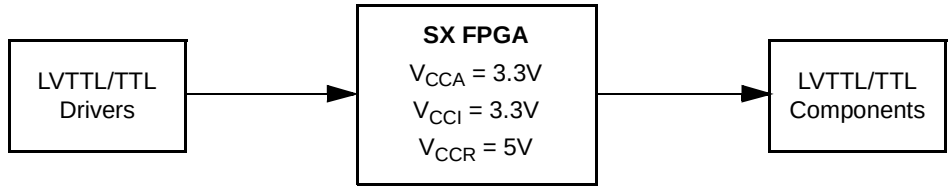

Figure 2 • *SX Operating Mode for Mixed LVTTL/TTL Systems*

Table 2 • DC Electrical Characteristics for 54SX08, 54SX16, 54SX32, and 54SX16P

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
V_{CCA}	Supply Voltage for Array	3.0	3.6	3.0	3.6	Volts
V_{CCI}	I/O Supply Voltage	3.0	3.6	3.0	3.6	Volts
V_{CCR}	Supply Voltage required for Internal Biasing	4.75	5.25	4.5	5.5	Volts
V_{IL}	Input Low Voltage		0.8		0.8	Volts
V_{IH}	Input High Voltage	2.0		2.0		Volts
V_{OL}	I_{OL} = 20 µA (CMOS)		0.1			Volts
	I_{OL} = 12 mA (TTL)		0.5			Volts
	I_{OL} = 8 mA (TTL)				0.5	Volts
V_{OH}	I_{OH} = –20 µA (CMOS)	(V_{CCI} – 0.1)	V_{CCI}	(V_{CCI} – 0.1)	V_{CCI}	Volts
	I_{OH} = –8 mA (TTL)	2.4	V_{CCI}			Volts
	I_{OH} = –6 mA (TTL)			2.4	V_{CCI}	Volts

Table 3 • 5V PCI DC Electrical Characteristics for 54SX16P

Symbol	Parameter and Condition		Commercial		Units
			Min.	Max.	
V_{CCA}	Supply Voltage for Array		3.0	3.6	Volts
V_{CCI}	I/O Supply Voltage		4.75	5.25	Volts
V_{CCR}	Supply Voltage required for Internal Biasing		4.75	5.25	Volts
V_{IL}	Input Low Voltage		–0.5	0.8	Volts
V_{IH}	Input High Voltage		2.0	V_{CCI} + 0.5	Volts
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5V		–70	µA
I_{IH}	Input High Leakage Current	V_{IN} = 2.7V		70	µA
V_{OL}	Output Low Voltage				
	I_{OL} = 3 mA (signals without pull up resistor)			0.55	Volts
	I_{OL} = 6 mA (signals requiring pull up resistor)			0.55	Volts
V_{OH}	Output High Voltage	I_{OH} = –2 mA	2.4		Volts

Table 4 • 3.3V PCI DC Electrical Characteristics for 54SX16P

Symbol	Parameter and Condition		Commercial		Units
			Min.	Max.	
V_{CCA}	Supply Voltage for Array		3.0	3.6	Volts
V_{CCI}	I/O Supply Voltage		3.0	3.6	Volts
V_{CCR}	Supply Voltage required for Internal Biasing		3.0	3.6	Volts
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	Volts
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	Volts
V_{IPU}	Input Pull-up Voltage[1]			$0.7V_{CC}$	
I_{IH}	Input Low Leakage Current	$0 < V_{IN} < V_{CCI}$		±10	µA
V_{OL}	Output Low Voltage	I_{OL} = 1500µA		$0.1V_{CCI}$	Volts
V_{OH}	Output High Voltage	I_{OH} = –500µA	$0.9V_{CCI}$		Volts

Note:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*

54SX16P Operating Modes

The 54SX16P FPGA has added system flexibility because it has been designed with three operating modes as shown in Table 5.

Mode A (3.3V PCI/LVTTL)

In Mode A, the 54SX16P device accepts 3.3V PCI/LVTTL signals on all inputs, and the outputs can drive any 3.3V PCI/ LVTTL/TTL devices. The V_{CCA}, V_{CCI}, and V_{CCR} pins must be supplied with 3.3V. This mode is intended for 3.3V PCI/LVTTL systems. Figure 3 shows the Mode A configuration.

Mode B (Mixed LVTTL/TTL)

In Mode B, the 54SX16P device accepts LVTTL/TTL signals on all inputs, and the outputs can drive any LVTTL/TTL devices. The V_{CCA} and V_{CCI} pins must be supplied with 3.3V, while the V_{CCR} pin must be supplied with 5V. This mode is intended for mixed LVTTL/TTL systems. Figure 4 shows the Mode B configuration.

Mode C (5V PCI/ TTL)

In Mode C, the 54SX16P device accepts 5V PCI/LVTTL/TTL signals on all inputs, and the outputs can drive any 5V PCI/TTL devices. The V_{CCA} pins must be supplied with 3.3V, while the V_{CCI} and V_{CCR} must be supplied with 5V. This mode is intended for 5V PCI and TTL systems. The output can be driven up to 5V. Figure 5 shows the Mode C configuration.

Table 5 • *54SX16P Operating Mode*

Modes	Description	V_{CCA}	V_{CCI}	V_{CCR}	Input Voltage Tolerance	Output Voltage (Max)
A	3.3V PCI/LVTTL	3.3V	3.3V	3.3V	3.3V	3.3V
B	MixedLVTTL/TTL	3.3V	3.3V	5V	5V	3.3V
C	5V PCI/TTL	3.3V	5V	5V	5V	5V

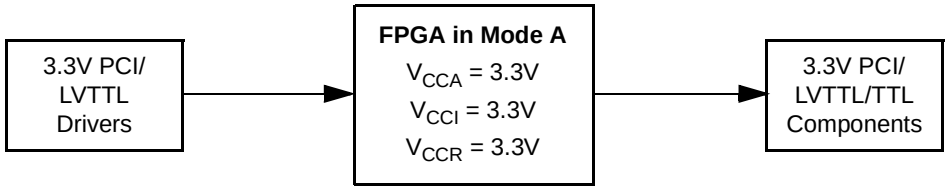

Figure 3 • *Mode A Configuration*

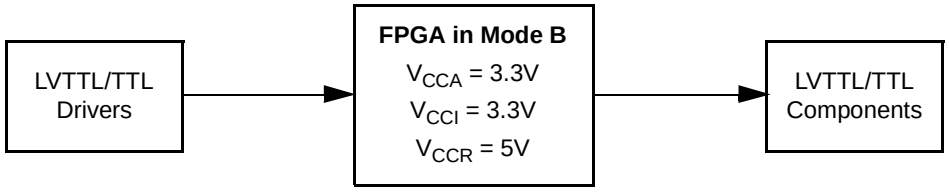

Figure 4 • *Mode B Configuration*

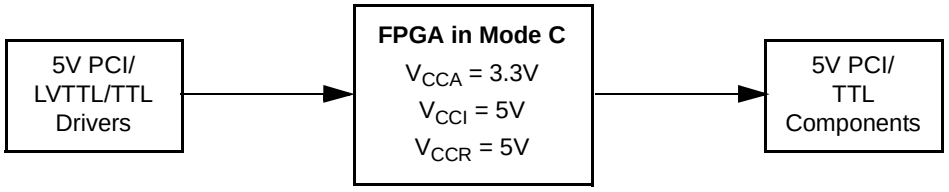

Figure 5 • *Mode C Configuration*

Two-way Mixed-Voltage Interfacing

The 54SX08, 54SX16, and 54SX32 are designed with an N-channel pull-up through the I/Os. The circuit design is shown in Figure 6. Additionally, the 54SX16P flexible I/Os are designed with a P-channel pull up, as shown in Figure 7. These I/Os can be driven to either 3.3V or 5V to support two-way mixed-voltage interfacing.

The order in which the power supplies are ramped up and ramped down is critical for all SX devices. To avoid device damage, V_{CCR} must be greater than or equal to V_{CCI} at all times. This guideline applies to both power-up and power-down sequences. A p-n junction exists between the V_{CCI} and V_{CCR} power supplies in the circuitry of the JTAG TDI and TMS pins. When V_{CCI} is greater than V_{CCR} by 0.6V, the p-n junction will forward bias and cause excessive current flow. The excessive current through the p-n junction may damage the TDI and TMS pin circuitry. For more information about power-up and power-down of SX devices, refer to the "Power-up and Power-Down Behavior of SX and RT54SX Devices" Application Note.

Conclusion

Most systems currently use 5V and 3.3V devices. To support this design trend, new devices must support two-way mixed-voltage interfacing. Actel offers a solution with its SX family of FPGAs.

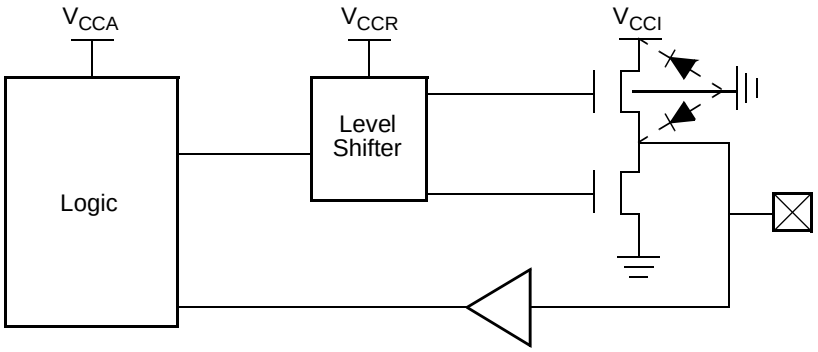

Figure 6 • *SX I/Os with N-channel Pull-up*

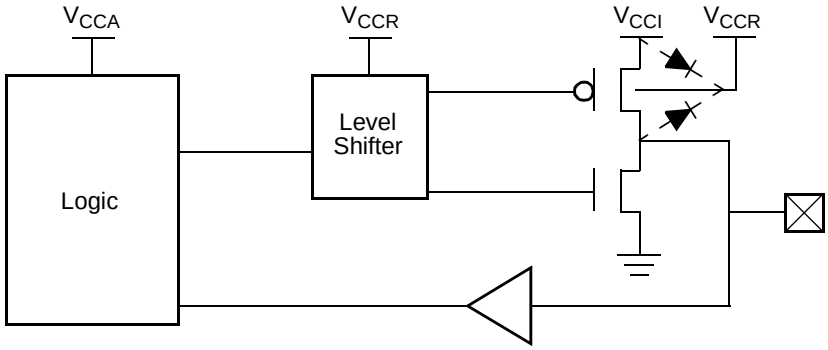

Figure 7 • *SX I/Os with P-channel Pull-up*

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