AC263

Application Note

Simultaneous Switching Noise and Signal Integrity

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Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 3.0

Revision 3.0 was published in January 2018. In revision 3.0 of the document, SSO guidelines and standards for MSIO, MSIOD, DDRIO and pushout delays for RT4G150-CG1657-ES and RT4G150-LG1657-PROTO Devices, are added . For more information, see all the tables from Table 3 (see page 10) to Table 16 (see page 23).

1.2 Revision 2.0

Revision 2.0 was published in June 2006. The following is a summary of changes done in revision 2.0 of the document:

- ProASIC^{PLUS} information was removed from this application note. For SSN ProASIC^{PLUS} information, refer to the ProASIC^{PLUS} SSO and Pin Placement Guidelines application note.
- Axcelerator and RTAX-S information is new.
- Table 1 (see page 9)was updated with Axceleator and RTAX-S data.
- Table 2 (see page 9) was updated with MX data.

1.3 Revision 1.0

Revision 1.0 was published in December 2015. It was the first publication of this document.

2 Simultaneous Switching Noise and Signal Integrity

2.1 Simultaneous Switching Noise and Signal Integrity

Ground bounce and V_{CC} bounce have always been present in digital circuits. However, in the past they were not always noticeable because of slow edge rates and low pin count. Any designer working with high-edge-rate devices must be aware of these noise issues and will need to address them.

2.1.1 Simultaneous Switching Noise

The following section describes the details of simultaneous switching noise.

2.1.2 GND Bounce and V cc Bounce

When multiple output drivers switch simultaneously, they induce a voltage drop in the chip/package power distribution. The simultaneous switching momentarily raises the ground voltage within the device relative to the system ground. This apparent shift in the ground potential to a non-zero value is known as simultaneous switching noise (SSN) or, more commonly, ground bounce. The ground bounce voltage is related to the inductance present between the device ground and the system ground, and the amount of current sunk by each output. It is given by the following equation.

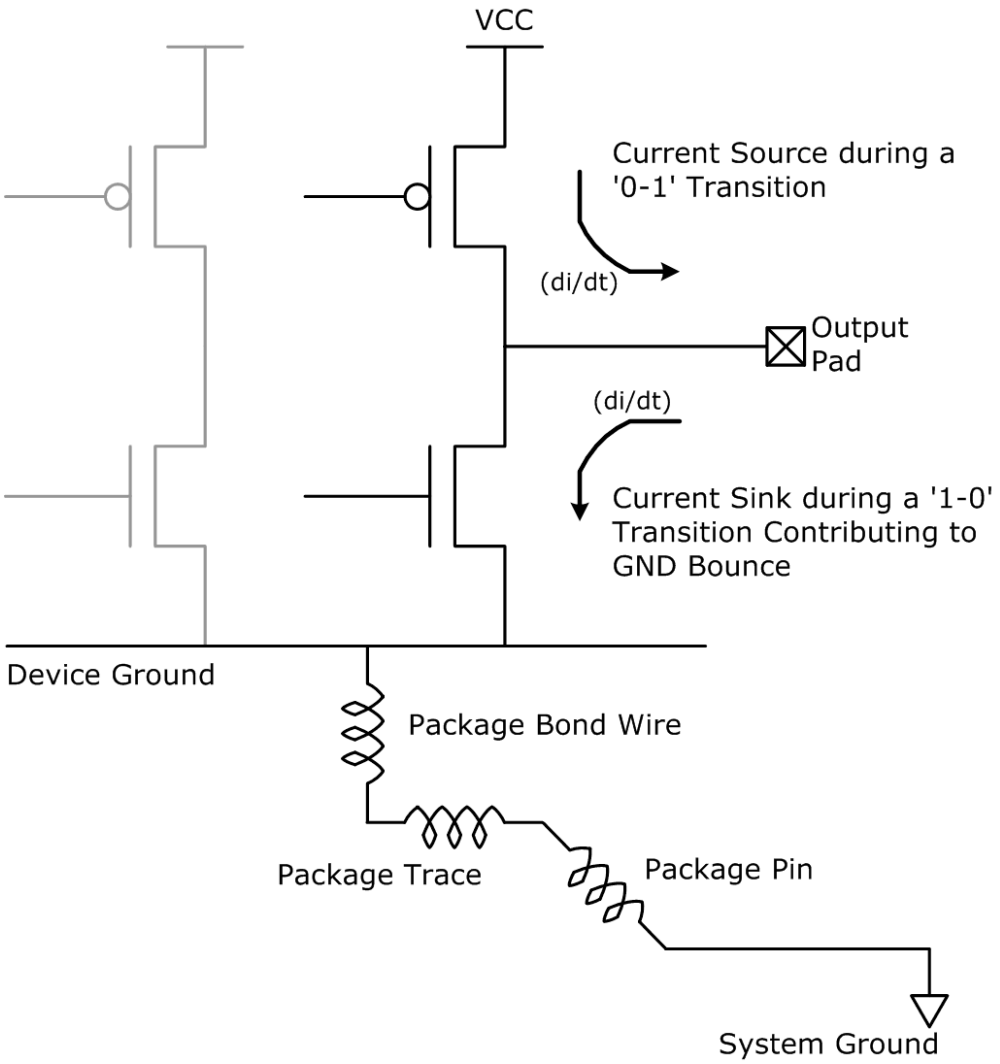
$V = L \times di/dt$

An I/O switching from high to low or low to high is actually discharging or charging the capacitor that loads the I/O. The resulting value of di/dt is cumulative and increases with the number of simultaneously switching outputs (SSOs). Therefore, the higher di/dt, the higher the ground bounce amplitude.

The device ground is connected to the system ground (PCB ground) through a series of inductors, comprised of package bond wire, package trace, and board inductance as shown in the following figure.

$L_{eff} = L_{bondwire} + L_{trace} + L_{pin}$

Figure 1 • A Sample Switching Output Buffer Showing Parasitic Inductance



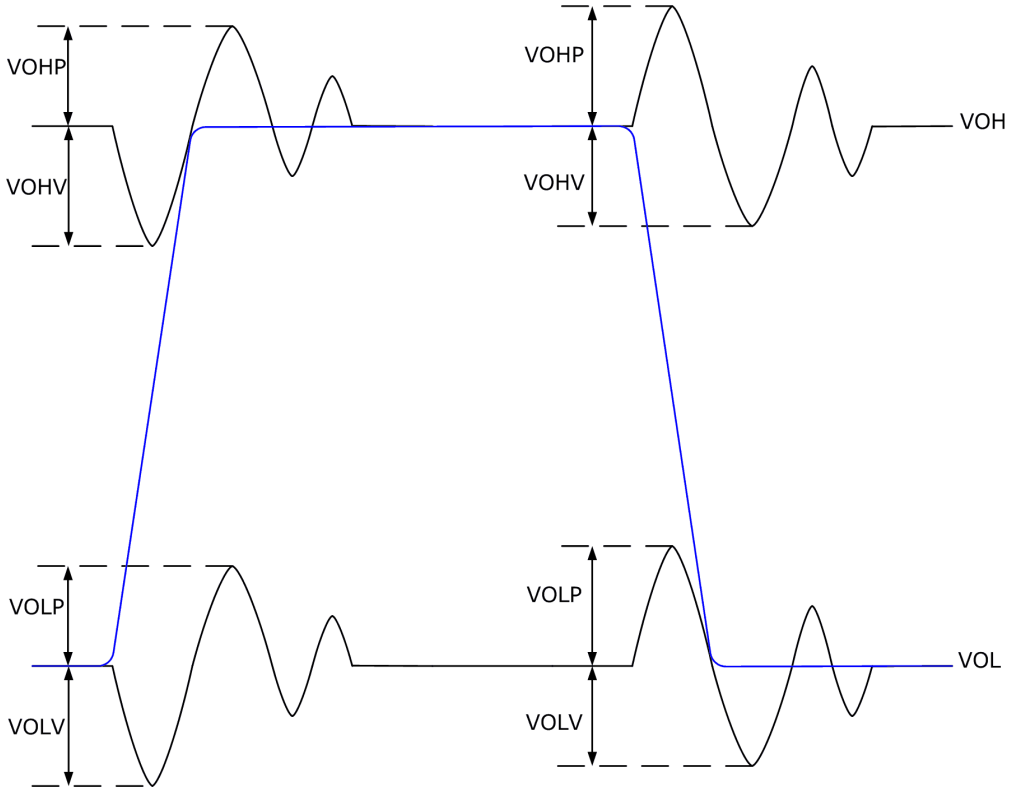
As a result, the higher L_{eff}, the higher the amplitude will be. Problems may arise when this ground bounce gets transferred to the outside through output buffers driving low. If the bounce is higher than the V_{IL} threshold of the input being driven, there is a possibility that the glitch will be recognized as a legal logic '1'. The same phenomenon applies to V_{CC} and is called V_{CC} bounce. Both ground bounce and V_{CC} bounce are important noise parameters, but devices usually tend to have more noise margin near the high level ('1') than near the low level ('0'). Therefore, ground bounce is considered more often.

2.1.2.1 Various GND Bounce Parameters

The amplitude of a glitch or bounce dies with time. Depending on the direction of the switching edge, the first pulse of the glitch can be either positive or negative. There are a few parameters usually associated with SSN.

They are V_{OLP} (peak) and V_{OLV} (valley) for ground bounce and V_{OHP} (peak) and V_{OHV} (valley) for V_{CC} bounce as shown in the following figure.

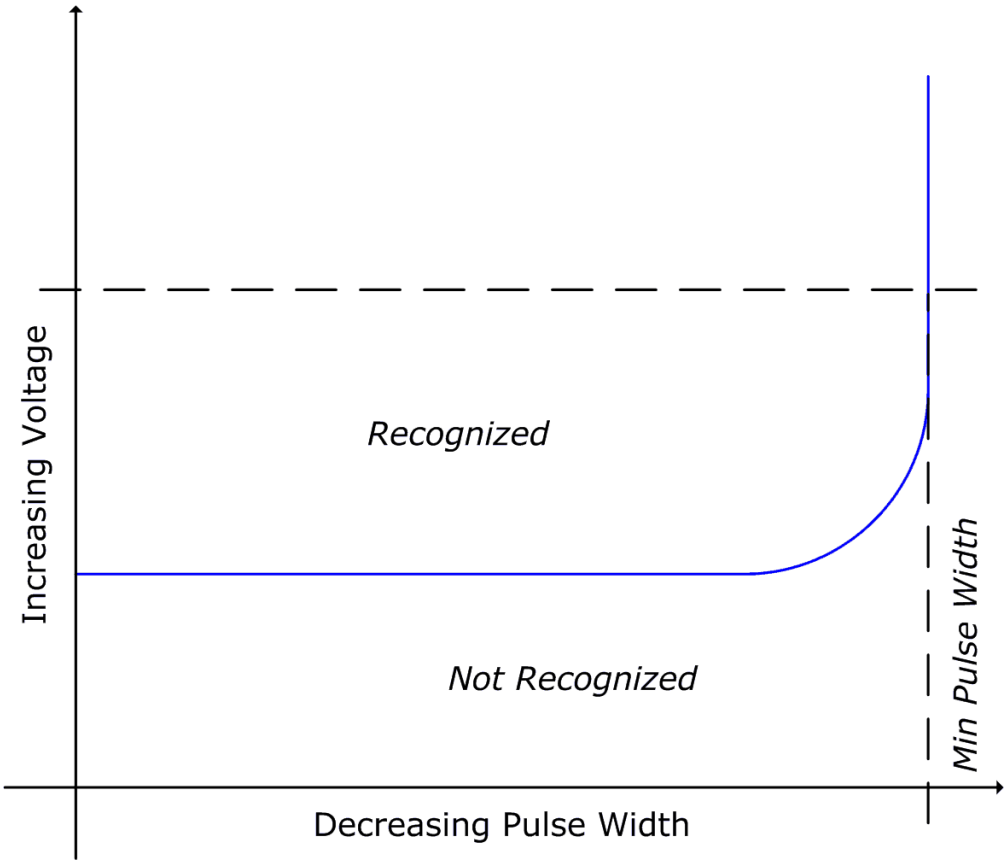
Figure 2 • Ground-Bounce Parameters



Another parameter to look at is the width of the pulse. The pulse width, or the settling time of the bounce, is the time for which the signals stay over a given threshold criterion. Since the waveform of a ground bounce pulse looks more like a sinusoid than a square wave, the width of the pulse depends on the point of measurement. This parameter is important because every input buffer has a limit on the smallest pulse that it can recognize with regard to width and amplitude. Any pulse smaller than this is not recognized, even though the amplitude might be much higher as shown in the following figure. For example, an input buffer with a minimum recognizable pulse width of 3 ns at 2.0 V will not recognize a pulse that is 1 ns wide, even if its amplitude is 2.5 V.

Therefore, with regard to noise, the pulse width and voltage amplitude of the glitch need to be minimized so it is not interpreted as a logic pulse by the input buffer of the receiving device.

Figure 3 • Voltage Vs Pulse Width Plot of an Input Buffer



2.2 Factors Influencing SSN

Microsemi SoC Products Group has performed a number of SSN experiments to understand the likelihood of SSN affecting device performance. The following information is based on real test data taken from Microsemi SX-A and RTSX-SU FPGAs.

Since the device ground is within the package, it is hard to measure the actual internal ground bounce. The most common way to measure ground bounce is to configure an output to drive low (or high for V_{CC} bounce) and observe it using an oscilloscope. In-house measurements and validation were done with reference to MIL-STD-883. The device being tested was soldered onto a custom board. High-bandwidth oscilloscopes, upwards of 1 G samples per second, were used for this purpose. Typical conditions were used in making all measurements. According to the specification, all switching outputs (including the quiescent output) were loaded with a 50 Ω resistor to ground in parallel with a 50 pF capacitor.

2.2.1 Effect of Changing Capacitive Load on GND Bounce

Varying the capacitive load had an effect on both the amplitude and the width of the pulse. The amplitude tended to decrease with increasing capacitive load, whereas the pulse width increased. The increased capacitive load tends to reduce the slew rate on the outputs, thereby reducing the amplitude. However, as previously seen, the pulse width needs to be considered in combination with the absolute amplitude.

2.2.2 Effect of Output Slew Rate on GND Bounce

The slew rate (dv/dt) of the output can affect ground bounce more than any other parameter. The slower the output slew, the lower the ground bounce will be. This becomes a trade-off between performance and signal integrity. However, the frequency of the output does not affect ground bounce. The following figure shows the falling edge of a reference output (purple) in the high slew configuration, which is about 1.5 V/ns, and a ground bounce pulse (green) of about 400 mV. The plot in the following figure shows a ground bounce (green) of about 100 mV (note the change in scale).

The only difference between this and the previous data is the output slew rate, which is less than 0.75 V /ns. This shows a 75% improvement when compared to high slew.

Figure 4 • Ground-Bounce Plot with a High Slew Output Reference

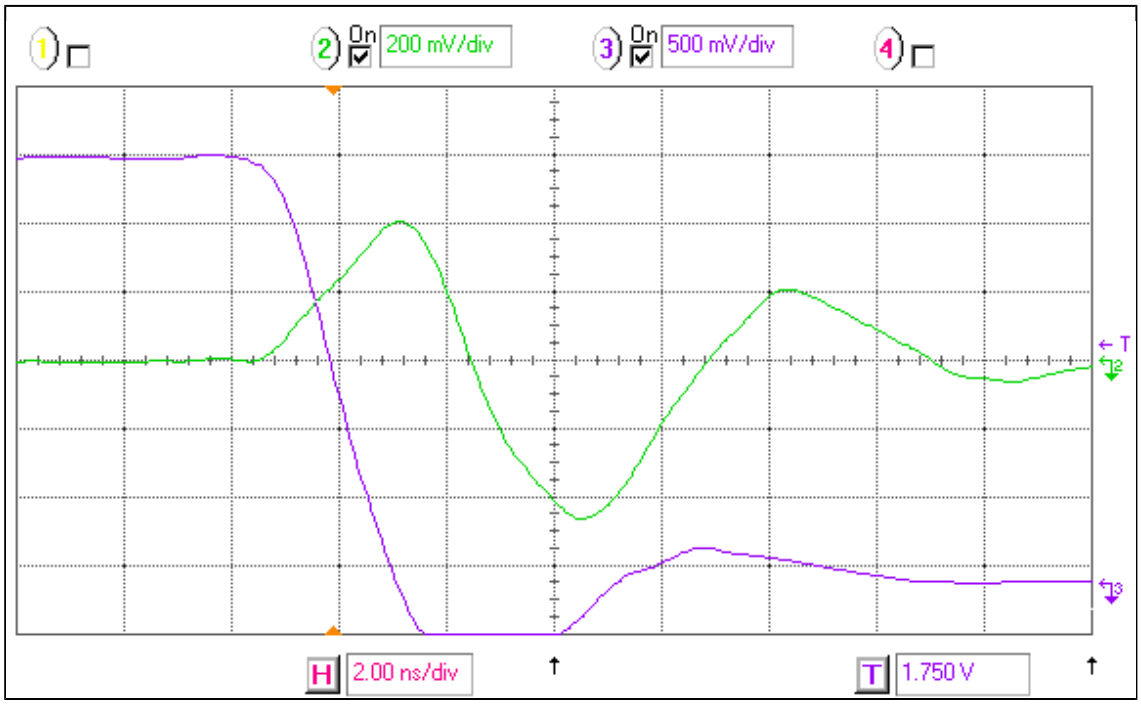
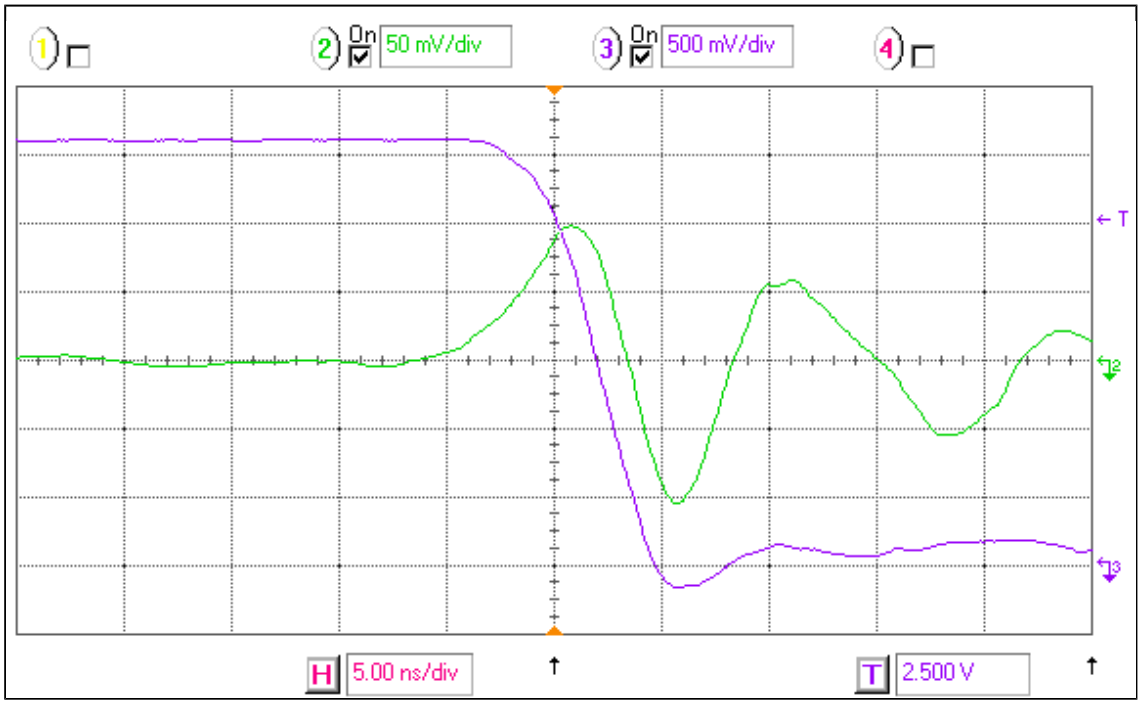


Figure 5 • Ground-Bounce Plot with a Low Slew Output Reference



2.3 Avoiding SSN Problems

SSN problems may be reduced or completely avoided by including SSOs as a design parameter from the early stages of system design. Since an FPGA is a programmable device, the I/O configuration parameters, such as voltage compliance and slew rate, are not selected until the FPGA I/O buffers are configured and programmed. This gives the designer a lot of flexibility in making design adjustments to solve system-level signal integrity issues, such as ground bounce and V_{CC} bounce. The following are a few recommendations that save time and effort:

- Identify potential SSOs and spread them around the package.
- Avoid placement of asynchronous pins (resets, enables, etc.) near SSOs.
- Place SSOs away from clock pins/traces.
- Decouple V_{CC}/GND pairs to filter out noise.
- When possible, use low slew outputs.
- Low pass filters can be used to meter out the glitches at the PCB level.
- Whenever possible, create synchronous designs that are glitch tolerant.
- Because they have better noise margin, use 5 V CMOS–compliant inputs when possible.
- Increased capacitive load decreases the amplitude of the ground bounce by reducing the output slew rate.
  The switching outputs can be made to switch in a staggered fashion by inserting delays in the design so switching is not simultaneous. This can be achieved by inserting the Microsemi macro BUFD to force buffer delays. Even if the system layout is fixed, this method can help reduce SSN, as no board changes are necessary.

2.4 Recommendations for Microsemi Devices

Microsemi defines SSOs as any outputs that transition in phase within a 1 ns window. The measurements made by Microsemi are based on the following worst-case conditions:

1. The switching outputs are adjacent to the quiet output on either side.
2. All unused I/O buffers are tristated so they do not help either ground or V_{CC}.
3. A worst-case package was used.

The following table gives the recommendations for Microsemi devices under typical conditions. The recommendations give the number of adjacent I/Os that can be switched simultaneously around an I/O required to be quiet. For legacy products, refer to Table 2 (see page 9) . For SSO recommendations on ProASIC3/E and ProASICPLUS®, refer to the family-specific application notes.

Table 1 • SSOs around a Quiet Output for SX-A, RTSX-SU, Axcelerator, RTAX-S, and ProASIC Devices

Device and I/O Supply Voltage	SSOs	
	At High Slew	At Low Slew
RTAX-S (2.5 V / 3.3 V)[1]	40[2]	Unrestricted[2]
Axcelerator (2.5 V / 3.3 V)	40[2]	Unrestricted[2]
SX-A/RTSX-SU 5.0 V	24[3]	> 40[3]
SX-A/RTSX-SU 3.3 V	32[2]	> 40[2]
ProASIC 3.3 V	32[2]	> 40[2]

Note:

1. *Applies to RTAX2000S and smallerdevices.*
2. *Theobservedgroundbounceislessthan1.25Vwithapulsewidthoflessthan2.0ns.*
3. *The observed ground bounce is less than 1.5 V with a pulse width of less than 2.0 ns.*

Table 2 • Recommended SSO Limits for Microsemi Legacy FPGAs

Device	Package	Maximum Recommended SSOs for Loads		
		20 pF	35 pF	50 pF
42MX (5 V)	PQ160	–	–	10[1]
42MX (3.3 V)	PQ160	–	–	75
40MX (5 V)	PQ160	–	–	29[2]
40MX (3.3 V)	PQ160	–	–	56
A1010A/A1020A	44 PLCC	40	22	16
A1010A/1020A	68 PLCC	60	34	24
A1020A	84 PLCC	80	45	32
A1010A/1020A	84 PGA	80	45	32
A1010A/A1020A	100 PQFP	80	45	32
A1280/A1280XL	PG176, PQ160	160	90	64
A1240/A1240XL	PG132, PQ144	120	68	48
A1240/A1225/A1225XL	84 PLCC	80	45	32
A1225/A1225XL	100 PGA, PQFP	80	45	32
A1400 family[3]	84 PLCC	64	48	42
A1400 family[3]	All other packages	128	64	58

Note:

1. *If one or more pins exist between the SSOs and quiet output, the recommendation increases to 100.*
2. If one or more pins exist between the SSOs and quiet output, the recommendation increases to 46.
3. The recommended SSO value for the A1400 family can be doubled for outputs using low slew drivers.

The following table lists the MSIO SSO guidelines and standards when SSO load for MSIO is 500 Ω in parallel with 50 pF load, at a pulse width of 1 ns for RT4G150-CG1657-ES devices.

Table 3 • MSIO SSO Guidelines at 1 ns Pulse Width for RT4G150-CG1657-ES Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVTTL	**20**	76	76
	16	76	76
	12	76	76
	8	76	76
	4	76	76
	2	76	76
LVCMOS25	**16**	76	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**12**	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**8**	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS12	8	76	76
	6	76	76
	4	76	76
	2	76	76

The following table lists the MSIO SSO guidelines and standards when SSO load for MSIO is 500 Ω in parallel with 50 pF load, at a pulse width of 0 ns for RT4G150-CG1657-ES devices.

Table 4 • MSIO SSO Guidelines at 0 ns Pulse Width for RT4G150-CG1657-ES Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVTTL	**20**	76	76
	16	76	76
	12	76	76
	8	76	76
	4	76	76
	2	76	76
LVCMOS25	**16**	76	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**12**	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**8**	7 6	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS12	**8**	76	76
	6	76	76
	4	76	76
	2	76	76

The following table lists the MSIOD SSO guidelines and standards when SSO load for MSIOD is 500 Ω in parallel with 50 pF load, at a pulse width of 1 ns for RT4G150-CG1657-ES devices.

Table 5 • MSIOD SSO Guidelines at 1 nS Pulse Width for RT4G150-CG1657-ES Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**12**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**10**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**8**	76	76
	6	76	76
	4	76	76
	2	76	7 6
LVCMOS12	**4**	76	76
	2	76	76

The following table lists the MSIOD SSO guidelines and standards when SSO load for MSIOD is 500 Ω in parallel with 50 pF load at a pulse width of 0 ns for RT4G150-CG1657-ES devices.

Table 6 • MSIOD SSO Guidelines at 0 nS Pulse Width for RT4G150-CG1657-ES Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**12**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**10**	76	76
	8	76	76
	6	76	76
	4	7 6	76
	2	76	76
LVCMOS15	**8**	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS12	**4**	76	76
	2	76	76

The following table lists the DDRIO SSO guidelines and standards when trace load for DDRIO is 17 pF, at a pulse width of 1 ns for RT4G150-CG1657-ES devices.

Table 7 • DDRIO SSO Guidelines at 1 nS Pulse Width for RT4G150-CG1657-ES Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**16**	16	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**16**	76	76
	12	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**12**	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS12	**8**	76	76
	4	76	76
	2	76	76

The following table lists the DDRIO SSO guidelines and standards when trace load for DDRIO is 17 pF, at a pulse width of 0 ns for RT4G150-CG1657-ES devices.

Table 8 • DDRIO SSO Guidelines at 0 nS Pulse Width for RT4G150-CG1657-ES Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**16**	16	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**16**	76	76
	12	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**12**	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS12	**8**	76	76
	4	76	76
	2	76	76

The following table lists the MSIO SSO guidelines and standards when SSO load for MSIO is 500 Ω, in parallel with 50 pF load, at a pulse width of 1 ns, for RT4G150-LG1657-PROTO devices.

Table 9 • MSIO SSO Guidelines at 1 ns Pulse Width for RT4G150-LG1657-PROTO Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVTTL	**16**	76	76
	12	76	76
	8	76	76
	4	76	76
	2	76	76
LVCMOS25	**14**	76	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**12**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**8**	76	76
	6	7 6	76
	4	76	76
	2	76	76
LVCMOS12	**4**	76	76
	2	76	76

The following table lists the MSIO SSO guidelines and standards when SSO load for MSIO is 500 Ω, in parallel with 50 pF load, at a pulse width of 0 ns, for RT4G150-LG1657-PROTO devices.

Table 10 • MSIO SSO Guidelines at 0 ns Pulse Width for RT4G150-LG1657-PROTO Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVTTL	**16**	76	76
	12	76	76
	8	76	76
	4	76	76
	2	76	76
LVCMOS25	**14**	76	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**12**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**8**	76	76
	6	7 6	76
	4	76	76
	2	76	76
LVCMOS12	**4**	76	76
	2	76	76

The following table lists the MSIOD SSO guidelines and standards when SSO load for MSIOD is 500 Ω, in parallel with 50 pF load, at a pulse width of 1 ns, for RT4G150-LG1657-PROTO devices.

Table 11 • MSIOD SSO Guidelines at 1 nS Pulse Width for RT4G150-LG1657-PROTO Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**10**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**8**	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**6**	76	76
	4	76	76
	2	76	76
LVCMOS12	**4**	76	76
	2	76	76

The following table lists the MSIOD SSO guidelines and standards when SSO load for MSIOD is 500 Ω, in parallel with 50 pF load, at 0 ns pulse width, for RT4G150-LG1657-PROTO devices.

Table 12 • MSIOD SSO Guidelines at 0 nS Pulse Width for RT4G150-LG1657-PROTO Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**10**	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**8**	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**6**	76	76
	4	76	76
	2	76	76
LVCMOS12	**4**	76	76
	2	76	76

The following table lists the DDRIO SSO guidelines and standards when trace load for DDRIO is 17 pF, at a pulse width of 1 ns, for RT4G150-LG1657-PROTO devices.

Table 13 • DDRIO SSO Guidelines at 1 nS Pulse Width for RT4G150-LG1657-PROTO Devices

IO Standards	Drive Strength(mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**16**	16	76
	12	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS18	**16**	76	76
	12	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**12**	76	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	7 6	76
LVCMOS12	**8**	76	76
	4	76	76
	2	76	76

The following table lists the DDRIO SSO guidelines and standards when trace load for DDRIO is 17 pF, at a pulse width of 0 ns, for RT4G150-LG1657-PROTO devices.

Table 14 • DDRIO SSO Guidelines at 0 nS Pulse Width for RT4G150-LG1657-PROTO Devices

IO Standards	Drive Strength (mA)	SSOs Causing GND Bounce	SSOs Causing VDDI Bounce
LVCMOS25	**16**	6	56
	12	14	76
	8	24	76
	6	34	76
	4	76	76
	2	76	76
LVCMOS18	**16**	16	76
	12	24	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	76	76
LVCMOS15	**12**	22	76
	10	76	76
	8	76	76
	6	76	76
	4	76	76
	2	7 6	76
LVCMOS12	**6**	76	76
	4	76	76
	2	76	76

The following table lists the pushout delays for MSIO, MSIOD, when SSO load is 500 Ω, in parallel with 50pF load and for DDRIO, when trace load is 17pF, in RT4G150-CG1657-ES devices.

Table 15 • PushOut Delays in RT4G150-CG1657-ES Devices

IO Standards	MSIO		MSIOD		DDRIO	
	IO Drive Strength (mA)	Maximum Push Out Delay Measured (ns)	IO Drive Strength (mA)	Maximum Push Out Delay Measured (ns)	IO Drive strength (mA)	Maximum Push Out Delay Measured (ns)
LVTTL[1]	20	0.21	–	–	–	–
LVCMOS25	16	0.197	12	0.172	16	0.121
LVCMOS18	12	0.244	10	0.175	16	0.143
LVCMOS15	8	0.294	6	0.192	12	0.16
LVCMOS12	4	0.785	4	0.226	8	0.157

Note:

1. MSIOD and DDRIO models do not support LVTTL I/O standard.

The following table lists the pushout delays for MSIO, MSIOD, when SSO load is 500 Ω, in parallel with 50pF load and for DDRIO, when trace load is 17pF, in RT4G150-LG1657-PROTO devices.

Table 16 • PushOut Delays in RT4G150-CG1657-ES Devices

IO Standards	MSIO		MSIOD		DDRIO	
	IO Drive Strength (mA)	Maximum Push Out Delay Measured (ns)	IO Drive Strength (mA)	Maximum Push Out Delay Measured (ns)	IO Drive Strength (mA)	Maximum Push Out Delay Measured (ns)
LVTTL[1]	16	0.101	–	–	–	–
LVTTL[1]	4	0.121	–	–	–	–
LVCMOS25	16	0.146	10	0.128	16	0.152
LVCMOS25	–	–	4	0.153	–	–
LVCMOS18	12	0.189	8	0.141	16	0.158
LVCMOS18	–	–	2	0.164	–	–
LVCMOS15	8	0.226	6	0.148	12	0.153
LVCMOS15	–	–	2	0.155	–	–
LVCMOS12	4	0.276	4	0.185	6	0.169

Note:

1. MSIOD and DDRIO models do not support LVTTL I/O standard.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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