

# SPI Flash Emulation for Fusion Devices Design Example

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## General Description

As the world's first mixed-signal programmable logic family, Microsemi's Fusion® FPGAs integrate mixed-signal analog, flash memory (eNVM), and FPGA fabric in a monolithic device. Fusion devices enable designers to quickly move from concept to completed design and deliver feature-rich systems to market. Fusion devices have 256 kbyte eNVM blocks:

- The small devices, AFS090 and AFS250, have one eNVM block
- The medium size device, AFS600, has two eNVM blocks
- The biggest device in the family, AFS1500, has four eNVM blocks.

Except for AFS090, the read and write bus width for all devices is 32. The read and write bus width for AFS090 is 16. Refer to the Fusion handbook for additional information.

([www.actel.com/documents/Fusion\\_HB.pdf](http://www.actel.com/documents/Fusion_HB.pdf)).

This design example emulates SPI flash in a Fusion device by adding an SPI interface to eNVM. Users can use this design to remove an external SPI flash and integrate it within a Fusion device, which will reduce cost and board space.

Figure 1 describes the architecture of the SPI flash emulated in a Fusion device.

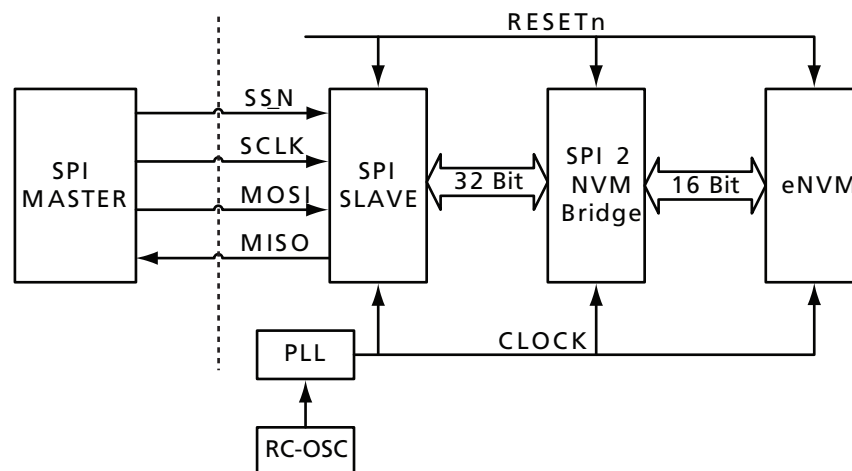


Figure 1 • Block Diagram

The block diagram (Figure 1) shows an SPI Slave, SPI 2 NVM bridge, and eNVM interfaced to emulate SPI flash device.

Files for this design example can be downloaded from the Microsemi website:

[http://soc.microsemi.com/download/rsc/?f=SPIFlash\\_Emulation\\_Fusion\\_DF](http://soc.microsemi.com/download/rsc/?f=SPIFlash_Emulation_Fusion_DF)

The design files included are compliant with Verilog 2001:

Spi\_s.v – This is the 32-bit SPI slave.

Spi\_Nvm\_Bridge\_32bit.v – This is the 32-bit SPI to 32-bit eNVM bridge.

Spi\_Nvm\_Bridge\_16bit.v – This is the 32-bit SPI to 16-bit eNVM bridge.

SPINVM.v – This is the top level for the design that interconnects the two blocks and the 32-bit/16-bit eNVM bridge, based on the MODE\_32B\_16B parameter setting.

## CFI Commands Supported

A subset of the CFI type commands are supported in this design example (Table 1).

**Table 1 • Supported CFI Commands**

Instruction	Description	Instruction Code (1 Byte)		Address Bytes	Dummy Bytes	Data Bytes
WREN	Write enable	0000 0110	0x06	0	3	0
RDID	Read identification	1001 1111	0x9F	0	3	4
RDSR	Read status register	0000 0101	0x05	0	3	4
FAST_READ	Read data words	0000 1011	0x0B	3	4	1 to $\infty$
PP	Page program	0000 0010	0x02	3	0	128

*Note:* All commands are limited to a word (4 bytes). The page program expects 1 page, 32 words.

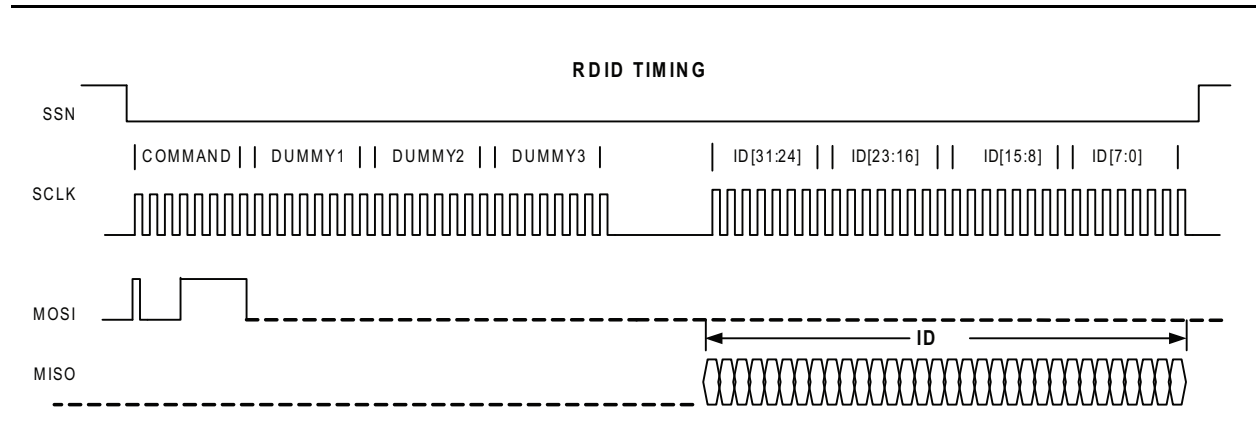
## Functional Description

Once slave select is asserted, the SPI slave monitors the serial line MOSI input signal for incoming data. After 32 bits have been received (32 pulses of SCLK corresponding to one word of data), the data is synchronized with the backend clock and presented to the SPI2NVM bridge on RCD\_DATA. The SPI slave asserts the RCD\_DATA\_VALID signal to indicate to SPI2NVM bridge that it has valid data. SPIN2NVM takes the 32 bits of data and decodes it to determine whether data or the commands are valid.

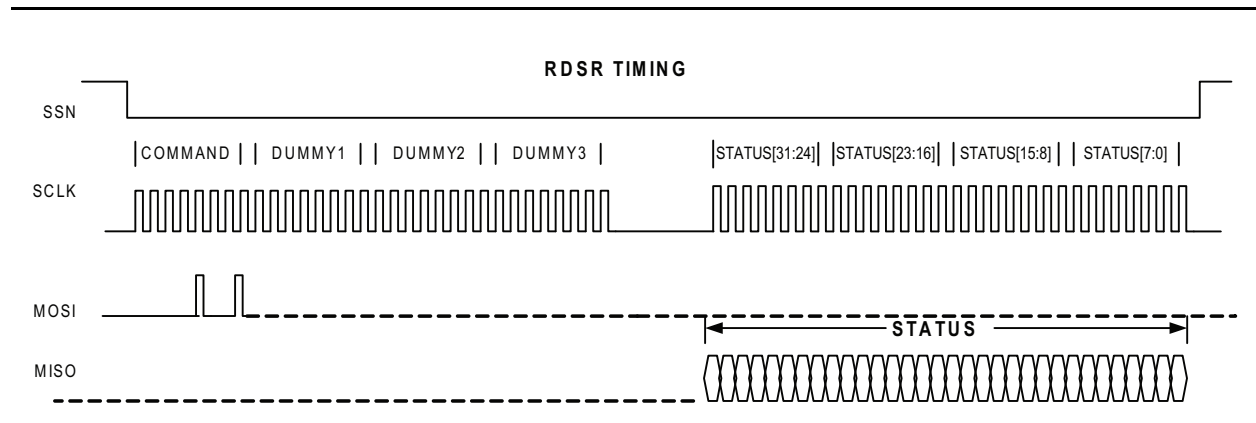
Once the data received is validated, the bridge services the command as appropriate. The bridge takes care of the word to half-word translation between SPI and eNVM. The sequence of operation for each of the supported commands is described below:

- **RDID or RDSR:** When either of these two commands (which do not require eNVM access) is received and SPI slave is ready to accept, as indicated by READY\_TO\_SEND, the bridge

presents the appropriate data on the TX\_DATA bus. Once the data is placed on the bus, the bridge asserts TX\_DATA\_VALID for SPI to start transmission (MISO).

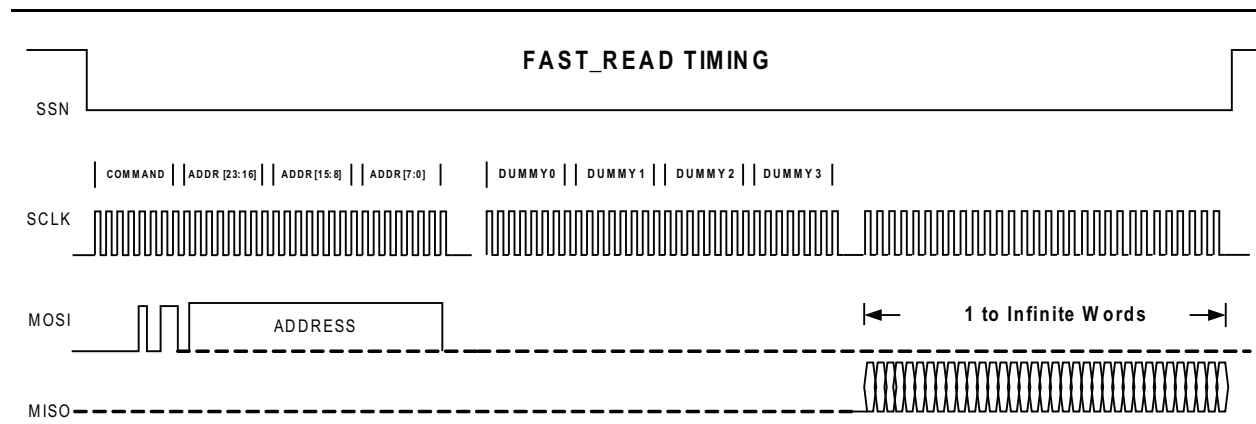


**Figure 2 • RDID Timing**



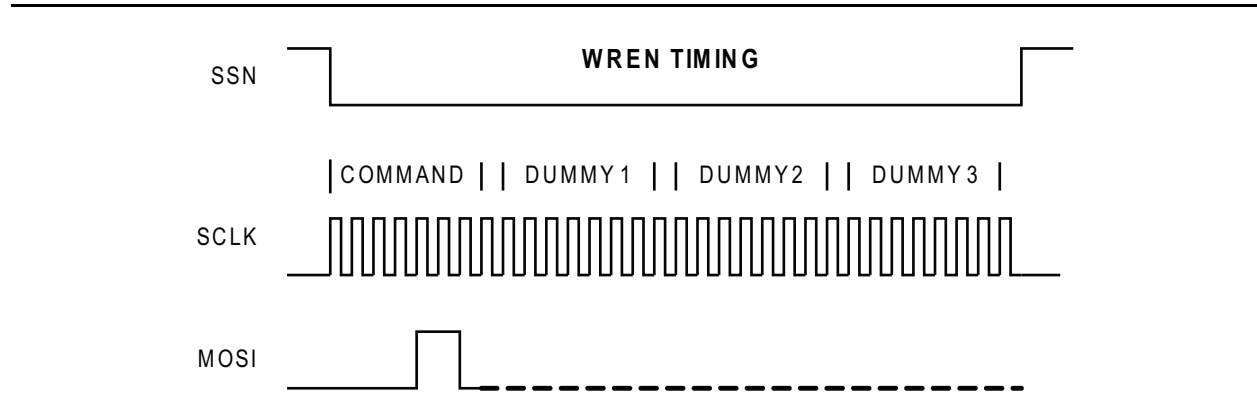
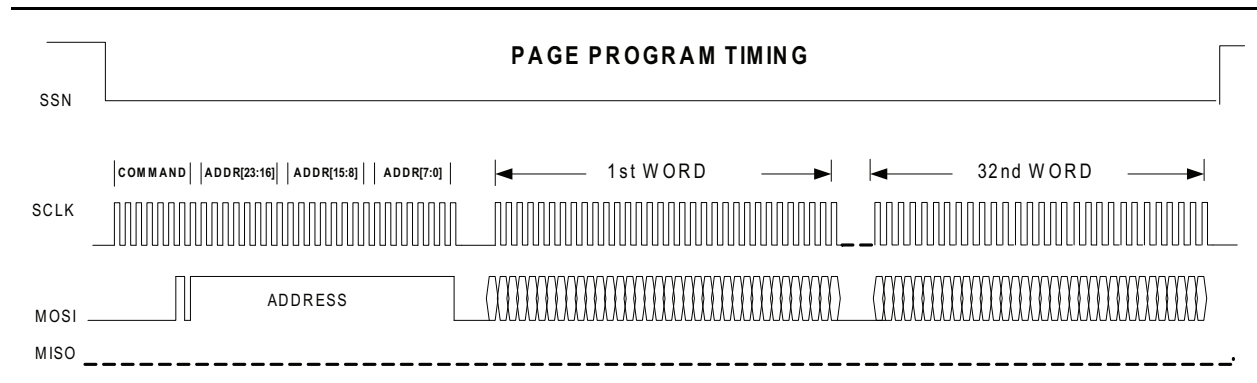
**Figure 3 • RDSR Timing**

- FAST\_READ:** When this command is received and SPI slave is ready to accept, as indicated by READY\_TO\_SEND, the bridge starts reading from the eNVM array at the address specified and presents data on the TX\_DATA bus. Once data is placed on the bus, the bridge asserts TX\_DATA\_VALID for SPI to start transmission (MISO). The address is auto-incremented and read operation continues until it is terminated (TERMINATE\_READ is asserted).



**Figure 4 • Fast\_Read Timing**

- PP:** This command must be preceded by the command WREN to be considered legal. After WREN, PP expects exactly 32 words (128 bytes, which equals the page size in eNVM). Each word received is written to the page buffer and the page is programmed into the flash array. If less than 32 words are received the, design keeps waiting. If more than 32 words are received, words above 32 are discarded.


**Figure 5 • WREN Timing**

**Figure 6 • Page Program Timing**

# Interface Details

## SPI Slave

In order to optimize utilization, this design uses a custom SPI slave with 32-bit SPI operation and clock synchronization between the SPI clock and backend clock (Figure 7).

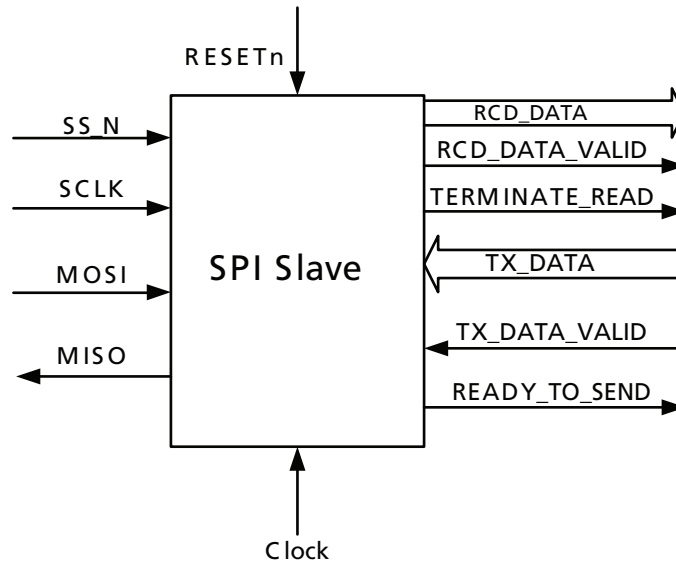


Figure 7 • SPI the Slave Block

Signals are described in Table 2.

Table 2 • Signal Descriptions

Signal Name	Description	Width	Direction	Polarity
<b>Globals</b>				
CLOCK	Input clock to the block. This clock is used by the SPI backend.	1	Input	N/A
RESETn	Active Low-reset to the block	1	Input	Active Low
<b>Serial Interface</b>				
SCLK	Slave clock (comes from master)	1	Input	N/A
SS_N	Slave select (comes from master)	1	Input	Active Low
MOSI	Serial data input (comes from master)	1	Input	N/A
MISO	Serial data output (goes to master)	1	Output	N/A

**Table 2 • Signal Descriptions (continued)**

Signal Name	Description	Width	Direction	Polarity
<b>Backend Signals</b>				
rcd_data	Data received from master (parallel data from MOSI)	32	Output	N/A
rcd_data_valid	Indication to backend that SPI has data available	1	Output	Active High
terminate_read	Indication of end of read operation (this is SS_N transferred to backend)	1	Output	Active Low
tx_data	Data to be sent to master (this goes on MISO)	32	Input	N/A
tx_data_valid	Indication from backend that it has data for transmission	1	Input	Active High
ready_to_send	Indication to back-end that SPI is ready to accept data for transmission	1	Output	Active High

## SPI2NVM Bridge

This block acts as a bridge between SPI and NVM. The SPI2NVM bridge block decodes CFI commands received, controls NVM for writing and reading, increments auto-address for read and write, and optionally translates between word (32 Bit) SPI, and half-word (16 Bit) for eNVM (AFS090) (when parameter MODE\_32B\_16B is set to 1).

**Note:** All other NVM inputs are tied to ground as they are not dynamically changed in this design. These signals (READNEXT, PAGESTATUS, ERASEPAGE, SPAREPAGE, AUXBLOCK, UNPROTECTPAGE, OVERWRITEPAGE, DISCARDPAGE, OVERWRITEPROTECT, PAGELOSSPROTECT, PIPE, and LOCKREQUEST) are not shown in [Table 3](#) or [Figure 8](#) on [page 7](#).

**Table 3 • SPI2NVM Bridge Signal Description**

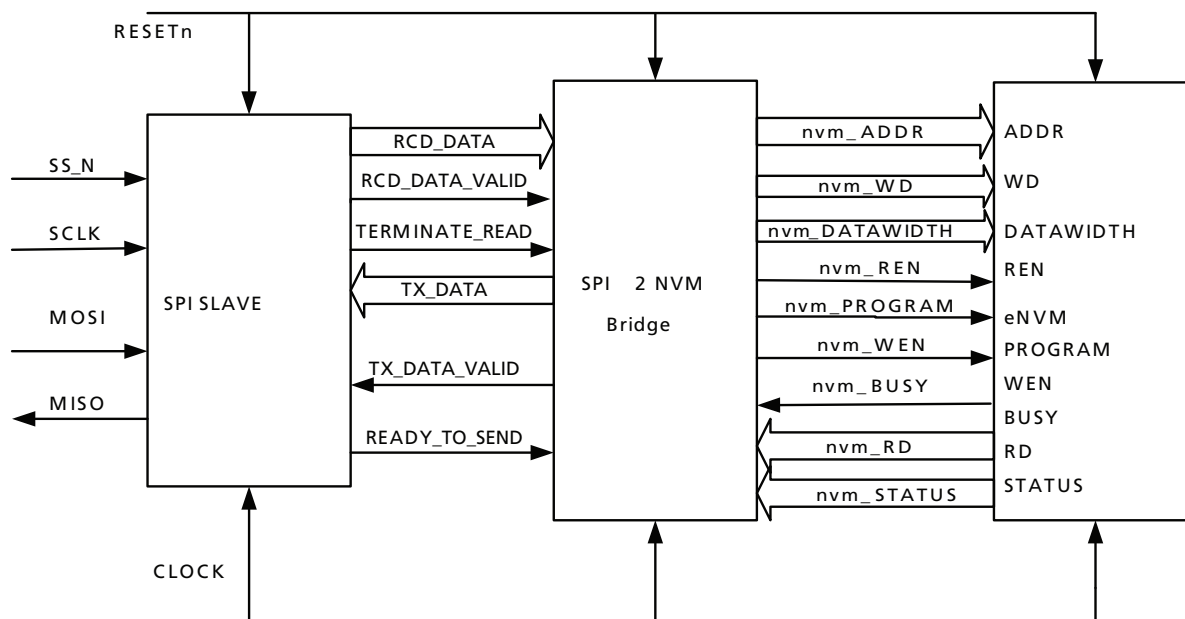
Signal Name	Description	Width	Direction	Polarity
<b>Globals</b>				
CLOCK	Input clock to the block. This clock is used by the SPI backend.	1	Input	N/A
RESETn	Active Low-reset to the block	1	Input	Active Low
<b>SPI Side</b>				
rcd_data	Received data from SPI slave (RCD_DATA of SPI slave)	32	Input	N/A
spi_data_valid	Received data from SPI slave (RCD_DATA_VALID of SPI slave)	1	Input	Active High
terminate_read	Indication of end of read operation (TERMINATE_READ of SPI Slave)	1	Input	Active Low
tx_data	Data to be sent to SPI slave (TX_DATA of SPI slave)	32	Output	N/A
tx_data_valid	Indication to SPI slave that data is ready (TX_DATA_VALID of SPI slave)	1	Output	Active High
ready_to_send	Indication from SPI slave that it is ready to accept data (READY_TO_SEND of SPI slave)	1	Output	Active High

**Table 3 • SPI2NVM Bridge Signal Description (continued)**

Signal Name	Description	Width	Direction	Polarity
<b>NVM Side</b>				
nvm_ADDR	Read/write address to NVM (ADDR of NVM)	18	Output	N/A
nvm_WD	Write data to NVM (WD of NVM)	32/16	Output	N/A
nvm_DATAWIDTH	Read/write access width. Set to 01 for 16 bits (DATAWIDTH of NVM).	2	Output	N/A
nvm_REN	Read enable to NVM (REN of NVM)	1	Output	Active High
nvm_WEN	Write enable to NVM (WEN of NVM)	1	Output	Active High
nvm_PROGRAM	Program input to NVM (PROGRAM of NVM)	1	Output	Active High
nvm_BUSY	Busy indication from NVM (BUSY of NVM)	1	Input	Active High
nvm_RD	Read data from NVM (RD of NVM)	32/16	Input	N/A
nvm_STATUS	Status of last operation from NVM (STATUS of NVM)	2	Input	N/A

*Note:* NVM\_WD and NVM\_RD are 16 bit when MODE\_32B\_16B parameter is set to 1.

Figure 8 shows the signal interconnection between the SPI slave and the SPI2NVM bridge.



**Figure 8 • SPI Slave and SPI2NVM Bridge Interconnection**

*Note:* The ratio of CLOCK (the clock on which SPINVM bridge and eNVM run) to SCLK (serial clock) must be two or higher for the design to function correctly.

## Utilization Details

This design was verified in the Fusion AFS600-484 FBGA, but can easily be instantiated in other Fusion devices that contain the minimum required resources. The device utilization values listed in [Table 4](#) are for the AFS600-484 FBGA device.

**Table 4 • Utilization Details**

Resource	Utilization	Total	Percentage
Core	580	13824	4.20
I/Os	6	172	3.49
Global(Chip+Quadrant)	3	18	16.67
PLL	0	2	0.00
RAM/FIFO	0	24	0.00
NVM	1	2	50.00





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