Prototyping for the RTSX-SU Enhanced Aerospace FPGA

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Introduction

Microsemi®SoC Products Group provides radiation-tolerant FPGAs for space applications. However, since the enhanced environmental properties of radiation tolerant devices are not required during prototyping, inexpensive commercial equivalent devices can be substituted during this design phase. This application note describes the basic prototyping methodology for the space qualified RTSX-SU FPGA devices using the commercial equivalent SX-A FPGA devices. This application note includes the prototyping flow, prototyping package options, and other prototyping considerations.

Compatible Devices

Since the RTSX-SU family of devices are 100% library compatible and density-matched with the SX-A family of devices, designers can first complete a design targeting the RTSX-SU, and then simply retarget the design to an equivalent SX-A device when prototyping. Refer to Table 1 for the correlation between the SX-A device and matching RTSX-SU device.

Table 1 • **Equivalent RTSX-SU and SX-A Devices**

Device	32,000 Gates	72,000 Gates
RTSX-SU device	RTSX32SU	RTSX72SU
SX-A equivalent	A54SX32A	A54SX72A

Prototyping Flow

In order to produce designs that satisfy application specifications and requirements, designers may utilize various deign tools, techniques, and verification strategies. However, to increase efficiency when prototyping for the RTSX-SU, the recommended prototyping flow is illustrated in Figure 1 on page 3.

Prototyping Flow Description

Step 1: Complete All Application Specifications and Design Requirements

Step 2: Target RTSX-SU in Designer and Complete Design Entry and Analysis

Implement the design targeting the RTSX-SU device in the SX-A family. This includes design capture (HDL or schematic), pre-synthesis simulation, synthesis, post-synthesis simulation, place-and-route, post-layout simulation, and static timing analysis. For designers using Libero™ Integrated Design Environment (IDE), refer to the latest version of Libero IDE online help or the user's guide for the *Libero IDE design flow*. Ensure to complete design-specific pin allocation, probe, and JTAG specification also. Note that for synthesis, Microsemi's Designer software uses RTSX-SU libraries for timing-driven synthesis for RTSX-SU. However, for simulation, SX-A libraries are used for both RTSX-SU and SX-A devices.

Then, during place-and-route and static timing analysis in Designer, you must target the RTSX-SU device to associate the correct package and timing information with the design.

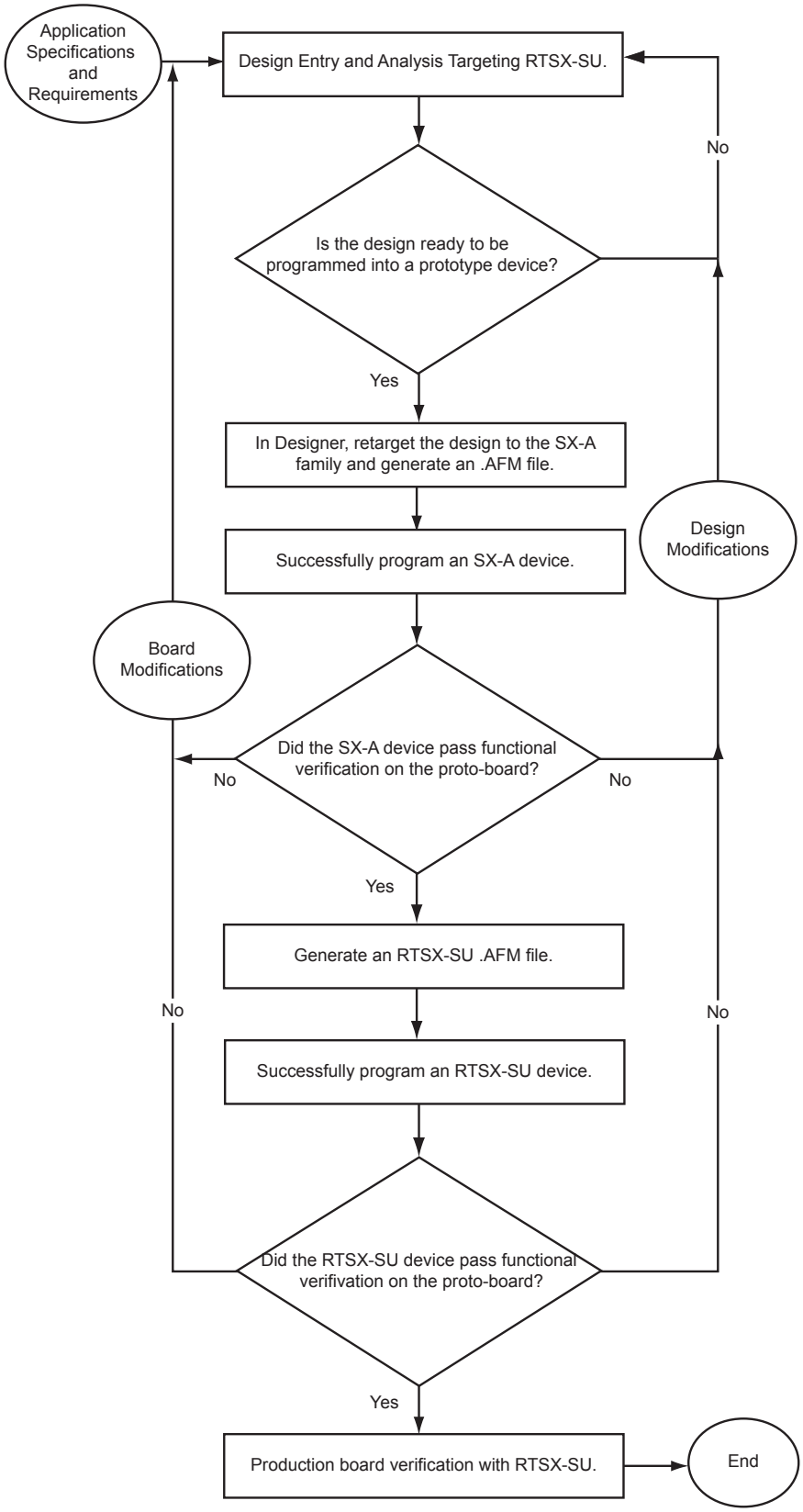

***Figure 1* • Prototyping Flow Diagram**

Step 3: Retarget Design to the SX-A Device

Once the design meets functional and timing requirements, retarget the design to its commercial equivalent.

In Designer, retarget the design from RTSX-SU to SX-A by selecting the following option from the Designer software tools menu: Tools > Device Selection > SX-A. This methodology ensures that all of your design specifications and constraints are carried over to the prototype device few exceptions listed below.

When retargeting the SX-A device from the RTSX-SU device, consider the following:

1. If the I/Os were previously configured as 5 V CMOS in the RTSX-SU design, they should be changed to 5 V TTL in the SX-A design. This is because the SX-A device family does not fully support 5 V CMOS I/Os. Therefore, during board-level verification, consider TLL and 5 V CMOS I/O specifications (that is VIH/VIL/VOH/VOL).
2. If the original targeted RTSX-SU device package is CQ256, select the FG484 for the SX-A device, as the SX-A device was not designed with a 256-pin plastic quad flat pack equivalent package. Note that repeating place-and-route is not required. See the "Prototyping Package Options" section on page 5 for details regarding the proper selection of prototyping device packages.

Step 4: Program an SX-A Device

To program a device, you must first generate a*.afm file, which is a design and package specific programming file. To generate a *.afm file, click **FUSE** in the **Designer GUI** and select **.AFM** from the drop-down menu. Once the *.afm file is generated the FUSE button turns green. The *.afm file is the only file required for programming and contains two sections:

- Header section – contains software and device information as well as the FUSECHECKSUM
- Programming section – contains the encrypted programming information

Note: The *.afm file programming content is different as it is appropriate for its targeted device family. Therefore, program the SX-A device only with the *.afm file specifically generated for it. Likewise, program the RTSX-SU device only with the *.afm file specifically generated for it. Mismatching or manually editing *.afm files in any way is not supported

To program the SX-A or RTSX-SU device, you need the following materials:

- PC
- Silicon Sculptor III programmer
- Silicon Sculptor III programming adaptor module (device package specific)
- Silicon Sculptor programming software (Windows or DOS version). Always use the latest version that is updated regularly on the Microsemi website.
- Design specific *.afm file

Step 5: Perform Proto-Board-Level Verification with the SX-A Device

In addition to functional verification of the SX-A design, ensure to verify the power cycling sequence. A power cycling sequence of powering VCCA before VCCI is recommended for the RTSX-SU. See the *RTSX-SU RadTolerant FPGAs for Space Applications* datasheet for details. Also, in addition to JTAG testing, be sure to verify a workable procedure for the required grounding of the TRST pin. See the "TRST Pin" section on page 7 for more information.

Step 6: Programming an RTSX-SU Device

Once the SX-A device successfully passes functional verification, generate a*.afm file targeting the RTSX-SU device and program an RTSX-SU device.

Step 7: Perform Proto-Board-Level Verification with the RTSX-SU Device

Repeat Step 5 using the RTSX-SU device.

Step 8: Production Board Verification

Finally, once the RTSX-SU device has been functionally verified on the proto-board, it is ready for production verification.

Prototyping Package Options

In order to facilitate using a commercial device for prototyping, Microsemi has designed the RTSX-SU device in the CQ208 package to be pin compatible with the equivalent SX-A device in the CQ208 and PQ208 packages. This provides a simple method for customers to make a drop-in replacement from prototyping to production. Unfortunately, there is no equivalent PQ256 device package for the CQ256 package, so prototyping for this device package will have to be done using the FG484 package and a socket in order to match the CQ256 package footprint layout. Refer to the "Prototyping with PQ208 for CQ208 and FG484 for CQ256 Packages and Sockets" section for solder pad dimensions.

Prototyping with PQ208 for CQ208 and FG484 for CQ256 Packages and Sockets

Figure 2 combined with Table 2 on page 6 shows the standard QFP solder pad layout for Microsemi quad flat packs and their associated dimensions.

Table 3 on page 6 contains board layout soldered pad dimensions to be employed if you are using a prototyping socket and either a CQ208, PQ208, or CQ256 package. These dimensions accept CQ208, PQ208, CQ256, and prototyping sockets.

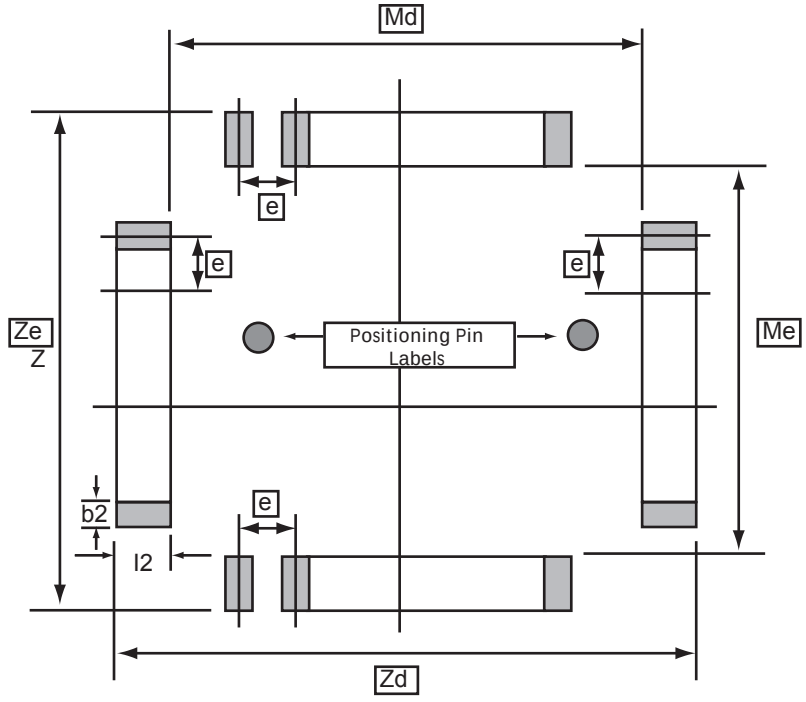

***Figure 2* • Solder Pad Layout**

Table 2 • **Combined PQ208/CQ208 and Prototype Socket / Combined CQ256 and CQ256-FG484 Adapter Socket**

Dimension[1]	PQ208/CQ208[2]	CQ256[2]/CQ256-FG484 Adapter Socket
Md	28.2	40.5
me	28.2	40.5
Zd	35.1	42.5
Ze	35.1	42.5
e	0.5	0.5
b2	0.3-0.4	0.3-0.4
l2	1.6	1.6
Socket Part Number	SY-PQG208[3]	SI-SX72-ACQ256SFG484 or SI-SX32-ACQ256SFG484

1. *Dimension = millimeters*
2. *Zd and Ze dimensions are based on trim and form data from Fancort Industries Inc. If you are using trim and form from another vendor, Zd and Ze could be different.*
3. *For the dimensions of the prototype socket, please refer to http://www,microsemi.com/soc/documents/sockets/20G.%20SY-PQG208.pdf*

Table 3 • **Prototyping Grid**

Flight Part	RTSX32SU-CQ84	RTSX32SU-CQ208	RTSX32SU-CQ256	RTSX32SU-CC256	RTSX72SU-CQ208	RTSX72SU-CQ256	RTSX72SU-CG624
Commercial Equivalent Part	A54SX32A-CQ84	A54SX32A-PQ208	A54SX32A-FG484	Not Available	A54SX72A-PQ208	A54SX72A-FG484	A54SX72A-FG484
Prototyping Adaptor Board			SI-SX32A-ACQ256SFG484			SI-SX72-ACQ256SFG484	SK-SX72-CG624RTFG484
Prototyping Adaptor Socket		SY-PQG208			SY-PQG208		
Pad Layout		QFP solder pad layout	QFP solder pad layout		QFP solder pad layout	QFP solder pad layout	See the *Microsemi CCGA to FBGA Adapter Socket Instructions* application note.

Special Considerations

5 V CMOS Prototyping Concern

Apart from the enhanced Single Event Upset (SEU) immunity, the RTSX-SU device has another capability, which the SX-A device lacks. The SX-A device has adjustable input trip points for TTL and PCI modes of operation. The RTSX-SU device has both of these as well as the 5 V CMOS input trip points. This feature allows the device to communicate more easily with certain CMOS devices, which are not designed for TTL noise margins. However, this poses a little difficulty when prototyping for a pure 5 V CMOS environment because the SX-A I/O thresholds are not fully CMOS compliant. For example,

Microsemi's SX-A TTL outputs drive close to rail and can drive 5 V CMOS inputs, but SX-A TTL inputs have lower trip points and less noise margin than 5 V CMOS inputs.

TRST Pin

For RTSX-SU and SX-A, the TRST pin functions as a Dedicated Boundary-Scan Reset pin with an internal pull-up resistor that is permanently enabled on the TRST pin. For SX-A this pin can also be configured as a user I/O. However, this is not recommended for prototyping for RTSX-SU.

During prototyping, employ JTAG by pulling the TRST pin high. However, during flight, the RTSX-SU devices require the JTAG reset pin to be hardwired to ground. This prevents SEUs in the TAP controller from inadvertently placing the device into JTAG mode.

Prototyping with RT_PROTO Units

For the lower-cost prototyping and final design validation activities, Microsemi offers RTSX-SU, RTAX-S, RTAX-DSP, and RT ProASIC3 FPGAs in "RT-PROTO" form. RT-PROTO devices have the same footprint and timing characteristics as the flight units. They are intended for hardware timing verification only and they should not be used for space flight applications, which require the quality of space flight parts, such as qualification of space flight hardware. Refer to www.microsemi.com/documents/RTPROTO_Description.pdf for more information on prototyping for space flight design with Microsemi RT-PROTO FPGAs.

Conclusion

As it is essential to have a viable prototyping solution to streamline design and development of flight qualified designs, Microsemi produces commercial equivalent devices, prototyping sockets, and prototyping adaptor boards. By using the basic prototyping flow in this application note as a model and after first completing the design targeting the RTSX-SU device and then implementing the commercial equivalent SX-A as the prototyping device, it is apparent that prototyping for the RTSX-SU can become time and cost efficient.

Related Documents

Datasheet

RTSX-SU Radiation-Tolerant FPGAs (UMC)

Application Note

Microsemi CCGA to FBGA Adapter Socket Instructions

Miscellaneous

Libero IDE Design Flow

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 2 (April 2012)	The Table 2 was updated (SAR 20911).	6
	The Table 3 was updated (SAR 20911).	6
	The "Prototyping with RT_PROTO Units" was added (SAR 20911).	7

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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