Differences Between RTAX-S/SL, RTAX-DSP, and Axcelerator

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Introduction

RTAX-S/SL and RTAX-DSP are field programmable gate array (FPGA) family devices by Microsemi designed for space applications and is a derivative of the Microsemi Axcelerator® FPGA family. The RTAX-S/SL and RTAX-DSP architecture is based on Microsemi's multi-featured, high-density Axcelerator architecture with enhancements for a high level of single-event upset (SEU) immunity. To achieve this, some Axcelerator features were removed from the silicon and other features were enhanced or added.

The purpose of this application note is to facilitate the prototyping process by highlighting the differences between RTAX-S/SL, RTAX-DSP, and Axcelerator. This document supplements the Microsemi application note *Prototyping RTAX-S Using Axcelerator Devices*.

RTAX-S/SL and RTAX-DSP Modifications for SEU Immunity

To ensure SEU immunity, the following Axcelerator features are not included in the RTAX-S/SL and RTAX-DSP feature set.

PLL

All eight phase-locked loop (PLL)s that are included in Axcelerator are not part of RTAX-S/SL or RTAX-DSP. The corresponding PLL supply voltage pins (VCCPLX and VCOMPLX) have become No Connects (NC). These pins are not connected to any circuitry in the device and can be driven to any voltage or left floating with no effect on the operation of the device. In addition, the special PLL macros cannot be used because they are not part of the RTAX-S/SL or RTAX-DSP macro library. These include PLLINT, PLLRCLK, PLLHCLK, PLLFB, and PLLOUT.

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LP Mode

The low-power (LP) mode capability that is featured in Axcelerator is not part of RTAX-S/SL or RTAX-DSP. The corresponding LP pin has become a GND pin. However, the VPUMP pin is still available for external charge pump access for chip power savings. To use the external pump, VPUMP must be 3.3 V to 3.6 V. When the external charge pump applies 3.3 V to the VPUMP pin, the internal charge pump is disabled, and the external charge pump will then drive the internal "pump" line. To use the internal pump, the VCCA supply must be powered up and VPUMP can be tied directly or through a 1K resistor to GND.

Programmable Input Delay Elements

For Axcelerator, the programmable input delay can be set for regular inputs and clock inputs. For RTAX-S/SL and RTAX-DSP, these input delay elements are not available for clock inputs but the option is still available on regular inputs.

Enhancements for Improved SEU Immunity

As mentioned earlier, several Axcelerator features have been improved to enhance SEU immunity. The following sections describe those features and their improvements in the RTAX-S/SL and RTAX-DSP FPGAs.

Flip-Flops

All dedicated flip-flops employ triple modular redundancy (TMR). This includes all flip-flops implemented with R-Cells and all I/O registers: input registers (InReg), output registers (OutReg), and enable registers (EnReg).

Global Resources

All four hardwired clock (HCLK) and all four routed clock (CLK) clock-trees have been enhanced to improve SEU immunity.

Embedded SRAM/FIFO

Since the SRAM does not employ TMR, error detection and correction an EDAC intellectual property (EDAC IP) core can be implemented to enhance SEU immunity. For EDAC implementation details, refer to the *Using EDAC RAM for RadTolerant RTAX-S FPGAs and Axcelerator FPGAs*. The internal RAM/FIFO controller is not RadTolerant but can be implemented at your discretion, based on system and/or SEU requirements. Alternatively, the SRAM can be controlled through the use of regular core logic.

JTAG/Probe Circuitry

The JTAG circuitry is not RadTolerant. Therefore, the TRST pin must be hardwired to ground during flight to hold the JTAG circuitry in reset. This ensures maximum SEU immunity.

Note: The TRST pin has an optional 10k pull-up resistor that can be disabled.

During flight, the following configurations for all JTAG and Probe pins are recommended (Table 1).

Table 1 • **JTAG and Probe Pin Recommendations for Flight**

JTAG and Probe Pins	Configurations
TCK	• Can be hardwired to VCCDA or ground • Can be driven to VCCDA or ground • Must not be left unterminated
TDO	Must be left unconnected

Table 1 • **JTAG and Probe Pin Recommendations for Flight (continued)**

JTAG and Probe Pins	Configurations
TDI	• Can be hardwired or driven to VCCDA • Can be left unconnected (equipped with internal 10k pull-up resistor)
TMS	• Can be hardwired or driven to VCCDA • Can be left unconnected (equipped with internal 10k pull-up resistor)
TRST	Must be hardwired to ground (equipped with optional internal 10k pull-up resistor)
PRA/B/C/D	Those pins can be left unconnected or can be connected through pull-up or pull-down resistor to VCCI or GND. PRA/B/C/D pins are in tristate mode during normal operation. In test mode, these pins put out the logic value of the internal node they are connected to.

Enhancements for Improved SET in RTAX-DSP

In addition to the SEU enhancement mentioned above, the R-Cell in the RTAX-DSP is enhanced with additional single event transient (SET) mitigation of the last output buffer. For RTAX-DSP R-Cell, the output buffer is tripled to three buffers with their outputs connected to a single node. If one of the tripled buffers suffers an SET event, the other two will subdue this SET effect and maintain correct signal. This mitigation solution is called triple-drive. With it, the R-Cell in RTAX-DSP is expected to be fully single event effects (SEE) mitigated. As SET is more sensitive at higher frequency, this enhancement is valuable for RTAX-DSP devices because it is intended for DSP applications where high frequency is often utilized.

Additional Features

Mathblock Multiply-Accumulate Function (RTAX-DSP only)

The RTAX-DSP has an addition of up to 120 flexible and cascadable embedded radiation-tolerant 18-bit x 18-bit multiply-accumulate blocks each capable of operating at 125 MHz over the full military temperature range (-55°C to 125°C), for a total throughput of 15 billion multiply/accumulates per second (15 GMACS).

This allows the integration of complex DSP functions into a single device without any external components for code storage and without multiple chip implementations for radiation mitigation. Refer to the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet for more details.

Development Software Support

The RTAX-S/SL and RTAX-DSP FPGAs are fully supported by Microsemi Libero® System-on-Chip (SoC), a design management environment that guides you through the FPGA design flow and provides seamless design tool integration, as well as project, data file, and log file management. Libero SoC enables you to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. The Microsemi designer toolset is included for back-end product implementation and programming file generation. Libero SoC and designer software tool suite has a built-in design rule check (DRC) that provides feedback, error messages, if features that are not supported in RTAX-S/SL and RTAX-DSP are used. For example, the instantiation of unsupported macros (that is, PerPin FIFO and PLL macros) generate error messages during software flow indicating that such features are not supported in the targeted RTAX-S/SL or RTAX-DSP devices.

Conclusion

The RTAX-S/SL and RTAX-DSP architecture is based on Microsemi's multi-featured, high-density Axcelerator architecture but enhancements for a high level of SEU immunity. To achieve this, some Axcelerator features were removed from the silicon and other features were further enhanced or added.

RTAX-DSP space-flight FPGAs add embedded radiation-tolerant multiply-accumulate blocks to the tried-and-trusted industry-standard RTAX-DSP product family. This gives RTAX-DSP a significant advantage in power consumption and heat dissipation relative to SRAM-based FPGAs.

Related Documents

Datasheets

RTAX-S RadTolerant FPGAs

www.microsemi.com/soc/documents/RTAXS_DS.pdf

Axcelerator Family FPGAs

www.microsemi.com/soc/documents/AX_DS.pdf

Application Notes

Prototyping RTAX-S and RTAX-SL Devices

www.microsemi.com/soc/documents/PrototypingRTAXS_AN.pdf

Using EDAC RAM for RadTolerant RTAX-S/SL and Axcelerator FPGAs

www.microsemi.com/soc/documents/EDAC_AN.pdf

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 1 (October 2012)	The "RTAX-S/SL and RTAX-DSP Modifications for SEU Immunity" section was revised by updating the programmable input delay support (SAR - 37602 and 33051).	1
	The "Enhancements for Improved SET in RTAX-DSP" section was added.	3
	The "Mathblock Multiply-Accumulate Function (RTAX-DSP only)" section was added.	3
	The "Development Software Support" section was revised.	3
	The "Conclusion" section was revised.	4

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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