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# RTAX-S/SL/DSP Programming Guide

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## Introduction

Programming of RTAX-S/SL/DSP FPGAs requires utmost attention in various areas. Without a proper hardware and software setup, customers may experience higher than expected failure rate which will incur additional cost to them.

This document contains information about programming Microsemi SoC RTAX-S/SL/DSP FPGAs using Silicon Sculptor II and III programmers. The document also contains programming and programming failure troubleshooting guidelines to ensure proper programming and help customers achieve the highest possible programming yield of the RTAX-S/SL/DSP FPGAs.

## Hardware Setup

RTAX-S/SL/DSP FPGAs are programmed with Silicon Sculptor II and III programmers. Before programming each FPGA you need to make sure the programmers are within calibration. The verification of calibration ([www.microsemi.com/soc/documents/SiliSculptProgCali\\_UG.pdf](http://www.microsemi.com/soc/documents/SiliSculptProgCali_UG.pdf)) and Self-Test (also known as programming diagnostics) with the required programming adapter module must be performed before programming each FPGA. The verification of calibration requires a special adapter module (Microsemi SoC Part Number: SM48DB, BPM Microsystems Part number: SM48D). You must buy this adapter module during the purchase of any Microsemi SoC or BPM Microsystems programmers. The Self-Test needs to be performed with the required adapter module installed, but without an FPGA inserted. Performing a Self-Test with a FPGA inserted can damage the FPGA.

You should also keep a redundant programming set-up (a programmer and adapter module) in case a problem is diagnosed with the first set-up. Having this redundant set-up will be helpful if there is a project deadline constraint. The Silicon Sculptor programmer needs FPGA and package specific adapter modules. A complete list of the adapter modules is available online at: [www.microsemi.com/soc/products/hardware/program\\_debug/ss/modules.aspx#ax\\_rtaxs](http://www.microsemi.com/soc/products/hardware/program_debug/ss/modules.aspx#ax_rtaxs).

Alternatively, the programming software (SculptW or BPWin) can be checked to get the part number of the required adapter module. Refer to the FAQ# 5 in the [Antifuse Programming FAQ](#) document for details.

You need to monitor the insertion limit of the adapter module. The insertion limit of Standard Pitch Socket Modules (i.e. for CQFP packages) is 10,000 cycles. The insertion limit of the Module base is 50,000. Insertion limit can be checked from the Silicon Sculptor software using **Tools > Socket Module Counter**.

You should carefully insert and remove the module from the programmer to avoid damage to the DIN connectors. Typical insertion cycles can be prolonged if the module base and socket modules are properly cleaned and maintained. Handling and cleaning practices can affect the number of insertions achieved.

## Power Supply Requirements

In addition, consideration must be made to ensure quality of the power supplies used to power the Silicon Sculptor programmer. The programming time for RTAX2000S/SL/D FPGAs is of the order of 2 hours, and the programming time for RTAX4000S/SL/D FPGAs is of the order of 4 hours. Therefore, any brown-outs, voltage spikes, or other anomalies on the power supply that could adversely affect programming are more likely to affect programming yield when the FPGAs being programmed are RTAX2000S/SL/D or RTAX4000S/SL/D owing to the time required to program.

Microsemi SoC strongly recommends that a filtered, genuine sine-wave, Uninterruptible Power Supply with sufficient battery back-up to allow for the entire programming time plus a safety margin of 20% be used with both the Silicon Sculptor II or Silicon Sculptor 3 programmer and with the computer attached to the programming hardware that is running the programming software. Such supplies are relatively inexpensive these days and are orders of magnitude less than the cost of programming failures. It should be remembered that a power failure during programming will irrevocably damage the silicon and a new FPGA will be required.

## Software Setup

Microsemi SoC strongly recommends using the latest Designer software version to generate the \*.afm file as well as the latest Silicon Sculptor programming software version to program the FPGAs. The Silicon Sculptor software is frequently updated in order to accommodate yield enhancements in FPGA manufacturing. These updates ensure maximum programming yield and minimum programming times.

Before programming, always check that the version of the Silicon Sculptor programming software you are using is the most recent:

[www.microsemi.com/soc/download/program\\_debug/ss/default.aspx](http://www.microsemi.com/soc/download/program_debug/ss/default.aspx).

You should run the programming software as “Novice Mode” in order to avoid unintentional interruption. If the programming is interrupted by accidental click on the “Stop” button the FPGA will no longer be programmable. Refer to the FAQ#80 in [Antifuse Programming FAQ](#) document for details.

## FPGA Handling

RTAX-S/SL/DSP FPGAs are based on CMOS and require proper grounding and ESD handling procedures. Although all Microsemi SoC parts have static discharge protection built in, you should always follow ESD handling procedures when handling these FPGAs. Handle FPGAs by the corners to avoid touching the leads. Always keep the FPGAs in their insulative carrying cases until they are used, and keep the surrounding environment clean and free of dust and debris. Periodically check the Adapter Module sockets to verify that they are free of dirt or other debris that would prevent good electrical pin connections between the FPGA and socket. You should always wear grounded wrist straps at an ESD workstation when handling RTAX-S/SL/DSP FPGAs. A calibrated ionizer should be on and functioning properly at the workstation. An ionizer air stream should be directed over the parts at all times.

## Inserting the FPGA in the Adapter Module

When loading the FPGAs in the Adapter Module socket, be sure that the orientation is correct. Damage can occur if the FPGA is loaded incorrectly. CQ packages should be loaded in the socket with face down while CG/LG packages should be face up.

For details on handling CG packages, refer to the [Ceramic Column Grid Array](#) application note.

## Troubleshooting Programming Failure

If any RTAX-S/SL/DSP FPGA fails to program, record the error message printed in the log file (c:\BP\DATALOG\BlackBox.log) and perform following actions:

1. For a possible solution, refer to the troubleshooting chapter of Silicon Sculptor User Guide: [www.microsemi.com/soc/documents/silisculptII\\_sculpt3\\_ug.pdf](http://www.microsemi.com/soc/documents/silisculptII_sculpt3_ug.pdf).
2. If the solution for specific error code that you got is given please apply it and program another FPGA after running verification of calibration and self test with the adapter module. If there is no solution available, please contact Tech Support ([soc\\_tech\\_itar@microsemi.com](mailto:soc_tech_itar@microsemi.com)).

If the second FPGA fails to program STOP programming, fill out the [Programming FA checklist](#) and send it to [soc\\_tech\\_itar@microsemi.com](mailto:soc_tech_itar@microsemi.com) along with the log file.

## List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 1 (September 2011)	In the Hardware Setup section, the referenced document for verification of calibration was corrected to SiliSculptProgCali_UG.pdf (SAR 34019). Previously it was given as PCN0705_SS_Cali.pdf.	1

*Note: \*The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*



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