Using A54SX72A and RT54SX72S Quadrant Clocks

Architectural Overview

The A54SX72A and RT54SX72S devices offer four quadrant clock networks (QCLK0, 1, 2, and 3) that can be driven from external points or from internal logic signals within the device at minimal die cost (Figure 1). Each of these clock networks individually drives a quadrant of the chip, or they can be grouped together to drive multiple quadrants. These additional four quadrant clocks are high-speed, low-skew networks dedicated to providing suitable paths for high-speed clocks. They can also be used for more local signals in need of low-skew paths or lines with high fanout such as reset and enable signals. Using these built-in networks enables better performance by reducing skew between loads and by freeing up regular routing resources that would otherwise be consumed by large buffer trees.

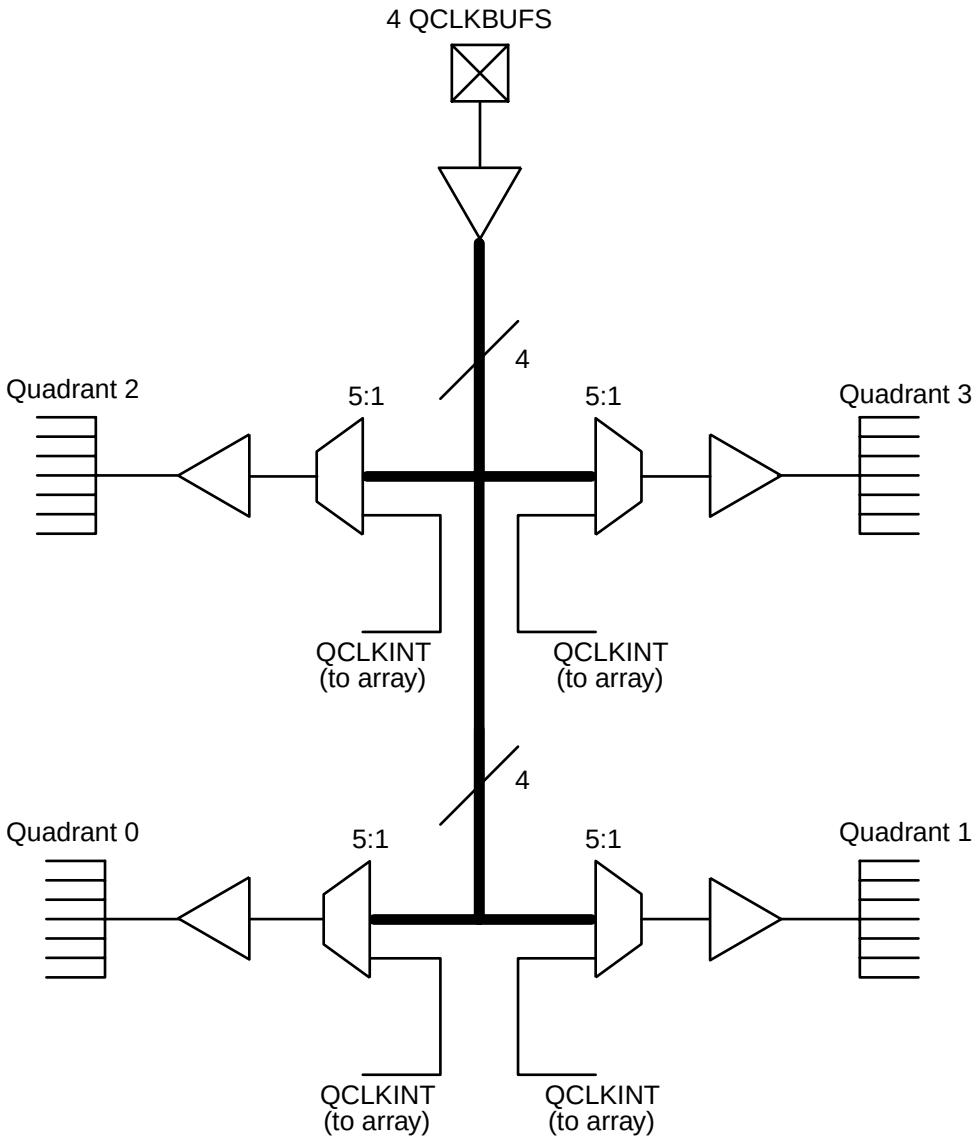


Figure 1 • QCLK Network Architecture

Any module (R-cell or C-cell) can be driven by only the QCLK within that quadrant and by other global clocks (i.e. CLKA, CLKB, and HCLK), but it cannot be driven by the QCLK from another quadrant in the device. Two pads at the top and two pads at the bottom of the chip are available as QCLK inputs. Note that the naming of these input pads as QCLKA, B, C, and D in Actel's Designer software's PinEdit GUI have no bearing on the actual QCLK quadrant used to route this signal. Alternately, any QCLK pins can be used as regular I/Os.

The QCLK network can be accessed through the use of QCLKBUF, QCLKBUFI, QCLKINT, QCLKINTI, QCLKBIBUF, and QCLKBIBUFI macros. The following section lists some key differences between the QCLK macros. Schematics, pin lists, and truth tables of the macros can be found in Actel's *Macro Library Guide* available on located on Actel's website.

Behavior

Due to architectural differences, the behavior differs between QCLKBUF, QCLKBIBUF, and QCLKINT (Figure 1 on page 1).

QCLKBUF/QCLKBUFI

When QCLKBUF is used, Actel's Designer software does not necessarily constrain the routing of the signal to a particular quadrant, but instead, it may be spread out across multiple quadrants (Figure 2). Designer does this even when there are enough resources in a quadrant to contain all registers driven by the QCLKBUF macro. This behavior results from the architecture of the device. There is direct dedicated wiring from each QCLK pin to one of the inputs of each QCLK multiplexor, as illustrated in Figure 1 on page 1.

QCLKBIBUF/QCLKBIBUFI

The QCLKBIBUF macro enables users to alternate between driving the quadrant clock network with an internal signal or an external signal. The architecture and behavior of this macro is similar to QCLKBUF, as Designer software does not try to constrain the registers to a particular quadrant and the signal may be spread and routed across multiple quadrants, as shown in Figure 2. Again, direct dedicated wiring from each QCLK pin to one of the inputs of each QCLK multiplexor is used. However, it should be noted that there is more delay when the quadrant clock network is driven with an internal signal than when it is driven with an external signal through the QCLKBIBUF due to the required routing from an internal node to the QCLKBIBUF.

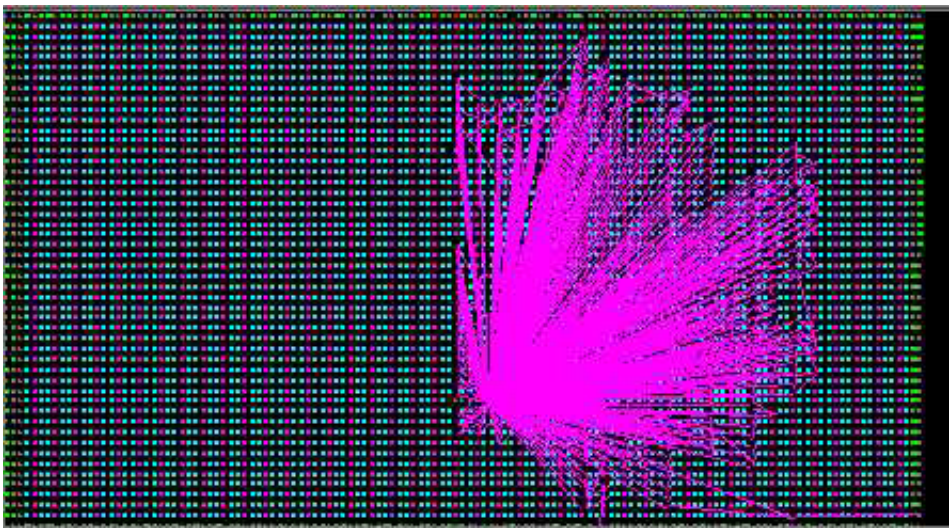


Figure 2 • *ChipEdit View of QCLKBUF and QCLKBIBUF Behavior*

QCLKINT/QCLKINTI

When QCLKINT is used, only one quadrant can be driven by each QCLKINT macro (Figure 3). Actel's Designer software must constrain the signal to a particular quadrant of the device, since a QCLKINT macro is routed by local resources to the fifth input of its associated QCLK multiplexor, as illustrated in Figure 1 on page 1.

When the signal fanout of a QCLKINT macro exceeds the quadrant limit, Designer software gives the following error message during Compile:

```
ERROR: Cannot find an Assignment for Qclocks.
There were 1 error(s) and 0 warning(s) in this design.

The Compile command failed (00:00:07)
```

In this case, multiple quadrants are needed, and one QCLKINT macro must be instantiated for each quadrant to be used, because Designer software does not automatically tie the macros together. The user needs to manually connect each QCLKINT macro to the internal clock net (Figure 4).

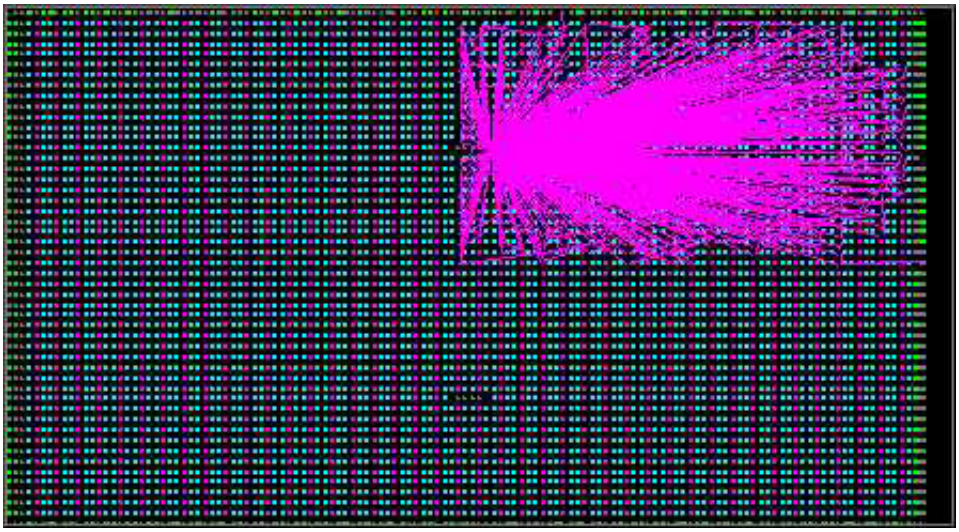


Figure 3 • *ChipEdit View of QCLKINT Behavior*

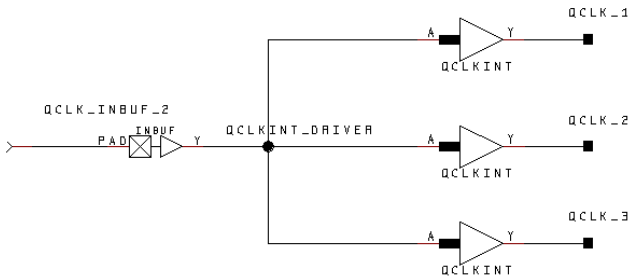


Figure 4 • *Example of Connecting Multiple QCLKINT Macros*

Design Considerations and Tips

Clock Skew

Use of the QCLKBUF and QCLKBIBUF macro results in very low skew regardless of the quadrant employed, because there is dedicated routing between the I/O pad and the QCLK multiplexors. In the case of QCLKINT, there will be a relatively large skew between quadrants because local routing is used to connect the internal logic to each QCLK driver.

For a sample RT54SX-S design with 59% R-cell utilization, using only QCLKBUF, a comparison of the fastest and shortest in-reg path for the entire design shows:

Worst-case skew = ~1.0ns
Best -case skew = ~0.5ns

The same design driven by a QCLKBIBUF macro through internal logic and directly from a pad gives similar results as above for clock skew.

For an alternate design that uses QCLKINT to drive three QCLK networks, the results are as follows:

Worst-case skew:
- Within Quadrant 1: ~1.1ns
- Within Quadrant 2: ~1.0ns
- Within Quadrant 3: ~1.0ns
- Skew between quadrants= ~7.0ns

Best-case skew:
- Within Quadrant 1: ~0.6ns
- Within Quadrant 2: ~0.5ns
- Within Quadrant 3: ~0.5ns
- Skew between quadrants = ~3.0ns

From the above data, note that within each quadrant, the skew of a signal driven by the QCLKINT macro is similar to that of a signal driven by the QCLKBUF or QCLKBIBUF macro across the whole die. However, the skew between quadrants using QCLKINT macro can be large. For this reason, pay special attention to potential skew problems through careful timing analysis when using QCLKINT macros.

The use of the QCLKINT macro to distribute an internally generated clock signal across multiple quadrants should be avoided if possible. One method to reduce this skew is to route the signal out of the device and bring it back into the design through the use of a QCLKBUF or QCLKBIBUF macro for clock redistribution.

Using the QCLKINT Macro to Gang QCLK Quadrants

Due to the architecture of the device, the upper-quadrant QCLK MUXes are grouped together and the lower-quadrant QCLK MUXes are grouped together. The skew between quadrants is reduced if only the upper quadrants are ganged or only the lower quadrants are ganged when distributing an internally generated clock signal through multiple QCLKINT macro instantiations.

Defining the QCLK Quadrant(s) to be Driven

In order to define the particular quadrant(s) to use, layout must first be run without any placement constraint. Then, ALL of the modules in the current quadrant(s) (including the QCLK driver) must be unplaced using ChipEdit. Place and fix one of the macros to each new quadrant, commit the changes, and rerun layout with incremental layout turned off. This will guarantee that the quadrant(s) with the fixed macro is driven by the QCLK signal.

Confining QCLKBUF/QCLKBIBUF to a Quadrant

To confine registers driven by a QCLKBUF/QCLKBIBUF signal to a quadrant, the user needs to first instantiate QCLKINT and INBUF macro (Figure 5) in place of QCLKBUF/QCLKBIBUF in the design, and run place-and-route. Then after a successful layout, the user needs to replace QCLKINT and INBUF with QCLKBUF/QCLKBIBUF (Figure 6) in the original design source and run layout again with the "incremental" option set to FIX. This will keep the signal confined to a particular quadrant. If incremental is set to ON instead of FIX, then additional quadrants may be driven. The same pin location may be used for both configurations, since the QCLK pins can function as regular I/Os.

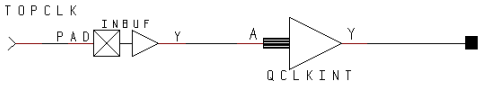


Figure 5 • *External Signal through INBUF Driving a QCLKINT Macro*

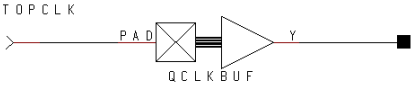
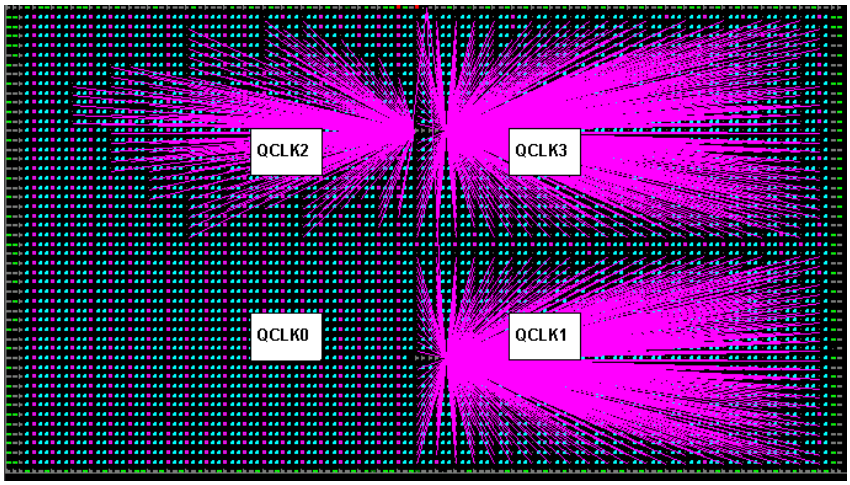


Figure 6 • *A QCLKBUF Macro Driven by External Input*

APPENDIX – QCLK DATA

Layout of QCLK Quadrants



QCLK Quadrant Boundaries

QCLK Quadrant	Columns	Rows
0	3-62	1-23
1	63-128	1-23
2	3-62	25-48
3	63-128	25-48

Note: *Macros in row 24 have their lower inputs driven by the lower quadrants and their upper inputs by the upper quadrants. For this reason, slots in row 24 are not used for Q-clock driven macros unless the quadrants above and below are ganged together.*

Location of QCLK Multiplexers

QCLK Quadrant	Column	Row
0	63	12
1	68	12
2	63	36
3	68	36

Note: *Indexing starts from the bottom left corner of the die.*

QCLK Quadrant Capacities

Section	Logic Tiles	Sequential Tiles
QCLK0	920	460
QCLK1	1,008	504
QCLK2	960	480
QCLK3	1052	526
Middle Row	84	42
Total	**4,024**	**2,012**

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