Physical Interface to QDRII Memories using Actel ProASIC®3E FPGAS

Introduction

Quad Data Rate (QDR) memories are a family of memory products defined and developed by the QDR™ Consortium comprised of Cypress, Hitachi, IDT, Micron, NEC, and Samsung. QDR memories have been developed mainly to address increasing demand for high data bandwidth in today's high speed applications. QDR memories achieve high data transfer rates by providing two independent data paths. One path for read data and another for write data. Each data path uses Double Data Rate (DDR) operation to transfer data. Thus QDR memories effectively transfer four data words (two words on read paths and two words on write paths) in a single clock cycle. This application note shows how to implement a physical interface to QDRII memories in Actel's ProASIC3E devices, as well as IGLOO™e devices, and A3PE3000L device (ProASIC3L family).

QDRII Memory

As clock speed increases, interfacing QDR memories to FPGAs becomes more challenging. This challenge is mainly due to the shorter data valid window that leaves very small timing margin to satisfy device setup and hold times and channel to channel skew in the design. QDRII SRAM architecture is designed to improve the bandwidth of QDR and also to increase the data valid window compared to QDR memories. Furthermore, QDRII memories are equipped with a pair of echo clock outputs which make it easier for designers to latch the read data with certain accuracy.

QDRII memories have 3 pairs of clock ports. The two clocks in each pair are nominally 180 degrees out of phase with respect to each other. The clock pairs are:

K, $\overline{K}$: Input clock pair

C, $\overline{C}$: Input clock pairQD

CQ, $\overline{CQ}$: Output echo clock pair

All inputs to the QDRII memory are synchronous to the K and $\overline{K}$ clocks which comprise the master clocks. The C and $\overline{C}$ clocks comprise output data clocks. CQ and $\overline{CQ}$ are echo clock outputs and are aligned with the read data. This helps the user correctly register the read data from QDRII memory. In relatively low speed applications (~ 133 MHz), the QDRII can operate in simple clocking mode in which there is no need for C and $\overline{C}$ clocks and the read data output is synchronized to the K and $\overline{K}$ master clocks.

The address bus in QDRII memories is shared between Read and Write operations. The operation and usage of the address bus depends on the type of the QDRII memory. QDRII (and QDR) memories are offered in two different methods: 4–word burst and 2–word burst.

4–Word Burst QDRII

In 4–word burst memories, four words of data are transmitted in each Read or Write operation. In this memory, the address bus operates in Single Data Rate (SDR) mode. The Write and Read operations are requested on different clock cycles allowing the address bus to be shared. In 4–word burst memories, every address location is associated with four pieces of data. This is true for both Read and Write operations. With burst of 4, read and write addresses are provided on different clock cycles so the memory controller has to generate only one address in each clock cycle.

If a system application can handle data burst lengths of four, then a 4–word burst memory controller is easier to implement since the address toggles in SDR mode. Moreover, for the same memory configuration, 4–word burst memories use one fewer pin than 2–word burst memories.

Figure 1 shows the timing diagram of a 4–word burst QDRII memory for Read, Write, and No Operation (NOP) commands. For simplicity, it is assumed that the memory is only using K and $\overline{K}$ as input clocks.

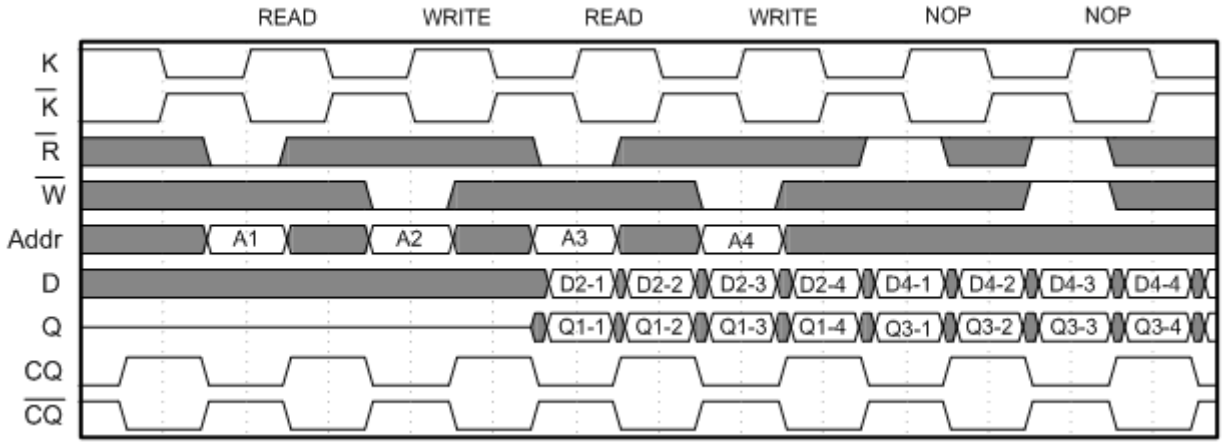

Figure 1 • **Timing Diagram for 4–Word Burst QDRII SRAM**

During Read operations, QDRII memories put out the first read data on the rising edge of $\overline{K}$ (in single clock mode as shown in Figure 1) or $\overline{C}$. In QDR memories, the first read data is clocked out on the rising edge of K (in single clock mode) or C. This is the only functional difference between QDR and QDRII memories.

2–Word Burst QDRII

In contrast to 4–word burst RAM, in 2–word burst RAM, each address location is associated with two pieces of data. Therefore the address line is operated in DDR mode to maintain the quad data rate. Figure 2 illustrates the timing diagram of 2–word burst QDRII memories.

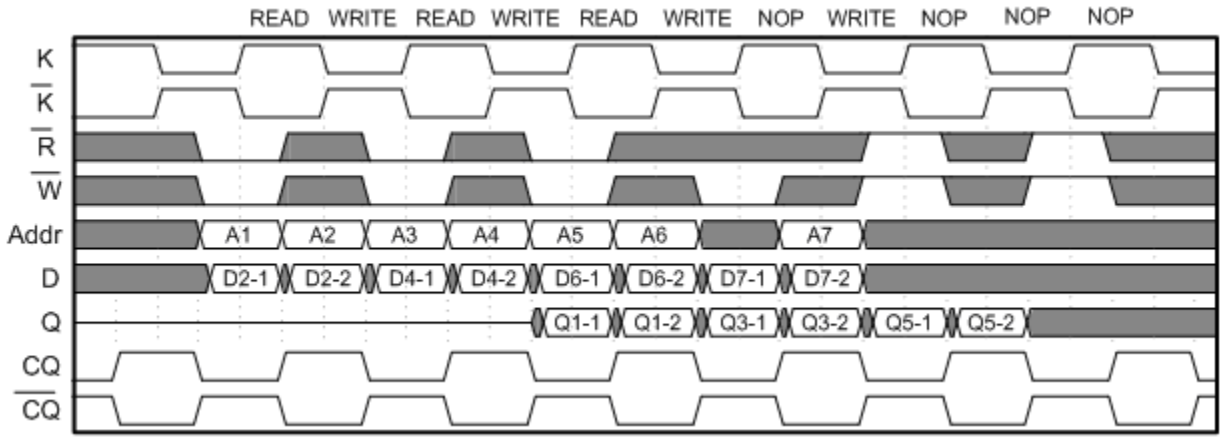

Figure 2 • **Timing Diagram for 2–Word Burst QDRII SRAM**

The address line operates on a DDR basis and is shared for Read and Write operations. Similar to 4–word burst memories, the echo clock outputs (CQ and $\overline{CQ}$) are aligned with read data outputs, making it easier for the receiving device to capture the data in an optimal manner.

FPGA Features

QDRII memory I/Os conform to the JEDEC HSTL standard. ProASIC3E (as well as IGLOOe) FPGAs offer banks of Pro I/Os supporting a variety of advanced I/O standards, including HSTL Class I and II. Furthermore,

ProASIC3E (as well as IGLOOe) FPGAs offer embedded DDR transmit and receive macros in each of the advanced I/Os. This facilitates the interface to QDRII memories in which most of the transactions are carried out using DDR methodology.

ProASIC3E (and IGLOOe) devices are also equipped with six embedded Phase Lock Loops (PLLs). These PLLs facilitate the management of clocks to the QDRII memories. The programmable clock delay and phase shift of the PLLs enable designers to operate at high speeds with relatively large timing margins when interfacing with QDRII memories. See "Physical Interface" for additional information.

This application note does not contain a general user interface that connects to the physical interface. However, the embedded SRAM blocks and hard/soft FIFO controllers as well as abundance of global clock networks in the ProASIC3E FPGA make it easier for designers to create a suitable user interface to the physical interface.

Physical Interface

This section discusses the implementation of the physical interface to QDRII memories. The example implementation in this section assumes interfacing with a 4–burst QDRII memory. However, implementation of physical interface to 2–burst QDRII memory is very similar. It is also assumed that the QDRII memory operates in single clock mode (C and $\overline{C}$ are not used). The 4–burst memory physical interface design is then implemented in a ProASIC3E FPGA. The simulation and timing numbers are also presented.

Implementation

Different components of the physical interface are individually discussed and then combined to form the complete interface.

Clock Generation

To achieve maximum performance of QDRII memories, it is important that the phase difference between K and $\overline{K}$ (and similarly C and $\overline{C}$) are as close as possible to 180 degrees. Though there are many different methods to create two clocks that have an accurate 180 degree phase difference that is robust to changes in operating conditions, two methods stand out. One method is to use the phase shifted outputs of ProASIC3E PLLs and another is to use a PLL to drive the embedded DDR output macros of ProASIC3E I/Os. Both methods are described below.

The embedded PLLs of ProASIC3E devices offer a 180 degree option for phase shifting the VCO output. Therefore the VCO output frequency and its 180° phase shifted counterpart can be used to drive the K and $\overline{K}$ clock inputs of the QDRII memory. Figure 3 shows a simple block diagram of this method.

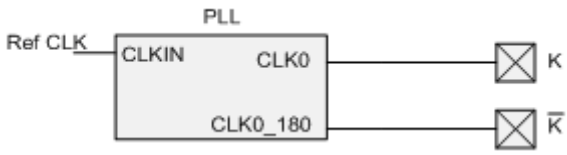

Figure 3 • **PLL Phase Shift Outputs Generating K and $\overline{K}$ Clocks**

The K and $\overline{K}$ clocks are driven via two separate clock networks. Therefore the phase difference between K and $\overline{K}$ is sensitive to loading of each clock network and may be affected if one of the clock networks has significantly higher fanout than the other. In order to eliminate the effect of clock network fanout on the phase relationship of K and $\overline{K}$, drive both clocks from the same clock network. In this case, the 180 degree phase shift between the two clocks can be achieved by using the embedded DDR output macros in the I/O cell. Figure 4 illustrates the usage of DDR output macros to create two clocks that have a 180 degree phase difference.

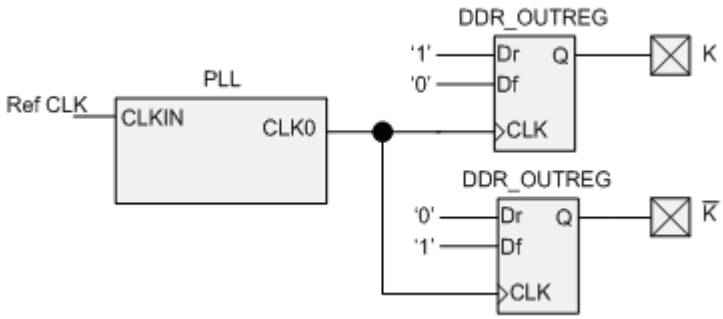

Figure 4 • **DDR Output Macro Generating K and $\overline{K}$ Clocks**

Both K and $\overline{K}$ are driven from the same clock network with edges that transition in opposite directions. This method is used in the example implementation of physical interface in this application note.

The same method can be used to generate C and $\overline{C}$ clocks.

Write Data, Address, and Control Signals Generation

To achieve the maximum performance of the QDRII memory, with sufficient setup and hold for the memory inputs to account for board level channel–to–channel propagation delay skew, the write data, address, and control signals (e.g., read enable) should be center aligned with K,$\overline{K}$ and C,$\overline{C}$ at the output pins of the FPGA. This can be achieved by using the phase shift feature of embedded PLLs. In this approach, the clock used to generate the data, address, and control lines is shifted 90 degrees (or 270 degrees) with respect to the clock used to generate K and $\overline{K}$ (as described in "Clock Generation" on page 3). Figure 5 illustrates this implementation for one of the write data bits to the QDRII memory.

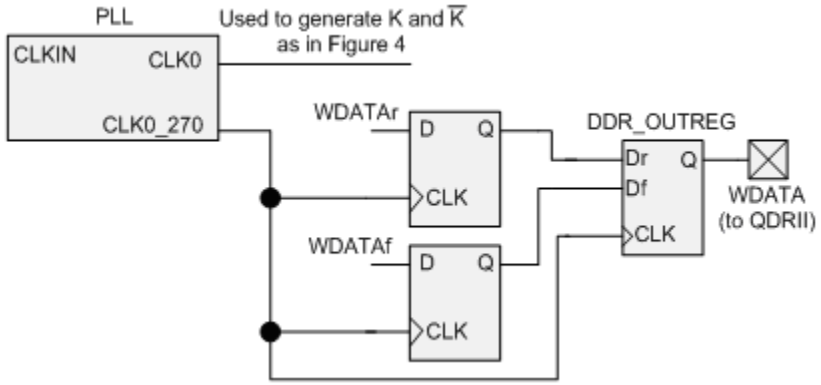

Figure 5 • **PLL Phase Shift to Center Align Write Data with Master Clock**

The CLK0_270 output of the PLL is a 270 degree–phase–shifted version of the CLK0 output. Therefore, with the addition of the clock–to–out delay for the write data path, the WDATA at the FPGA pin will be center aligned with the master clock. See "Timing Characteristics of the Physical Interface" on page 8 for timing analysis of this circuit.

Read Data Path

The read data output of QDRII memory is in DDR format. Actel's ProASIC3E devices offer embedded DDR input registers in the I/Os that enable designers to easily capture DDR inputs.

QDRII memories output two echo clocks (CQ and $\overline{CQ}$) that are aligned with read data output. These clocks are used by the FPGA to capture the read data at the middle of the data valid window. The embedded PLLs of ProASIC3E devices are used to lock onto the QDRII echo clock and generate the read data capture

clock that is center aligned with the incoming data. The output clock of the PLL drives the input DDR registers to capture the read data which can be used by the user interface in SDR format.

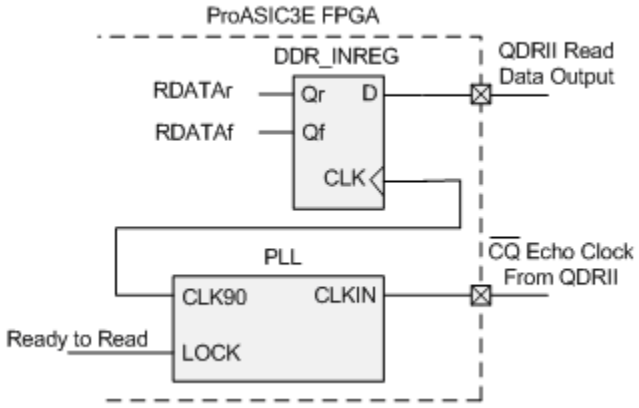

Figure 6 • **Read Data Path Implementation**

Figure 6 shows the read data path implementation in ProASIC3E devices. One of the embedded PLL blocks of the ProaSIC3E device is used to shift the $\overline{CQ}$ echo clock of QDRII by 90 degrees. Shifting the $\overline{CQ}$ clock by 90 degrees results in an output clock with edge transitions center aligned with the read data as shown in Figure 1.

Furthermore, as shown in Figure 6, the lock output of the PLL can be used as a "data path ready" flag. Once the PLL is locked onto the incoming echo clock and a stable capture clock is created, the lock output of the PLL signals the user interface that the physical interface of the read data path is ready for operation.

Combining all the elements discussed in the "Implementation" section on page 3, a simple, efficient, and high performance QDRII physical interface can be constructed inside ProASIC3E devices. Figure 7 shows the implementation of this interface for a 4–word burst, 32–bit QDRII.

In the 2–word burst QDRII memory case, the physical interface implementation is more or less the same as in Figure 7. The main difference is the registers driving the address and control lines (read and write enable). In a 2–word burst implementation the address lines as well as the read and write enable should be DDR output macros (DDR_OUTREG) similar to those for write data. The read data path in a 2–word burst implementation is the same as shown in Figure 7.

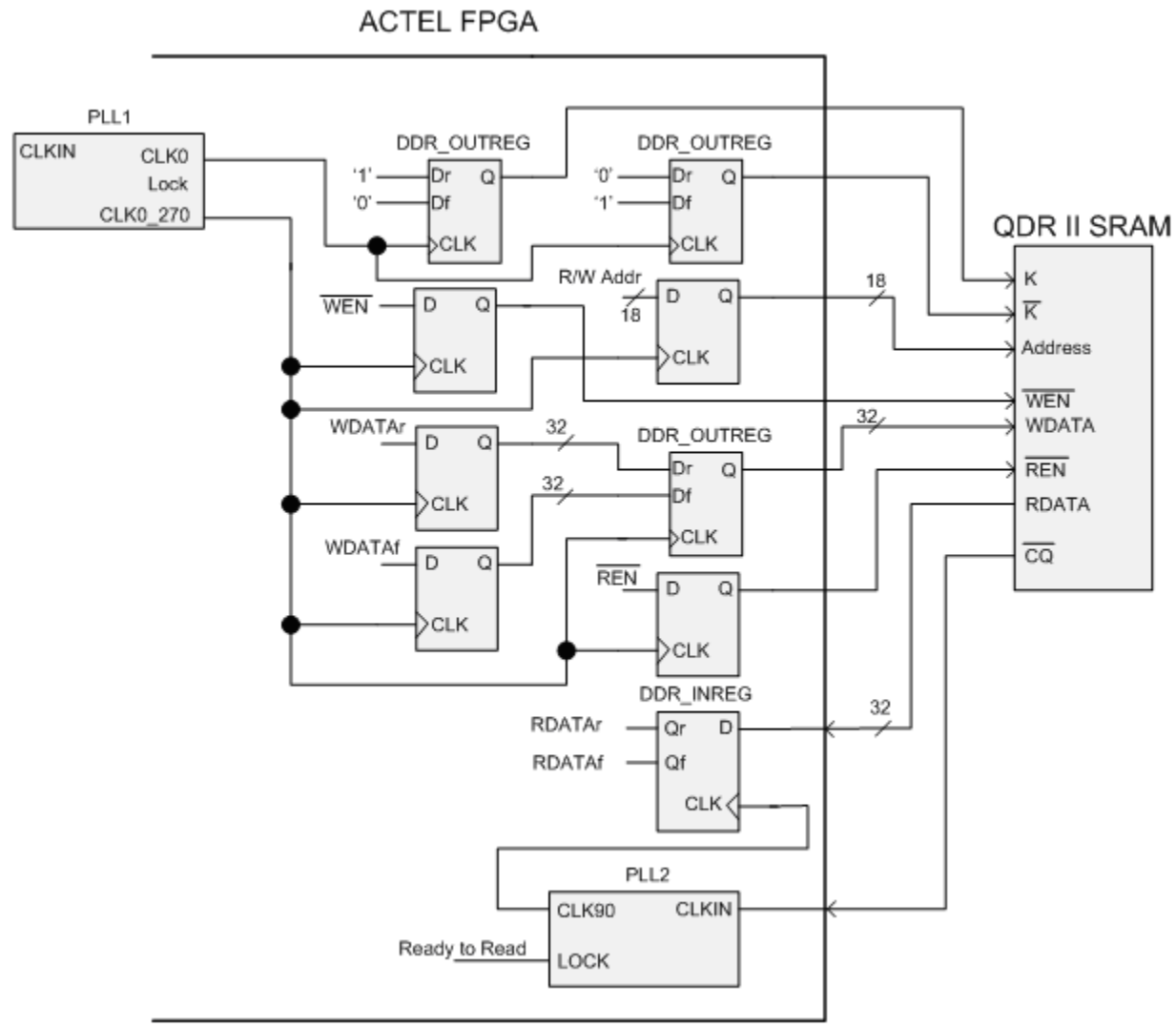

Figure 7 • **4–Word Burst QDRII Physical Interface in ProASIC3E FPGA**

Utilizing I/O Registers

Channel–to–channel skew in clock–to–out timing for data, address and control lines is an important factor in limiting the maximum performance of the memory interface. Minimizing the clock–to–out differences among all data, address, and control pins improves the timing margins significantly and provides more flexibility in board level routing. This becomes more critical as the numbers of data and address bits increase in larger memory arrays. ProASIC3E input and output DDR registers are all embedded in the I/O cell. This minimizes the clock–to–out or input delay skew among pins inside the device. To achieve the same level of channel–to–channel skew on the signals that are in Single Data Rate format (e.g., address lines in a 4–word burst memory interface), the driver registers should be placed inside the I/O macro using ProASIC3E I/O registers. This will minimize the clock–to–out delay and the channel–to–channel skew for these signals. When designing with Actel Designer software, users can configure their I/O ports (by using PDC constraint file or I/O Attribute Editor GUI) to use embedded I/O registers.

Simulation

The physical interface of Figure 7 was implemented in an A3PE600–FG484 (standard speed grade) and simulated in worst case operating condition (110°C ambient temperature and 1.425 V core voltage) using back annotated timing. The QDRII clocks (K and $\overline{K}$) were set to 133 MHz. The simulation results are shown in Figure 8.

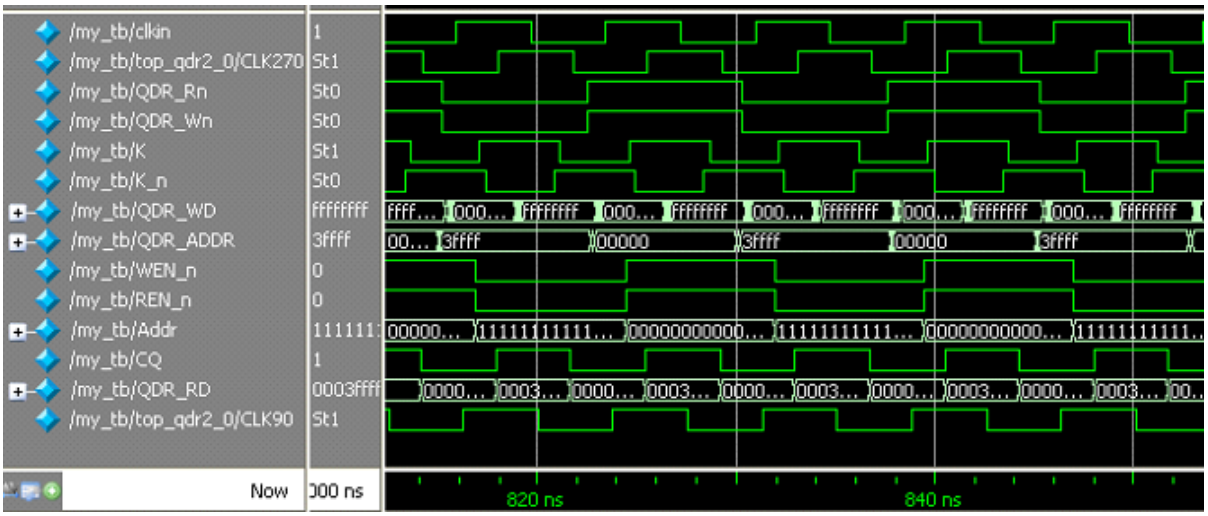

Figure 8 • **QDRII Physical Interface Back Annotated Simulation Results**

The signal descriptions of the simulation shown in Figure 8 are listed in Table 1:

Table 1 • **Simulation Sign Descriptions**

Signal	Description
clkin	System clock input to the design/physical interface
CLK270	PLL output shifted 270 degrees compared to reference clock
CLK90	PLL output shifted 90 degrees compared to reference clock
QDR_Rn	Active–low read enable output from FPGA to the QDRII memory
QDR_Wn	Active–low write enable output from FPGA to the QDRII memory
K	Master clock (K) output from FPGA to the QDRII memory
K_n	Master clock ($\overline{K}$) output from FPGA to the QDRII memory
QDR_WD	Memory write data (32 bits)
QDR_ADDR	Memory address lines (18 bits)
CQ	Echo clock input from QDRII
QDR_RD	Memory read data (32 bits)

In the simulation results of Figure 8, the write data and control lines are center aligned with the master clock to the QDRII FPGAs. This enables designers to achieve optimal timing margins when interfacing with the QDRII memory.

The duty cycle of the master clock outputs (K and $\overline{K}$) is not exactly at 50% as shown in Figure 8. This is mainly due to the output buffer propagation delay difference between a rising and falling edge of the signals. The simulation in Figure 8 is performed with the assumption of 35 pF load on the device I/Os. Smaller loads result in smaller delay variation between rising and falling edges of the signals. Although non–50% duty cycle of master clocks reduces the timing margins, the high performance of ProASIC3E FPGAs makes up for this loss of timing margin. Refer to "Timing Characteristics of the Physical Interface".

Timing Characteristics of the Physical Interface

As stated in the "Simulation" section on page 7, the physical interface was implemented in standard (–std) speed grade of ProASIC3E devices and simulated in worst case operating conditions (110°C and 1.425 V core supply). Figure 9 shows a closer view of the signals in the simulation used to extract the timing information.

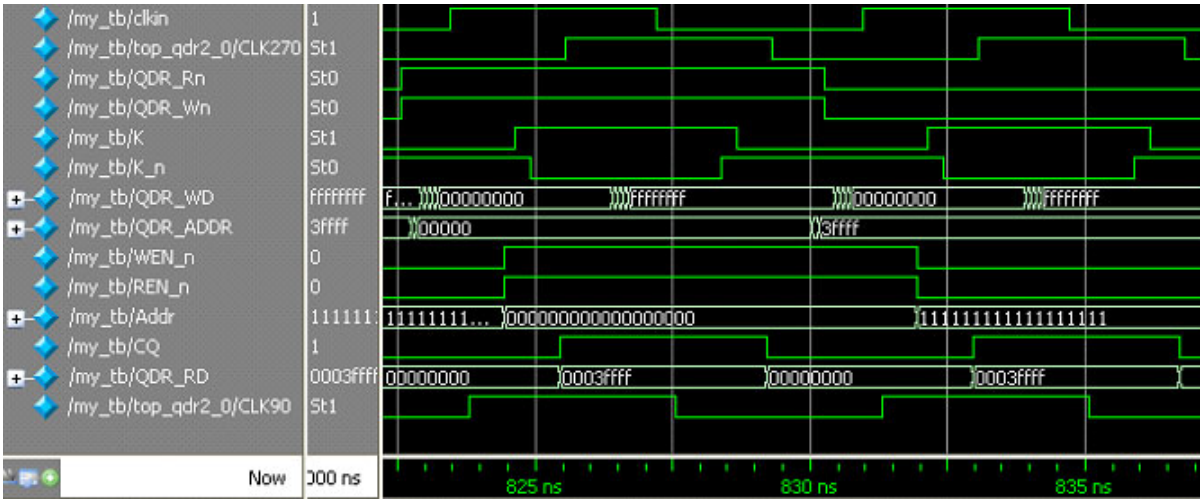

Figure 9 • **Close Up of Physical Interface Simulation**

Write Path Timing

The write path timing is calculated based on the clock–to–out timing of the FPGA, shown in Figure 9 simulation, and the timing requirements (setup, hold, etc.) of the target QDRII memory. If the physical interface of Figure 7 is implemented in a standard ProASIC3E device and interfaced with a Samsung KTR643684M memory, simulation with worst case operating conditions at 133 MHz gives the timing results shown in Table 2.

Table 2 • **Timing Data of QDRII Physical Interface[1, 2]**

Parameter	Name	Spec[3] (ns)	Margin (ns)
Setup — Address	^{t}AVKH	.07	1.3
Setup — Control	^{t}IVKH	.05	0.9
Setup — Data	^{t}DVKH	.05	0.85
Hold — Address	^{t}KHAX	.07	>2[4]

Table 2 • **Timing Data of QDRII Physical Interface[1, 2]**

Parameter	Name	Spec[3] (ns)	Margin (ns)
Hold — Control	^{t}KHIX	.07	>2[4]
Hold — Data	^{t}KHDX	.05	1.2

1.,Timing data is extracted with master clocks running at 133 MHz
2.Timing data of ProASIC3E device is extracted from a dtandard device at 110°C and VCC=1.425 V
3.Spec is extracted from Samsung K7R643684M (–16 speed grade) datasheet
4.By design, as shown in Figure 7 and Figure 8, the address and control lines do not change until the next cycle

The margins in Table 2 are calculated based on the QDRII memory timing requirements, clock–to–out timing of the physical interface in ProASIC3E FPGA devices, and the clock frequency (133 MHz). The timing margins can be used to account for channel–to–channel propagation delay skew on the board (channel–to–channel skew inside the FPGA is included in the numbers of Table 2), clock jitter, and other factors in the design.

The timing margins of Table 2 show that the performance of the physical interface in ProASIC3E device can be easily extended beyond 133 MHz. Note that the timing margins in Table 2 will improve if a faster speed grade device (FPGA and/or memory) is selected in the design.

Read Path Timing

The read path timing margins are extracted based on the clock–to–out delay of the QDRII memory and the input setup/hold requirements of the FPGA with respect to the clock. As shown in Figure 7 on page 6, the echo clock output of the memory is shifted by 270° to center align the read data with the clock driving the DDR input registers. Assuming 133 MHz clock, this will provide ¼ of a clock cycle (~1.85 ns) window to register the data. The timing margins are calculated as follows:

^{t}CQHQV: QDRII memory CQ clock–to–read data valid

^{t}DDRISUD: FPGA DDR input external setup time

Set up timing margin = ¼ Clock Cycle–^{t}CQHQV–^{t}CQHQV

^{t}CAHQX: SRAM CQ clock–to–read data hold

^{t}DDRIHD: FPGA DDR input external hold time

Hold timing margin = ¼ Clock Cycle–^{t}CAHQX–^{t}DDRIHD

Assuming the same memory type as in the "Write Path Timing" section on page 8, worst case operating conditions, and 133 MHz clock, the timing margins can be calculated as:

Setup margin: 1.85 ns–0.4 ns–0.4 ns = 1.05 ns

Hold margin: 1.85 ns–(–0.4 ns)–0 ns > 2 ns

Similar to write path timing, these margins can be further improved if faster speed grade devices are utilized in the design.

Conclusion

ProASIC3E FPGAs offer embedded PLLs with precise phase shift capability as well as I/O support for HSTL and embedded DDR input / output registers. These features, along with the performance of the FPGAs, enable users to interface with large high performance QDRII memories. The capabilities of ProASIC3E devices allows users to easily center align data and control signals with the respective clocks and achieve timing margins that facilitate board level design and low cost. This application note demonstrates the implementation of the QDRII physical interface in ProASIC3E FPGAs and demonstrated that desirable timing margins can be achieved even with the standard speed grade of ProASIC3E FPGAs and slower speed grades of QDRII memories.

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