Post-Programming Burn-In (PPBI) for Actel RT54SX-S and SX-A FPGAs

Abstract

Burn-in (BI) for programmed Field Programmable Gate Arrays (FPGAs) is a growing concern in the space community. This application note addresses these concerns with regard to the Actel RT54SX-S and SX-A FPGA device families in an unprogrammed versus a programmed mode.

This application note discusses the main differences between the architecture of the RT54SX-S and SX-A families and it describes the testing methodologies for Actel FPGAs. It discusses pre and post-burn-in methodologies for unprogrammed units for dynamic and static burn-in conditions and compares these to the programmed conditions for dynamic burn-in. It analyzes Actel's internal Quality Control (QC) design and discusses Ongoing Reliability Testing (ORT) results. It also provides guidelines for acceptable burn-in criteria.

Data in this application note demonstrates that Post-Programming Burn-In (PPBI) for Actel RT54SX-S and SX-A devices is neither required nor recommended.

Introduction

RT54SX-S and SX-A devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility in Japan. RT54SX32S and A54SX32A devices use a three layer metal process while RT54SX72S and A54SX72A devices use a four layer metal process. The RT54SX-S device architecture is an enhanced version of Actel's SX-A device. RT54SX-S devices offer greater levels of radiation survivability than typical CMOS devices.

The main difference between RT54SX-S and SX-A FPGAs is in the R-cell design. Triple Module Redundancy (TMR) is a well-known technique for Single Event Upset (SEU) mitigation. Instead of a single flip-flop, TMR uses three flip-flops hardwired to a majority gate voting circuit. If one flip-flop is flipped to the wrong state, the other two flip-flops override it and the correct value is propagated to the remainder of the circuit. RT54SX-S FPGAs have a self-refreshing TMR built into every register, thereby eliminating the need to use software techniques to perform TMR on each flip-flop. SX-A FPGAs do not have this feature.

Although there are distinct differences between the two product families, they share the identical antifuse design, composition, structure, and process. This application note explains why PPBI is not required.

Architecture

The *RT54SX-S RadTolerant FPGAs for Space Applications* datasheet and *HiRel SX-A Family FPGAs* datasheet describe the architecture of the RT54SX-S and SX-A FPGA families.

Table 1 lists the main differences between the RT54SX-S and SX-A FPGA families.

Table 1 • *RT54SX-S and SX-A FPGAs Differences*

Feature	RT54SX-S	SX-A
Technology	0.25µm	0.25µm
TMR	Built in	Software
Radiation Survivability	Yes	No
TRST Pin	Dedicated	User-defined
5V CMOS I/O	Yes	No
PCI, TTL	Yes	Yes
Charge Pump Enhancement	Yes	No
Military Flows	B, E	B
SEL Immune	Yes	No

Antifuse devices have isolation transistors to keep high programming voltages out of the logic circuits. During normal operation a charge pump drives these gates high to pass a logic signal. The devices put all modules in a predetermined state until the charge pump reaches operating voltage, then the modules immediately switch to a user state. Outputs are tristated until the correct state is reached, then outputs are enabled. To minimize switching noise, slew rate control is available on the general purpose I/Os. The JTAG TRST pin, which should always be grounded in space, is a dedicated input pin for RT54SX-S devices and is user selectable for SX-A devices.

The unique FPGA architecture allows device testing in an unprogrammed state via the JTAG interface. All routing tracks can be addressed and driven to a state of '0'or '1'. The state of any track can be sampled and read back. The output of any logic module can be observed using internal probe circuitry.

Testing Actel FPGAs

The following tests ensure 100% test coverage of Actel FPGAs:

1. A shift register, which can be loaded and read back during testing, circles the periphery of the chip. A pattern of all 0, all 1, and alternating 0 and 1, is loaded and read back.

   The various shift register patterns ensure that different portions of the internal circuits are fully functional. Since the Boundary Scan Register (BSR) is used in several different testing patterns, it is included in this testing.
2. All vertical and horizontal tracks are tested for continuity and shorts.
3. All vertical and horizontal pass transistors are tested for leakage and functionality.
4. The clock buffers, modules, and drivers are fully tested by driving with the clock pins and reading the proper levels.
5. Using the shift register, two special pins, Probe A and Probe B, address the output of each logic module inside the array to ensure functionality. Every logic module in the blank FPGA is fully tested.
6. Through Probe A and Probe B, numerous other functional tests, such as verification of the routed clock modules, are allowed on a blank FPGA.
7. The JTAG BSR can drive all output buffers to low, high, or tristate for testing. Therefore, V_{OL}, V_{OH}, I_{OL}, I_{OH} and output leakage tests are performed. The limits for all output modes are tested.
8. All input modes such as PCI, TTL, and CMOS are configured and tested for V_{IH}, V_{IL}, and input leakage.
9. A dedicated column on the FPGA, which is transparent to the customer, allows Actel to program antifuses connecting inputs and outputs of modules into the "binning circuit." Programming is performed at conditions identical to those used by the programmer (Silicon Sculptor) while programming a customer design.

   This allows Actel to ensure functionality of the programming circuitry and programmed antifuses. It also guarantees speed performance of the FPGA.
10. The device has special circuitry and high voltage devices to isolate low voltage logic from the elevated voltages during programming. Specific tests verify the functionality of this circuitry.
11. Specific tests ensure the reliability and quality of the antifuse in the FPGA and that all antifuses are unprogrammed. These proven electrical screens are performed prior to and after the tests that exercise the programming conditions of the FPGA.
12. Standby current measurement testing is performed for V_{PP}, V_{CCI}, V_{CCA}, V_{KS}, and V_{SV}.

    Every unit in the wafer lot is 100% tested with the above tests. Each test is completed at 125°C, –55°C, and room temperature.
13. Antifuse stress tests are performed only at wafer sort and commercial testing to screen out weak antifuses. After the stress tests, an antifuse shorts test is performed to detect any failures.
14. Each flow goes through B or E-flow per MIL-STD-883E. One major difference is that B flow units go through dynamic blank burn-in only, whereas E-flow units go through both dynamic and static burn-ins.

The above tests (except antifuse stress tests) are performed at military temperatures for both pre and post-burn-ins. Table 2 on page 3 shows the Class E and Class B product flows.

Table 2 • *Actel Mil-STD-883 Flows*

Actel MIL-STD-883 Class E Product Flow	Actel MIL-STD-883 Class B Product Flow
Destructive In-Line Bond Pull3	NA
Internal Visual	Internal Visual
Serialization	NA
Temperature Cycling	Temperature Cycling
Constant Acceleration	Constant Acceleration
Particle Impact Noise Detection	Particle Impact Noise Detection
Radiographic	NA
Seal	Seal
a. Fine	a. Fine
b. Gross	b. Gross
Visual Inspection	Visual Inspection
Pre Burn-In Electrical Parameters	Pre Burn-In Electrical Parameters
Dynamic Burn-In	Dynamic Burn-In
Interim (Post Burn-In) Electrical Parameters	Interim (Post Burn-In) Electrical Parameters
Static Burn-In	NA
Interim (Post Burn-In) Electrical Parameters	NA
Percent Defective Allowable (PDA)	Percent Defective Allowable (PDA)
Final Electrical Test	Final Electrical Test
Static Tests: 25ºC, –55ºC, and +125ºC	Static Tests: 25ºC, –55ºC, and +125ºC
Functional Tests: 25ºC, –55ºC, and +125ºC	Functional Tests: 25ºC, –55ºC, and +125ºC
Switching Tests at 25ºC	Switching Tests at 25ºC
External Visual	External Visual

Actel FPGA Burn-In

Unprogrammed antifuse infant mortality failures are sufficiently screened out during blank device electrical testing. Therefore, it is not necessary to perform a burn-in to screen out infant mortality failures in standard commercial production units. Voltage stress testing of semiconductor devices is a more effective screen than a temperature burn-in[1]. Additionally, as shown in Figure 1 on page 4, defect densities have significantly dropped as semiconductor technology has matured.

1 J.M. Bendetto, "Reliability Analysis of Programmed UTMC PROMs following Post-Program Conditioning." MAPLD Conference (1998).

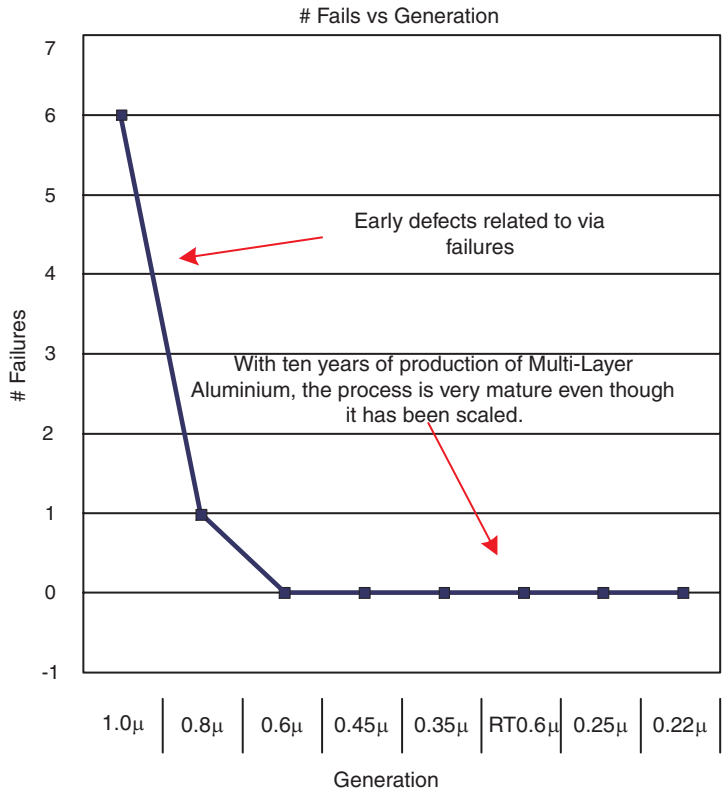

Figure 1 • *Failure Rate versus Technology Generations*

During blank device electrical testing, Actel devices are subjected to controlled voltage stress conditions significantly higher than the maximum operating conditions specified in the datasheet. Due to the lower defect densities and the voltage screening that Actel performs, infant mortality failures have not been an issue. The fallout seen during the burn-in test phases have not been due to defects but to handling and improper burn-in conditions.

Military 883E products require burn-in. MIL-883E Method 1005 enables several types of burn-in screens, which can be divided into two categories: dynamic and steady-state (static). Dynamic burn-in applies AC signals to device inputs. These signals are selected so that the device receives internal and external stresses similar to those it would experience in a typical application. A properly designed dynamic burn-in can effectively stress inputs, outputs, and internal circuits. Dynamic burn-in of ASICs can be very expensive because each ASIC design requires a customer-specific burn-in pattern and burn-in boards must be designed and built to properly stress the device. This results in large NRE costs and long lead times. For burn-in, a programmed FPGA is the same as a mask-programmed ASIC. Both require custom burn-in circuits to perform the dynamic burn-in. However, the testability features of Actel FPGA products provide effective dynamic burn-in of unprogrammed devices. This dynamic blank burn-in (DBBI) enables the stressing of FPGA circuits in a way that a programmed dynamic burn-in is incapable of duplicating.

Dynamic Blank Burn-In

Actel performs dynamic blank burn-in (DBBI) to stress unprogrammed antifuses, inputs, outputs, internal circuits, and I/Os.

During a DBBI stress test, blank FPGA units are inserted onto a burn-in board (BIB) and IEEE 1149.1 JTAG device pins are driven from an EPROM on the burn-in system driver board.

The HCLK, CLKA, CLKB, and QCLKA-D inputs (on A54SX72A and RT54SX72S devices) are driven with a 500 KHz 50% duty cycle clock driver. During the blank device electrical test program, which stresses the unprogrammed antifuses, the V_{PP} pin is biased at 4.5V for the Actel RT54SX-S and SX-A devices.

However, due to accelerated temperature stress on the device during DBBI, the V_{PP} is reduced to 4.1V. The supply pins for SX-A and RT54SX-S devices during DBBI are:

- V_{CCI} = 5.5V ± 0.25V
- V_{CCA}= 2.75V ± 0.25V
- V_{SV} = V_{PP} = 4.10V ± 0.25V

EPROM provides a stimulus to exercise the device through the following sequence:

1. Load the Actel internal Long Scan Register via the JTAG extension command to drive all vertical tracks in the device to '0' and all horizontal tracks to '1'.
2. Set and load the Actel internal Mode Register to setup the cross antifuse stress condition.
3. Load the Mode Register to enable antifuse stress.
4. Load the I/O pattern for bonded out pins via the BSR.
   - Using BSR, each pin is configured to one of the following states:
     – tristated 'Z'
     – driving '0'
     – driving '1'
   - To minimize the simultaneous switching of outputs during burn-in, the BSR pattern (loaded in Step 4) is loaded so that on any given TCK cycle, only one pin in each group of four pins switches between the driving '1' and '0' state. Non-switching pins remain in the 'Z' state. Table 3 shows a sample pattern.

Table 3 • *Pattern Used during DBBI*

Cycle	Pin 1	2	3	4
0	1	Z	Z	Z
1	0	Z	Z	Z
2	Z	1	Z	Z
3	Z	0	Z	Z
4	Z	Z	1	Z
5	Z	Z	0	Z
6	Z	Z	Z	1
7	Z	Z	Z	0

5. Switch the antifuse stress direction by reversing the drive state on vertical and horizontal tracks. This also causes all input and output tracks of the logic modules to toggle, stressing the internal devices of every logic module.
6. Use the BSR to toggle the I/O pins.
7. Repeat Step 3.

Unlike a typical programmed design where only a percentage of logic modules and antifuses are stressed, dynamic blank burn-in stresses 100% of all logic modules, routing tracks, and antifuses. Additionally, switching noise is reduced by toggling 25% of the I/Os at any time.

Static Blank Burn-In

The dynamic blank burn-in process is followed by a static blank burn-in (SBBI). Actel products processed to the E-flow are screened with a static burn-in of the blank device. Static burn-in applies DC voltage levels to the pins of the device under test. Static burn-in is easier to implement if the device is powered-up.

By choosing appropriate biasing conditions and load resistors, it is possible to design a single BIB for both unprogrammed and programmed devices. With a properly designed BIB, the pattern programmed into the device is not important. Static burn-in can be an effective screen for mobile ionic contamination failure modes, which affect device inputs or outputs. Effective design of seal ring barriers and device passivation makes this type of contamination highly unlikely. Static burn-in is not very effective for stressing internal device circuits. Most internal nodes will be biased at ground without receiving any voltage or current stress. The supply pins for the SX-A and RT54SX-S devices during SBBI are:

- V_{CCI}= 5.5V ± 0.25V
- V_{CCA}= 2.75V ± 0.25V
- V_{SV}= V_{PP} = 2.75V ± 0.25V

After burn-in, post-read and record testing is performed as specified by MIL-STD-883E. To ensure that the combined fallout is less than 5%, the percent defect allowed (PDA) is calculated for units subjected to both the DBBI and SBBI (E-Flow only) screening.

Programming

J.M Bendetto[2] reports that an amorphous silicon-based antifuse PROM requires a post-programming temperature bake to cull out infant mortality of programmed antifuses that are subsequently reprogrammed. This is not the case with Actel amorphous silicon antifuse FPGAs. As shown in Figure 2, PROMs by their very nature, have one transistor per switch element (antifuse).

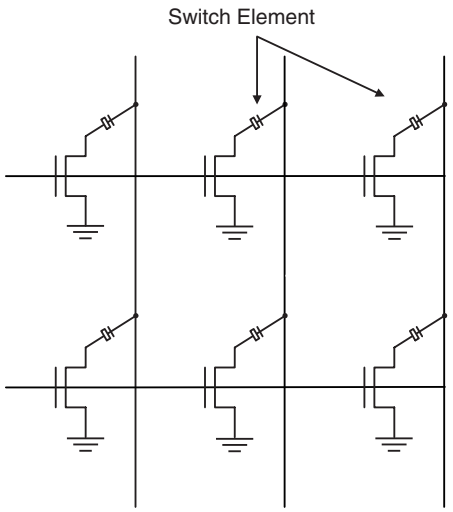

Figure 2 • *PROM Schematic*

The antifuse is small and sits above the silicon, hence the die size is directly affected by the size of the programming transistor. To fit in a reasonable die size, designers must use the minimum size required for the programming transistor.

As a result, the programming currents will be limited to a few milliamps. The sense currents in this type of device can be made small enough (assuming speed is not an issue) without affecting the antifuse during read. However, such a small link is very susceptible to the mechanical stress placed on the link by temperature variations. Therefore, an antifuse programmed at low currents can open up during a bake or temperature cycle stress.

As shown in Figure 3, Actel FPGAs require one programming transistor, which can have as many as 1,000 antifuses per metal track. Furthermore, due to the high speed nature of metal tracks, the interconnecting antifuses must have low resistance (typically 20 to 100 Ω) requiring the programming currents to be much higher than those in a PROM. This makes the programmed metal filament larger and stronger so that high temperature bakes and cycle stress have no effect on the integrity of the antifuse.

2 Bendetto, 1998

All transistors, metal lines, and antifuses have been tested except the programmed state of the antifuse, which needs to be tested during programming. The programming algorithm runs serially and identifies the antifuse to be programmed per the customer generated Actel Fuse Map (AFM) file. This file uniquely identifies each antifuse that needs to be programmed per design.

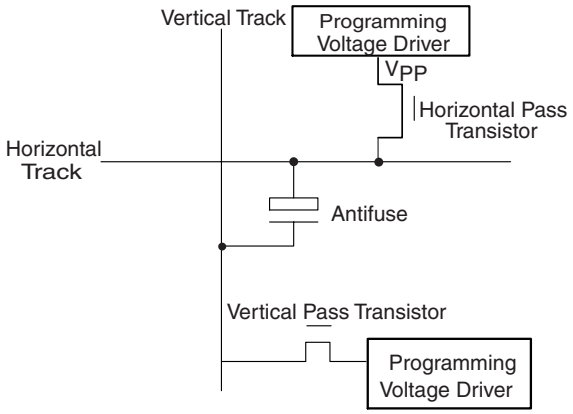

Figure 3 • *Actel FPGA Schematic*

Programming and Testing

The programming and testing process applies pulses to the antifuse that requires programming until a current is sensed. Additional checks are performed at a lower voltage to ensure that the correct antifuse has been addressed and programmed. A soak is performed after programming to ensure that a low resistance antifuse link has been established.

Additional tests are performed before the algorithm moves to the next antifuse. Once the algorithm finishes programming the antifuses, the programmer performs several checks to verify that only the correct antifuses have been programmed. If the correct antifuses have not been programmed, a programming failure has occurred.

To ensure the correct nets have been generated to guarantee the functionality of the part, numerous tests are performed after each antifuse, channel, and column. These tests include:

I_{CCA} Measurement

This measurement ensures that no changes occurred to electrical characteristics of the device after programming.

Before beginning device programming, the programming algorithm performs a pre-I_{CCA} measurement. After programming, the algorithm verifies the post-I_{CCA}

measurements. It compares the pre-I_{CCA} measurement with the post-I_{CCA} measurement, and if the delta exceeds the predetermined delta value, it is deemed a programming failure.

Net Short Test

This test verifies that any unprogrammed antifuses remain unprogrammed after programming is complete to ensure that no sneak paths have been established.

End of Channel

Several End of Channel (EOC) tests are performed after the array antifuse programming. The primary tests check for shorts on the input, output, horizontal, and vertical tracks within the channels.

End of Programming

End of Programming (EOP) tests are performed after completion of the array antifuse programming, EOC, and net short tests. EOP tests include:

- V_{CC} to GND short
- Output to Horizontal and Vertical routing tracks
- Output to Output Short between different columns
- Output to Output Short in the same column
- Clock tracks to V_{CC} or GND
- Clock to Clock
- Other

These tests ensure that all nets are tested for 100% continuity and shorts. Samples of units are programmed to a Quality Control (QC) design from each wafer lot prior to shipment of blank units from that lot. All units are tested for 100% functionality, and no failures are allowed prior to shipment. To date, no functional failures have been reported for processed SX-A and RT54SX-S wafer lots.

After the EOC and EOP tests, the silicon signature and the checksum antifuses, which are unique to each design, are programmed. Finally, the P-fuse, which enables the charge pump and allows the device to function as intended, is programmed.

Dynamic Post-Programming Burn-In

Actel devices are tested with 100% fault coverage testing and screened via dynamic blank and static blank burn-in. This section addresses customer concerns regarding post-programmed device reliability. It covers the testing methodology and reliability data collected by Actel with programmed units. Based on this data, Actel advises customers against performing their own dynamic post-programming burn-in (DPPBI).

In the RT54SX-S and SX-A FPGA families qualification process, a sample of 77 units were programmed and subjected to the Group C testing per Mil-Std-883E TM 1005 for each family. Tests were performed at High Temperature Operating Life (HTOL) and Low Temperature Operating Life (LTOL).

High Temperature Operating Life

High Temperature Operating Life (HTOL) checks for CMOS related failures such as gate oxide breakdown and BVII type issues. HTOL is equivalent to Group C testing. Serialized blank units used for the Group C testing are processed through the B-flow and then programmed to an internal Quality Control Monitor (QCM) design. This design has greater than 95% utilization of the logic modules. This design:

- Uses all the available combinatorial macro cells in the Actel library
- Exercises all the available user I/Os
- Uses a scheme that toggles 25% of the device I/Os per cycle

The design implements built-in self-test (BIST) blocks that use techniques to manage power consumption while maximizing all the features in the product. To ensure the stress of these global networks, the design uses all the low-skew clock resources in the device.

All units are tested for functionality and DC parameters (tristate leakage, continuity, shorts, standby currents). Pre and post-burn-in measurements are performed to check for parametric shifts.

Once the pre-burn-in tests are completed, units are loaded onto the burn-in board per the conditions specified in Table 4 on page 8. Units are tested post-burn-in to check for functional failures or drifts.

Table 4 on page 8 summarizes the qualification and HTOL data collected for the RT54SX-S and SX-A programmed units. All programmed unit burn-in testing is performed at 150°C.

Table 4 • *Summary of HTOL Data for the 0.25 µm*

MEC 0.25µm FPGA Reliability Summary (High Temperature Operating Life (HTOL))								
Product	**Package**	**Test Time**	**# Units**	**Test Hours/Failures**				**Unit Hours**
				168	**500**	**1000**	**2000**	
AX54SX32A	PQ208	500	50	0	0			25,000
AX54SX32A	PQ208	1000	80	0	0	0		80,000
AX54SX72A	PQ208	1000	28	0	0	0		28,000
AX54SX32A	PQ208	1000	88	0	0	0		88,000
AX54SX72A	PQ208	1000	88	0	0	0		88,000
AX54SX72A	PQ208	1000	77	0	0	0		77,000
RT54SX32S	CQ208/256	1000[1]	76	0	0	0		76,000
RT54SX72S	CQ208/256	1000*	77	0	0	1[2]		77,000
RT54SX32S	CQ208	2000	8	0	0	0	0	16,000
AX54SX32A	CQ208	1000*	77	0	0	1[3]		77,000
Total Units for MEC 0.25µm FPGA=			**649**	**Total test time hours=**				**632,000**
Total Failures for MEC 0.25µm FPGA=				**2**				

Notes:

1. *Device hours in test equivalent. Devices tested at 150 °C for 184 hours.*
2. *During the RT54SX-S qualification, 1 of the 77 units failed with excess I_{CCA}. Failure analysis of this unit indicated the root cause of the failure to be EOS (Electrical Over Stress) on the V_{CCA} power supply. A voltage spike on V_{CCA} >5V caused damage to an N-channel transistor resulting in high I_{CCA}. The cause for this electrical failure was traced to EOS in the burn-in system.*
3. *Failure analysis in progress.*

Low Temperature Operating Life

Normally, Low Temperature Operating Life (LTOL) screens for hot electron effects. Actel also runs programmed units through LTOL during qualification to check for programmed antifuse integrity at low temperatures. The transistor drive currents increase by ~20% at –55ºC, and antifuses are more sensitive to current stress than high temperature stress[3].

For the qualification, 45 programmed units were subjected to LTOL and no failures were observed. Table 5 summarizes the LTOL data collected to date for the 0.25µm technology.

3 John McCollum et al., "Reliability of Antifuse-Based Field Programmable Gate Arrays for Military and Aerospace Applications." MAPLD Conference (2001).

Table 5 • *Summary of LTOL Data for the 0.25 µm*

MEC 0.25µm FPGA Reliability Summary (Low Temperature Operating Life (LTOL))								
Product	**Package**	**Test Time**	**# Units**	**Test Hours/Failures**				**Unit Hours**
				168	**500**	**1000**	**2000**	
54SX32A	PQ208	500	50	0	0			25,000
54SX32A	PQ208	1000	80	0	0	0		80,000
54SX72A	PQ208	1000	28	0	0	0		28,000
54SX32A	PQ208	1000	88	0	0	0		88,000
54SX72A	PQ208	1000	88	0	0	0		88,000
RT54SX72S	CQ208	1000	45	0	0	0		45,000
Total Units for MEC 0.25µm FPGA=			**379**	**Total test time hours=**				**354,000**
Total Failures for MEC 0.25µm FPGA=				**0**				

Improper Burn-in

Over the course of Actel's history in the HiRel and Aerospace business, Actel has encountered several customer issues related to incorrect burn-in conditions. Thus, it is very important to understand the reasons for performing burn-in under proper conditions. This section describes the demerits of performing burn-in without a complete understanding of the inherent risks.

Actel has run several experiments for burn-in to establish acceptable burn-in criteria. During the course of these experiments, devices have been damaged when incorrect testing or vectors, systems, and procedures were used. Systems include board design, voltage protection circuits, bypass capacitors, burn-in ovens, fans, heaters, driver boards, cable lengths, power supplies, power lines, sockets and accurate monitors.

Incorrect design of any of the above mentioned parameters could result in device failures. Over voltage or under voltage spikes on power supplies or device inputs can result in CMOS (transistor related) failures. During the course of burn-in acceptable criteria development, experiments showed spikes on the power supply due to turning ON the heater for the burn-in oven in Figure 4. Figure 5 on page 10 illustrates an example of how overstress on an input pin can result in damage to the I/O buffer.

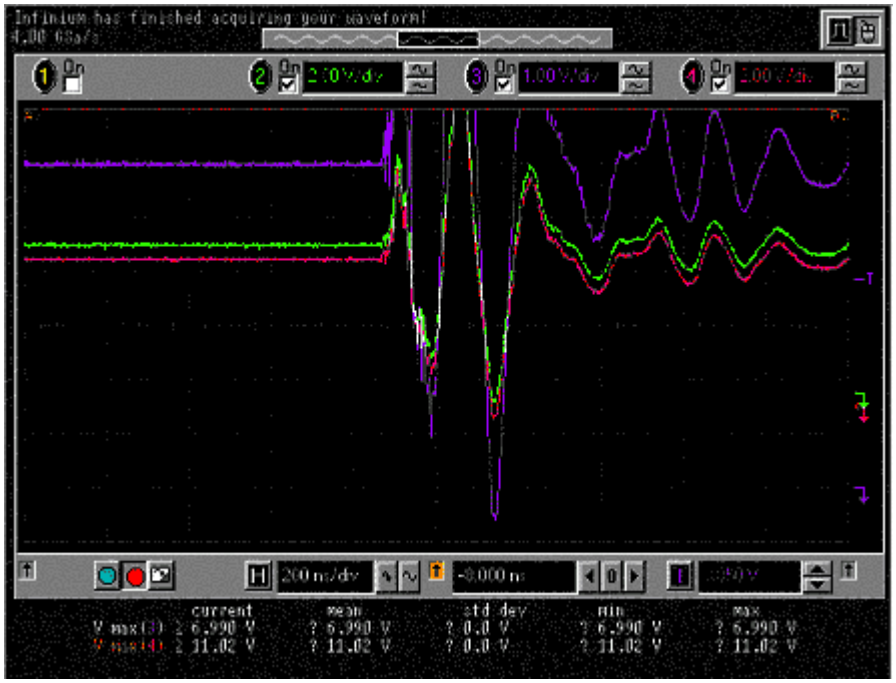

Figure 4 • *Spike on V_{CCA} and V_{CCI} in a Burn-in Oven*

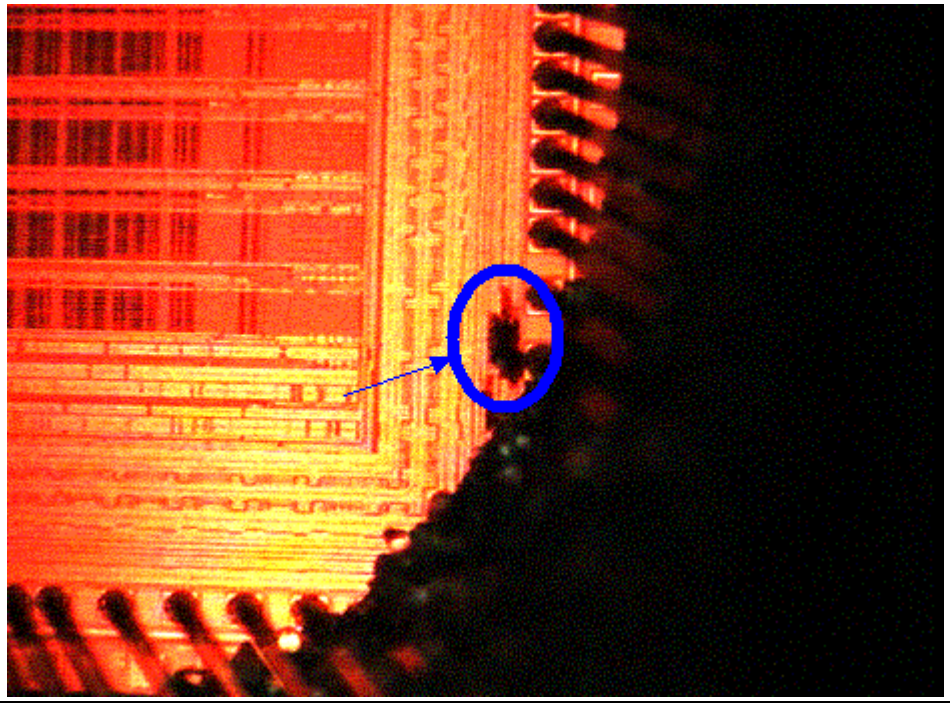

Figure 5 • *Damage to an Input Pin due to EOS*

Detailed attention should be paid to burn-in boards design in terms of the number of DUTs under test and the number of capacitors per DUT power supply. Capacitors to filter out high and low frequency noise must be appropriately chosen based on device operating frequency and PCB trace impedances. Voltage regulator circuits to detect spikes must be carefully incorporated.

Burn-in systems design must consider driver boards, cable lengths, proper terminations, oven conditions, sequence of turning on and off of fans, heaters, power line regulation, and filtering.

Antifuse related failures have also been observed in an incorrectly designed burn-in system. The root cause has been traced to an overstress condition on the V_{CCA} power supply. A spike on $V_{CCA,}$ when coupled with a toggling net, can result in pulsed DC currents in excess of the safe operating limits of the antifuse element, as shown by the red arrows in Figure 6.

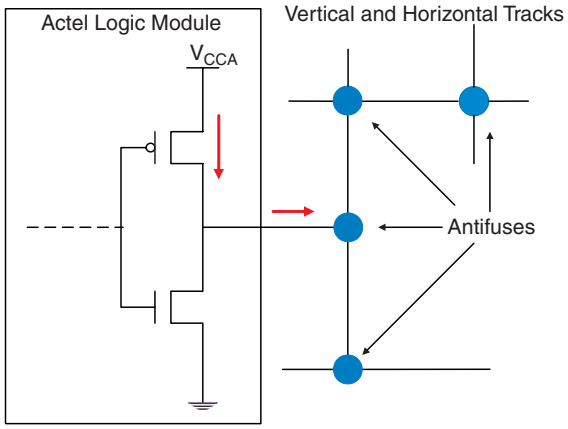

Figure 6 • *Logic Module and Fuses Schematic*

Improper design of any of the above conditions could result in failures of the device during burn-in. Customers have reported burn-in with incorrect power supplies and lack of capacitors on the boards. A spike on the power supply or the DUT inputs of a very short duration (ns) is enough to damage units. As the semiconductor industry moves towards smaller process technologies and lower power supplies, new technologies are increasingly sensitive to out of specification transients. For example:

2.5V spike (for a 5V part) = 50% overstress

2.5V spike (for a 2.5V part) = 100% overstress

2.5V spike (for a 1.5V part) = 167% overstress

Conclusion

The unique architecture of the Actel FPGA allows Actel to test with 100% coverage. All devices go through blank burn-ins (DBBI and SBBI-for E-flow only) that stress unprogrammed antifuses, logic modules, routing tracks, and I/Os. Many verifications are performed during programming to ensure that a robust antifuse link has been established and no unwanted antifuses are programmed. Programmed burn-in at Actel shows highly reliable devices:

- 632,000 hours of burn-in at HTOL
- 354,000 hours of burn-in at LTOL
- No antifuse related failures have been reported

Exercise great care in testing and designing burn-in systems. Considering the complexities and cost of these devices, it is not recommended that customers perform their own burn-in. Actel has effectively shown that PPBI for Actel RT54SX-S and SX-A devices is neither required nor recommended and is best left to the IC vendor.

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