ProASIC3/E SSO and Pin Placement Guidelines

Introduction

Ground bounce and VCC bounce have always been present in digital integrated circuits (ICs). With the advance of technology and shrinking CMOS features, the speed of designs, I/O slew rates, and the size of I/O busses have increased significantly in the past few years. As a result, simultaneously switching outputs (SSOs) and their effects on signal integrity have become an important factor in any digital IC design. When SSOs are not properly designed into a board layout or digital IC, data corruption and system failure may result.

To prevent SSO-induced issues in modern digital systems, designers must compromise an elegant board layout for reliability. An elegant board layout may include practices such as placing all inputs on one side of a chip, outputs on the opposite side, and all bus pins next to each other to make board layout simple. In today's digital systems, utilizing modern FPGAs such as Microsemi ProASIC®3/E may result in data corruption due to ground bounce, VCC bounce, or crosstalk. To design a reliable system for ProASIC3/E FPGAs, follow three simple rules:

1. Identify the SSOs in a design as early in the design cycle as possible, and spread them out across the entire die periphery. Avoid clusters of more than four adjacent SSO pins.
2. Identify sensitive (and usually asynchronous) system signals, and shield them from the effects of SSO (specific shielding techniques are discussed later in this document).
3. Use the lowest possible I/O slew rate and drive strength the design timing will support.

Furthermore, relatively large lead inductance in PQ, TQ, and VQ packages makes these packages more vulnerable to SSOs and hence undesirable for high-speed designs or designs with a considerable number of SSOs. FG or BG packages are preferred in such designs because they show much better SSO performance. By following the above three rules, you will create reliable systems free from the effects of SSOs. The following sections cover specific SSO recommendations and mitigation techniques for designs that do not comply with these recommendations.

SSO Effects

The total number of SSOs for each bus is determined by identifying the outputs that are synchronous to a single clock domain, have their clock-to-out times within ±200 ps of each other, and are placed next to each other on die pads that are on both sides of a sensitive I/O, as shown in Figure 1 on page 2. The sensitive I/O affected by SSO is sometimes referred to as the victim I/O or quiet I/O. SSOs may affect the victim I/O if the total number of SSOs on both sides of the victim I/O exceeds the ProASIC3/E SSO recommendation. It is important to note that the SSOs should be referenced to the die pads and not package pins, since neighboring package pins are not necessarily next to each other on the die (e.g., for BG and FG packages). This can be determined by using MultiView Navigator (MVN) in the Designer software, or die/package bonding diagrams provided by Microsemi. However, when routing traces on the board, it is important to note that SSOs on neighboring traces on the board may affect the quiet I/O surrounded by the SSO traces due to crosstalk or coupling.

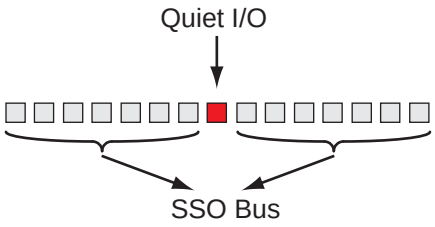


***Figure 1* • Basic Block Diagram of Quiet I/O Surrounded by SSO Bus**

SSO Effect on Power and Ground for Quiet Outputs

If SSOs toggle in one direction (either HIGH to LOW or LOW to HIGH), a significant amount of current quickly begins to flow to the ground or V_{CCI} pins. This current is the sum of the simultaneous sink or source currents of the CMOS output buffers. The quick jump in current causes a voltage drop on the parasitic inductance between the board and die VCCI and ground (V = L × di/dt). For more information about the ground and VCCI bounce phenomenon, refer to the *Simultaneous Switching Noise* application note. The local fluctuations of the VCCI and ground levels may cause the signals on quiet outputs (measured with respect to the fluctuating VCCI and ground) to be misinterpreted as unwanted logic glitches.

SSO Effect on Inputs

SSOs may also affect quiet inputs due to the mutual inductance and capacitance on the package in addition to possible crosstalk of signal traces on the board. SSOs can cause logic glitches on any quiet inputs they surround. The unwanted glitches may cause functional failures if they are propagated through the input buffer. In SSO characterization of ProASIC3/E devices, glitches are considered errors if they cause internal latches in the design to trigger.

SSO Effect on Output Delay (push-out)

As the speed and I/O slew rate of digital ICs increase, effects of ground and V_{CCI} bounce start to surface in digital system designs. One of these effects is output delay or push-out. The ground bounce and V_{CCI} dip induced by SSO transitions creates a temporary collapse of internal VCCI and/or GND supply levels in the output buffers. This change in supply level increases the output buffer propagation delay time. It is important to note that push-out occurs on the SSO bus itself as well as on the victim outputs. Multiple factors, such as SSO bus frequency, drive strength, and slew rate, contribute to push-out. These factors can be adjusted to mitigate the push-out phenomenon. If the clock-to-out time of the victim output is important, the push-out delay should be considered in the timing budget of the design.

SSO Effect on Minimum Input Slew Rate (input maximum rise/fall time)

If the SSOs surrounding an input exceed the Microsemi recommendation, the minimum slew rate requirement for that input may be affected. The minimum input slew rate is the slowest signal transition time (from 0 to 1 or vice versa) at the input that does not cause unwanted logic glitches during signal transition. Figure 2 on page 3 illustrates the unwanted logic glitches with slow transition times. As shown, the logic glitch due to the slow input transition time may cause logic malfunction at edge-sensitive inputs (i.e., clock signals). If the sensitive inputs are affected by the SSO bus, the input minimum slew rate (maximum rise and fall time) should be reduced from what is listed in the device datasheet. Usually, synchronous, level-sensitive inputs are not prone to malfunction due to this phenomenon because their logic value is important only when sampled by a clock.

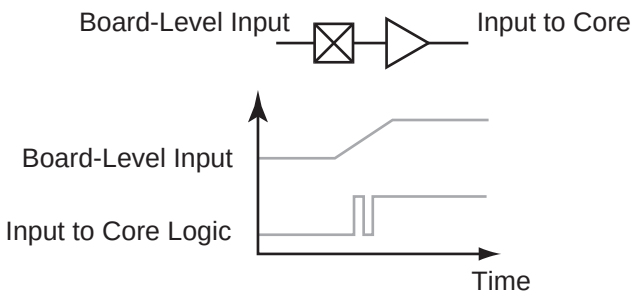


***Figure 2* • Slow Rise/Fall Time Causing Glitches at the Output of an Input Buffer**

Shielding from SSOs

When exposure of sensitive signals (e.g., asynchronous reset) to SSOs is inevitable, these signals need to be shielded from the SSOs to mitigate the unwanted effects. Shielding is basically separating the sensitive signals from SSOs using neighboring pins. Figure 3 shows a basic block diagram depicting a victim output in the presence of an SSO bus.

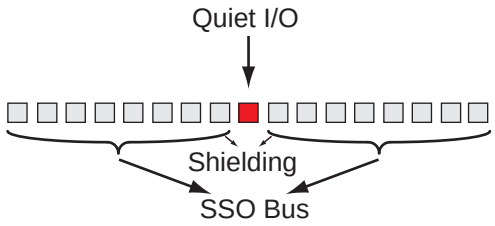


***Figure 3* • Shielding Scheme**

There are different shielding techniques that can be used to protect the victim I/O from the SSO bus. Before describing these techniques, the concept of *virtual ground* and *virtual* V_{CCI} should be understood.

Virtual Ground

Virtual ground, also known as soft ground, is used to improve noise performance. As opposed to a real ground, which is connected to planes within the package, a virtual ground is connected to the planes through the impedance of an I/O buffer. A virtual ground is a ground pin implemented using regular I/O ports. To implement a virtual ground, instantiate an output buffer (with highest drive strength and slew rate) in the design. Tie the input of this output buffer to zero within the design so the output buffer is constantly driving to the ground level.

Virtual VCCI

Virtual VCCI is similar to virtual ground. The only difference is that in the case of virtual VCCI, the output buffer is permanently driving to logic HIGH.

In general, there are two shielding methods recommended by Microsemi: a) using GND pins or virtual grounds and b) using any VCCII, GND, VCCI, unused I/O, used (but not sensitive) I/O, or any combination of these pins.

Shielding Using GND or Virtual Ground Pins

When shielding sensitive I/Os from the SSO bus, GND or virtual ground pins can be used if required. In this case, two or three GND or virtual ground pins should be placed on each side of the quiet I/O. The shielding pins should be connected externally to the board-level ground. To prevent any board-level coupling or crosstalk noise on the sensitive I/Os, the shielding pins should be routed on the board alongside the SSO bus for the whole length of the SSO traces and on the same board layer. These shielding traces should be connected to board ground at both ends of their length.

Shielding Using Other Pins

The type of shielding pins is not restricted to GND or virtual grounds. The shielding pins can also be VCCI, VCCII, virtual VCCI, unused I/Os, or used I/Os that are not sensitive to SSO effects (e.g., outputs driving LEDs).

How to Use This Document

The rest of this document is divided based on three different SSO effects: on outputs, on inputs, and on Clock Conditioning Circuits (CCCs). Each section includes tables that identify the recommended maximum number of SSOs and the required shielding if the number of SSOs exceeds the recommendation. The tables are categorized by device/package type (e.g., A3P600-FG484) and I/O configuration of the SSO bus (i.e., drive strength and slew rate). If the desired device/package combination cannot be found in the tables, choose the SSO recommendation for the closest package type and the next smaller die size. The following example describes two scenarios in which the SSO recommendation for another device/package can be used for a member of the ProASIC3/E family:

1. SSO guidelines for A3P250-PQ208 can be used when designing for A3P400-PQ208.
2. SSO guidelines for A3PE600-FG484 can be used when designing for A3PE1500-FG676.

You should study this entire document, consider the desired device/package combination, define the worst-case SSO scenario, and use the SSO guidelines or shielding recommendations described in the tables. At the end of each section, guidelines are given on how to mitigate the effects of SSOs. Note that the data presented in this document is collected at nominal operating conditions (1.5 V core voltage and room temperature). CMOS transistors switch faster when cold, and therefore the edge rates become faster, so SSO effects are usually worse at lower temperatures.

At the end of this document, some general board-level design guidelines are included. Microsemi recommends that you follow these guidelines when designing boards.

SSO Effects on Outputs

This section describes the SSO effects on other outputs. As stated in the "Shielding from SSOs" section on page 3, in ProASIC3 and ProASIC3E devices, the effects of SSOs on quiet outputs are categorized by ground bounce, VCCI bounce, and push-out. The following sections give the characteristics of SSO effects on outputs and provide guidelines on how to mitigate these effects.

Ground and VCCI Bounce

The most widely known effects of SSOs are ground and VCCI bounce. This section characterizes ProASIC3/E ground and VCCI bounce in the presence of SSOs. Since outputs with higher drive strength or faster slew rate source/sink higher current at the time of switching, SSOs are more disruptive when they are configured at higher drive strength and high slew rate. Table 1 on page 5 lists the number of SSOs causing specified levels of ground and VCCI bounce for various device, package, and SSO bus configurations. A disruptive ground bounce is one with a 1.25 V peak and 1 ns width—enough to trigger a high-speed input to change its value from zero to one. Similarly, a disruptive VCCI bounce causes oscillations on the quiet output (driving HIGH) with a magnitude of 2 V and width of 1 ns. These values are chosen based on Microsemi bench experiments using typical CMOS input sensitivity.

Table 1 • **Number of SSOs Causing Specified Ground and VCCI Bounce**

Device	Drive Strength (mA)	Slew Rate	SSOs Causing GND Bounce	SSOs Causing VCCI Bounce
A3P250-PQ208	24	High	4	2
		Low	4	6
	12	High	8	12
		Low	16	16
A3PE600-PQ208	24	High	6	4
		Low	8	8
	12	High	10	12
		Low	14	16
A3PE600-FG484	24	High	24	10
		Low	56	16
	12	High	>64	32
		Low	>64	>64
A3P1000-FG484	24	High	36	12
		Low	>64	26
	16	High	>64	24
		Low	>64	40
	12	High	>64	36
		Low	>64	>64
	8/6/4/2	High	>64	>64
		Low	>64	>64
A3PE1500-FG484	24	High	28	18
		Low	46	28
	16	High	46	26
		Low	>64	>64
	12	High	>64	62
		Low	>64	>64
	8/6/4/2	High	>64	>64
		Low	>64	>64
A3PE/AGLE3000-FG484	24	High	54	24
		Low	>64	42
	16	High	>64	44
		Low	>64	>64
	12	High	>64	>64
		Low	>64	>64
	8/6/4/2	High	>64	>64
		Low	>64	>64

Table 2 • Ground Bounce and Shielding for A3PE3000-FG896

Drive Strength (mA)	Slew Rate	Ground Bounce 5 < SSOs < 10	Ground Bounce SSOs >10	Shielding for 4 < SSOs < 8	Shielding for SSOs > 8
24	High	Negligible	1 ns	0	0
	Low	Negligible	Negligible	0	0
12	High	Negligible	800 ps	0	0
	Low	Negligible	Negligible	0	0
< 8	Any	Negligible	Negligible	0	0

Output Push-Out

As described in the "SSO Effect on Output Delay (push-out)" section on page 2, if an output is surrounded by SSOs, the propagation delay of that output may be increased due to the noise on ground or VCCI. Figure 4 shows a simple diagram of the push-out effect. As shown, the push-out effect occurs only if the affected output toggles at the same time as the SSO bus. If the outputs surrounded by the SSO bus are not switching simultaneously (within 200 ps of each other) with the SSOs, the outputs are not affected by the push-out phenomenon.

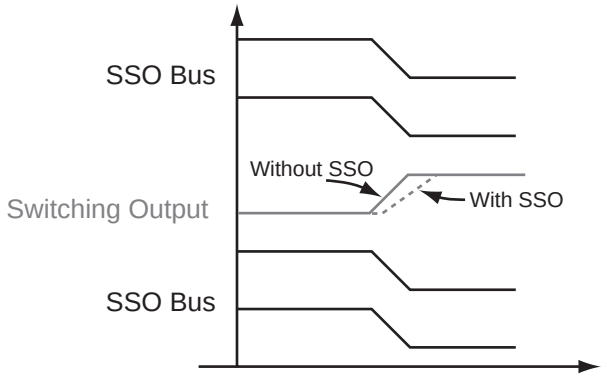


Figure 4 • SSO Push-Out Effect

Table 3 lists the increase in output delay for various SSO widths and configurations.

Table 3 • SSO Push-Out Effect on an Output Surrounded by SSOs

Package	Drive Strength (mA)	Slew Rate	5 < SSOs < 10	SSOs ≥ 10
PQ208	24	High	<1.1 ns	<1.8 ns
		Low	<600 ps	<1.2 ns
	12	High	<900 ps	<1.5 ns
		Low	Negligible	Negligible
	≤8	Any	Negligible	Negligible
FG484	Any	Any	Negligible	Negligible

Notes:

1. *Table data obtained when output load is 30 pF.*
2. *Larger output load increases the push-out effect. As an example, increasing the output load from 30 pF to 50 pF increases the push-out effect by 40%.*

Mitigating SSO Effects on Outputs

Any effort to mitigate the SSO effect starts with eliminating the SSOs themselves. As described in "Introduction" on page 1, the SSOs should be spread across the die pads to avoid a large SSO bus concentrated in one area of the die. If possible, the clock-to-out timing of output busses should be staggered to reduce the number of SSOs in vicinity of sensitive outputs. If placement of sensitive outputs close to an SSO bus is inevitable, such outputs should be shielded from the bus. The shielding scheme to protect delay-sensitive outputs is similar to the guidelines presented in Table 4 on page 8. Whenever shielding is required, it is recommended to use GND or virtual ground pins as shielding. However, it is acceptable to use other shielding pins to protect sensitive outputs from SSOs.

Segmenting SSO busses into smaller sections helps mitigate the SSO effect. The SSO bus can be segmented by inserting spacers among the SSO bus pins when placed on the die pads, as shown in Figure 5. The spacers can be GND or virtual ground, V_{CCI} or virtual V_{CCI}, unused I/O, or used I/Os that are not assigned to sensitive signals and do not toggle frequently or synchronously with the SSOs (e.g., signals driving LEDs).

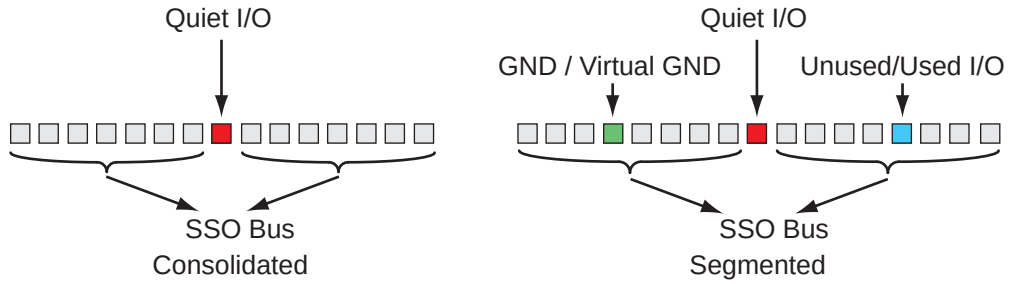


***Figure 5* • Example of Consolidated and Segmented SSO Bus**

Also, as described in Table 1 on page 5 and Table 3, FG and BG packages show much better characteristics with respect to SSO effects than PQ, TQ, or VQ packages. Therefore, for relatively high-speed designs or designs that have a significant number of wide output busses, FG or BG packages are strongly recommended.

In addition to the logic design and device package type, board-level design is a key parameter in mitigating SSO effects. A well-designed PCB, capable of providing clean voltage supplies to the FPGA, is less susceptible to noise and therefore performs better.

Board-Level Timing Analysis with Push-Out

Since the push-out effect changes the clock-to-out timing of the signal surrounded by SSOs, designers should take care when performing board-level timing analysis for such outputs. The following are the Microsemi recommendations for calculating the clock-to-out timing of signals affected by push-out phenomena:

- For board-level setup time calculations:

  Clock-to-out = worst-case clock-to-out reported by SmartTime + push-out delay
- For board-level hold time calculations:

  Clock-to-out = best-case clock-to-out reported by SmartTime

SSO Effects on Inputs

As described in the "Virtual VCCI" section on page 3, if a quiet input is surrounded by SSOs, the logic driven by that input may experience a glitch when the SSO bus is switching. In ProASIC3/E devices in FG or BG packages, the inputs are not affected by an SSO bus. However, in PQ, TQ, and VQ packages, due to larger lead inductance, the SSOs may affect the inputs as described in the "SSO Effect on Inputs" section on page 2 and the "SSO Effect on Minimum Input Slew Rate (input maximum rise/fall time)" section on page 2. Table 4 describes the input shielding required for various SSO sizes with different I/O configurations. For example, in a PQ208 package, if a sensitive input (e.g., asynchronous reset) is

surrounded by an SSO bus configured with 16 mA drive strength and low slew rate, two shielding pins are required on each side of the sensitive input to prevent any logic glitch on the reset line during transition of the SSO bus.

Table 4 • **Shielding Requirement Protecting Inputs from SSO [1]**

Package	Drive Strength (mA)	Slew Rate	Shielding Required [2] for 4 < SSO < 8	Shielding Required [2] for SSO > 8
PQ208	24	High	2	3
		Low	2	2
	16	High	2	3
		Low	2	2
	12	High	0	1
		Low	0	0
	8	Any	0	0
FG484	Any	Any	0	0

Notes:

1. *Measurements were performed with a 3.3 V swing on the SSO bus.*
2. *Shielding pins required on the side of the sensitive input adjacent to the SSO bus.*

In PQ, TQ, and VQ packages, the sensitive inputs may be affected by SSOs as described in the "SSO Effect on Minimum Input Slew Rate (input maximum rise/fall time)" section on page 2. If the edge-sensitive inputs surrounded by an SSO bus rise or fall at the same time as an SSO transition, the maximum rise and fall times of those inputs should be less than 3 ns to avoid any glitches, as described the "SSO Effect on Minimum Input Slew Rate (input maximum rise/fall time)" section on page 2.

Mitigating SSO Effects on Inputs

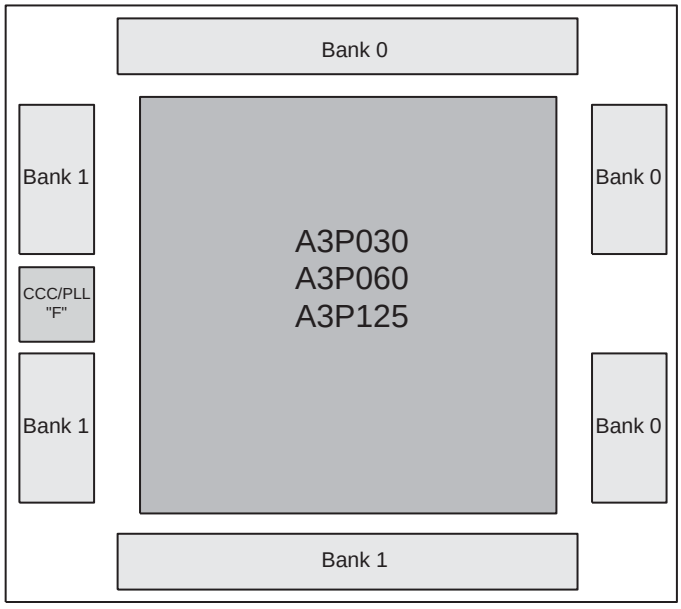
As illustrated in Table 1 on page 5, in PQ, TQ, and VQ packages, inputs may be affected by a surrounding SSO bus, depending on the configuration and number of the SSOs. FG and BG packages show much better SSO characteristics due to smaller lead inductance. Therefore, designers are encouraged to use these packages in designs that have SSOs and are sensitive to noise. It is also recommended that designers use the general guidelines described in "Introduction" on page 1 to eliminate SSO conditions that may cause system signal integrity problems.

In addition, experiments at Microsemi show that in ProASIC3/E devices, inputs configured with the Schmitt Trigger option are slightly more tolerant to the noise induced by an SSO bus. Therefore, Microsemi recommends that designers select the Schmitt Trigger option for critical inputs surrounded by SSOs whenever possible.

Whenever shielding is required by Table 4 on page 8, it is recommended to use GND or virtual ground pins as shielding (described in the "Shielding Using GND or Virtual Ground Pins" section on page 3); however, it is acceptable to use other shielding pins (as described in the "Shielding Using Other Pins" section on page 4) to protect the sensitive inputs from SSOs.

Mitigating SSO Effects on Clock Conditioning Circuits

In general, analog circuitry is more sensitive to noise than digital signals. As described in the "Shielding from SSOs" section on page 3, any sensitive signal surrounded by an SSO bus is affected by the noise induced by SSO activity. Therefore, if the analog power supply of the ProASIC3/E PLL (i.e., the VCCPLX pin) is surrounded by SSOs, the noise induced by the SSOs in the analog supply will cause an increase in the PLL output jitter. Experiments at Microsemi show that if the analog supply pin of the PLL is surrounded by two or more SSOs, the output jitter of the corresponding PLL will be increased beyond the jitter specification in the ProASIC3/E datasheet. Therefore, if PLLs are used in ProASIC3/E devices, the analog supplies of the PLLs used should be shielded from any SSOs by avoiding the placement of SSOs exceeding the guidelines given in Table 1 on page 5. Refer to Figure 6, Figure 7 on page 10, and Figure 8 on page 10 for more information about the I/O bank neighboring the PLL.



Note: The A3P030 device does not support a PLL (V_{COMPLF} and V_{CCPLF} pins).

***Figure 6* • Naming Conventions of ProASIC3 Devices with Two I/O Banks**

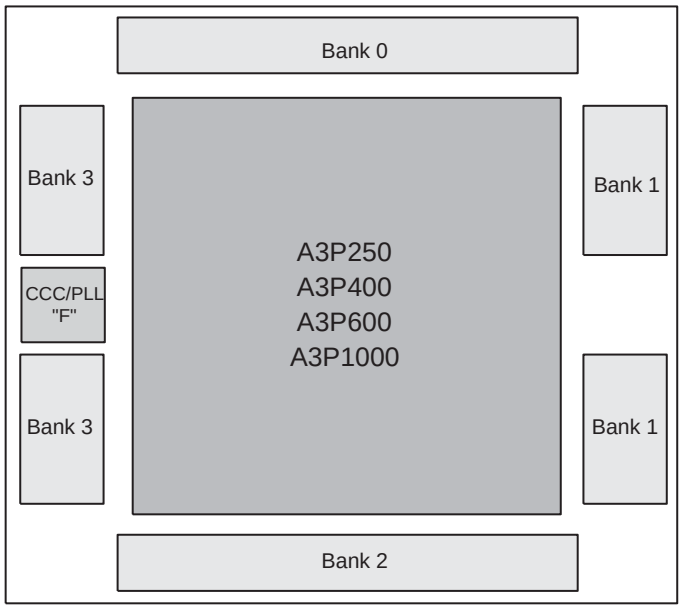


***Figure 7* • Naming Conventions of ProASIC3 Devices with Four I/O Banks**

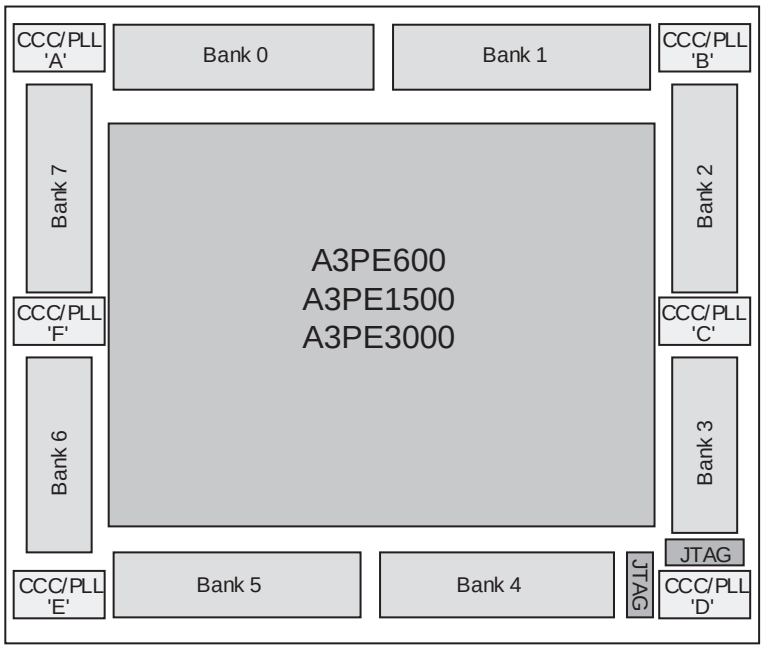


***Figure 8* • User I/O Naming Conventions of ProASIC3E Devices**

Conclusion

As digital designs get faster and larger, SSOs and their effects become a more critical part of system signal integrity analysis. This application note provides data characterizing and predicting the effects of SSOs on sensitive inputs and outputs in ProASIC3/E FPGAs. SSO effects should be mitigated to ensure the functionality of the design; this application note provides specific techniques for doing so.

SSO mitigation techniques should be conducted in parallel with chip-level and board-level design, as they play important roles in providing a clean digital system. For board-level design guidelines, refer to the *Board-Level Considerations* application note.

Due to the nature of SSOs, FG and BG packages are more tolerant to SSO effects than PQ or TQ packages. Therefore, for high-speed designs or designs with large numbers of SSOs, FG and BG packages are strongly recommended.

Related Documents

Application Notes

Simultaneous Switching Noise

http://www.microsemi.com/soc/documents/SSN_AN.pdf

Board-Level Considerations

http://www.microsemi.com/soc/documents/ALL_AC276_AN.pdf

List of Changes

The following table lists critical changes that were made in each revision of the chapter.

Date	Changes	Page
August 2012	The "Mitigating SSO Effects on Clock Conditioning Circuits" section was clarifed, referring to the guidelines given in Table 1 • Number of SSOs Causing Specified Ground and VCCI Bounce if PLLs are used in ProASIC3/E devices. The section previously stated that you should avoid the placement of SSOs in neighboring I/O banks (SAR 33974).	9
	The hyperlink for the *Board-Level Considerations* application note was corrected (SAR 36663).	11
June 2011	Table 1 • Number of SSOs Causing Specified Ground and VCCI Bounce was revised to add information for additional device packages and Table 2 • Ground Bounce and Shielding for A3PE3000-FG896 is new (SAR 31139).	5, 6
v1.0 (January 2008)	Figure 6 • Naming Conventions of ProASIC3 Devices with Two I/O Banks, Figure 7 • Naming Conventions of ProASIC3 Devices with Four I/O Banks, and Figure 8 • User I/O Naming Conventions of ProASIC3E Devices were updated.	9 – 10

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