Low-Power Modes in Actel ProASIC3/E and ProASIC3 nano FPGAs

Introduction

The demand for low-power systems and semiconductors, combined with the strong growth observed for value-based FPGAs, is driving growing demand for low-power FPGAs. For portable and battery-operated applications, power consumption has always been the greatest challenge. The battery life of a system and on-board devices has a direct impact on the success of the product. As a result, FPGAs used in these applications should meet low-power consumption requirements.

Actel ProASIC®3/E and ProASIC3 nano FPGAs offer low power consumption capability inherited from their nonvolatile and live-at-power-up (LAPU) flash technology. This application note describes the power consumption and how to use different power saving modes to further reduce power consumption for power-conscious electronics design.

Power Consumption Overview

In evaluating the power consumption of FPGA technologies, it is important to consider it from a system point of view. Generally, the overall power consumption should be based on static, dynamic, inrush, and configuration power. Few FPGAs implement ways to reduce static power consumption utilizing sleep modes.

SRAM-based FPGAs use volatile memory for their configuration, so the device must be reconfigured after each power-up cycle. Moreover, during this initialization state, the logic could be in an indeterminate state, which might cause inrush current and power spikes. More complex power supplies are required to eliminate potential system power-up failures, resulting in higher costs. For portable electronics requiring frequent power-up and -down cycles, this directly affects battery life, requiring more frequent recharging or replacement.

$$\text{SRAM-Based FPGA Total Power Consumption} = P_{static} + P_{dynamic} + P_{inrush} + P_{config}$$

EQ 1

$$\text{ProASIC3/E Total Power Consumption} = P_{static} + P_{dynamic}$$

EQ 2

Unlike SRAM-based FPGAs, Actel flash-based FPGAs are nonvolatile and do not require power-up configuration. Additionally, Actel nonvolatile flash FPGAs are live at power-up and do not require additional support components. Total power consumption is reduced as the inrush current and configuration power components are eliminated.

Note that the static power component can be reduced in flash FPGAs (such as the ProASIC3/E devices) by entering User Low Static mode or Sleep mode. This leads to an extremely low static power component contribution to the total system power consumption.

The following sections describe the usage of Static (Idle) mode to reduce the power component, User Low Static mode to reduce the static power component, and Sleep mode and Shutdown mode to achieve a range of power consumption when the FPGA or system is idle. summarizes the different low-power modes offered by ProASIC3/E devices.

Table 1 • **ProASIC3/E/nano Low-Power Modes Summary**

Mode	Power Supplies / Clock Status	Needed to Start Up
Active	On – All, clock Off – None	N/A (already active)
Static (Idle)	On – All Off – No active clock in FPGA Optional: Enter User Low Static (Idle) Mode by enabling ULSICC macro to further reduce power consumption by powering down FlashROM.	Initiate clock source. No need to initialize volatile contents.
Sleep	On – V_{CCI} Off – V_{CC} (core voltage), V_{JTAG} (JTAG DC voltage), and V_{PUMP} (programming voltage) LAPU enables immediate operation when power returns. Optional: Save state of volatile contents in external memory.	Need to turn on core. Load states from external memory. As needed, restore volatile contents from external memory.
Shutdown	On – None Off – All power supplies Applicable to all ProASIC3E, all ProASIC3 nano, and the A3P030 and A3P015 devices, cold-sparing and hot-insertion allow the device to be powered down without bringing down the system. LAPU enables immediate operation when power returns.	Need to turn on V_{CC}, V_{CCI}.

Static (Idle) Mode

In Static (Idle) mode, the clock inputs are not switching and the static power consumption is the minimum power required to keep the device powered up. In this mode, I/Os are only drawing the minimum leakage current specified in the datasheet. Also, in Static (Idle) mode, embedded SRAM, I/Os, and registers retain their values, so the device can enter and exit this mode without any penalty.

If the embedded PLLs are used as the clock source, Static (Idle) mode can be entered easily by pulling LOW the PLL POWERDOWN pin (active-low). By pulling the PLL POWERDOWN pin to LOW, the PLL is turned off. Refer to for more information.
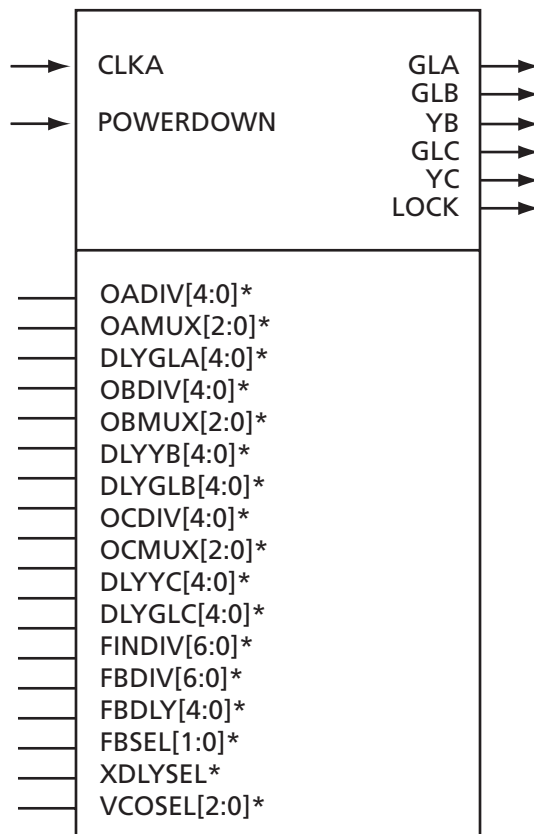
Figure 1 • **CCC/PLL Macro**

User Low Static (Idle) Mode

User Low Static (Idle) mode is an advanced feature supported by ProASIC3/E devices to reduce static (idle) power consumption. Entering and exiting this mode is made possible using the ULSICC macro by setting its value to disable/enable the User Low Static (Idle) mode. Under typical operating conditions, characterization results show up to 25% reduction of the static (idle) power consumption. The greatest power savings in terms of percentage are seen in the smaller members of the ProASIC3 family. The active-high control signal for User Low Static (Idle) mode can be generated by internal or external logic. When the device is operating in User Low Static (Idle) mode, FlashROM functionality is temporarily disabled to save power. If FlashROM functionality is needed, the device can exit User Low Static mode temporarily and re-enter the mode once the functionality is no longer needed.

To utilize User Low Static (Idle) mode, simply instantiate the ULSICC macro (Table 2 on page 4) in your design, and connect the input port to either an internal logic signal or a device package pin, as illustrated in Figure 2 on page 4 or Figure 3 on page 5, respectively. The attribute is used so the Synplify® synthesis tool will not optimize the instance with no output port.

This mode can be used to lower standard static (idle) power consumption when the FlashROM feature is not needed. Configuring the device to enter User Low Static (Idle) mode is beneficial when the FPGA enters and exits static mode frequently and lowering power consumption as much as possible is desired. The device is still functional, and data is retained in this state so the device can enter and exit this mode quickly, resulting in reduced total power consumption. The device can also stay in User Low Static mode when the FlashROM feature is not used in the device.

Table 2 • **Using ULSICC Macro***

VHDL	Verilog

```COMPONENT ULSICC   port (LSICC   : in   STD_ULOGIC); END COMPONENT;```
 	
Example:
 	
```COMPONENT ULSICC   port (LSICC   : in   STD_ULOGIC); END COMPONENT; attribute syn_noprune : boolean; attribute syn_noprune of u1 : label is true; u1: ULSICC port map(myInputSignal);```
	```module ULSICC(LSICC); input LSICC; endmodule```
	
	Example:
	
	```ULSICC U1(.LSICC(myInputSignal)) /* synthesis syn_noprune=1 */;```

* *Supported in Libero IDE v7.2 and newer versions.*
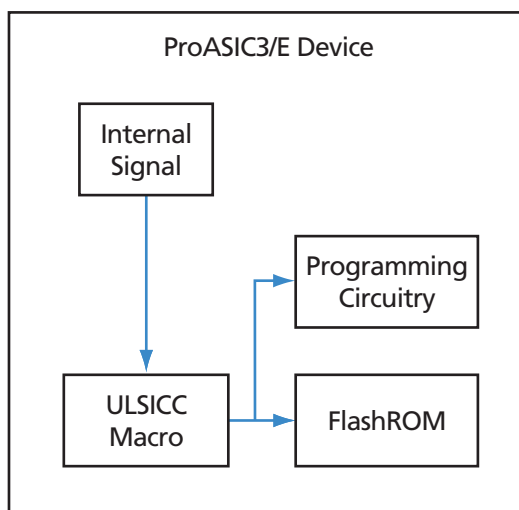
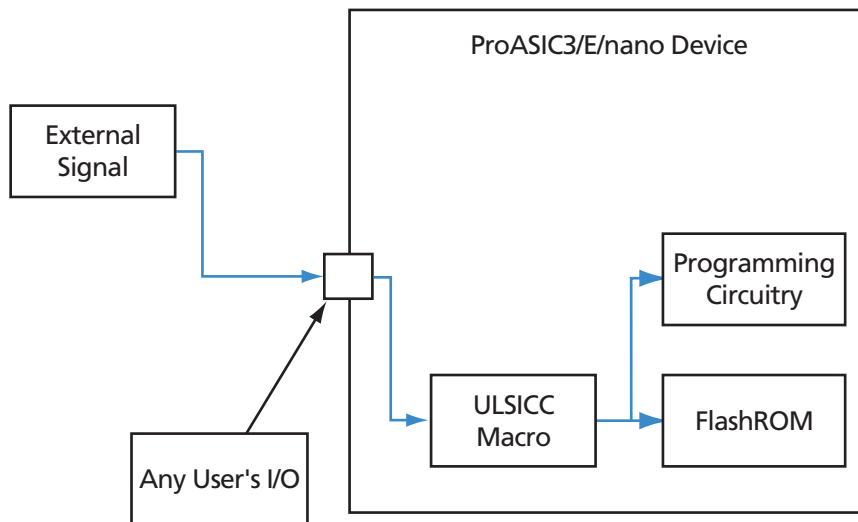*Figure 2 •* **User Low Static (Idle) Mode Application—Internal Control Signal**

Figure 3 • **User Low Static (Idle) Mode Application—External Control Signal**
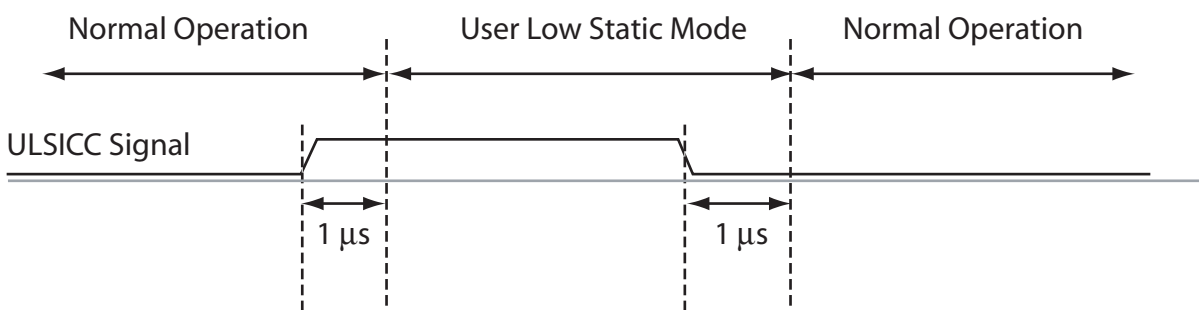

Figure 4 • **User Low Static (Idle) Mode Timing Diagram**

Sleep Mode

Actel ProASIC3/E and ProASIC3 nano FPGAs support Sleep mode when device functionality is not required. In Sleep mode, the V_{CC} (core voltage), V_{JTAG} (JTAG DC voltage), and V_{PUMP} (programming voltage) are grounded, resulting in the FPGA core being turned off to reduce power consumption. While the ProASIC3/E device is in Sleep mode, the rest of the system is still operating and driving the input buffers of the ProASIC3/E device. The driven inputs do not pull up power planes, and the current draw is limited to a minimal leakage current.

Table 3 shows the status of the power supplies in Sleep mode. When a power supply is powered off, the corresponding power pin can be left floating or grounded.

Table 3 • **Sleep Mode—Power Supply Requirements for ProASIC3/E/nano Devices**

Power Supplies	ProASIC3/E/nano Device
V_{CC}	Powered off
V_{CCI} = VMV	Powered on
V_{JTAG}	Powered off
V_{PUMP}	Powered off

Table 4 shows the current draw in Sleep mode for an A3P250 device with the following test conditions: V_{CCI} = VMV; V_{CC} = V_{JTAG} = V_{PUMP} = GND.

Table 4 • **A3P250 Current Draw in Sleep Mode**

Typical Conditions	A3P250	
	I_{CCI} (μA)	I_{CCI} (μA) per Bank
V_{CCI} = 3.3 V	31.57	7.89
V_{CCI} = 2.5 V	23.96	5.99
V_{CCI} = 1.8 V	17.32	4.33
V_{CCI} = 1.5 V	14.46	3.62
I_{CC} FPGA Core	0.0	0.0
Leakage Current per I/O	0.1	0.1
V_{PUMP}	0.0	0.0

Note: The data in this table were taken under typical conditions and are based on characterization. The data is not guaranteed.

Table 5 shows the current draw in Sleep mode for an A3PE600 device with the following test conditions: V_{CCI} = VMV; V_{CC} = V_{JTAG} = V_{PUMP} = GND.

Table 5 • **A3PE600 Current Draw in Sleep Mode**

Typical Conditions	A3PE600	
	I_{CCI} (μA)	I_{CCI} (μA) per Bank
V_{CCI} = 3.3 V	59.85	7.48
V_{CCI} = 2.5 V	45.50	5.69
V_{CCI} = 1.8 V	32.98	4.12
V_{CCI} = 1.5 V	27.66	3.46
V_{CCI} = 0 V or Floating	0.0	0.0
I_{CC} FPGA Core	0.0	0.0
Leakage Current per I/O	0.1	0.1
I_{PUMP}	0.0	0.0

Note: The data in this table were taken under typical conditions and are based on characterization. The data is not guaranteed.

ProASIC3/E and ProASIC3 nano devices were designed such that before device power-up, all I/Os are in tristate mode. The I/Os will remain tristated during power-up until the last voltage supply (V_{CC} or V_{CCI}) is powered to its functional level. After the last supply reaches the functional level, the outputs will exit the tristate mode and drive the logic at the input of the output buffer. The behavior of user I/Os is independent of the V_{CC} and V_{CCI} sequence or the state of other FPGA voltage supplies (V_{PUMP} and V_{JTAG}). During power-down, device I/Os become tristated once the first power supply (V_{CC} or V_{CCI}) drops below its brownout voltage level. The I/O behavior during power-down is also independent of voltage supply sequencing.

Figure 5 on page 7 shows a timing diagram for the FPGA core entering the activation and deactivation trip points for a typical application when the V_{CC} power supply ramp rate is 100 μs (ramping from 0 V to 1.5 V). This is, in fact, the timing diagram for the FPGA entering and exiting Sleep mode, as it is dependent on powering down or powering up V_{CC}. Depending on the ramp rate of the power supply and board-level configurations, the user can easily calculate how long it takes for the core to become active or inactive. For more information, refer to the *Power-Up/-Down Behavior of Low-Power Flash Devices* application note.
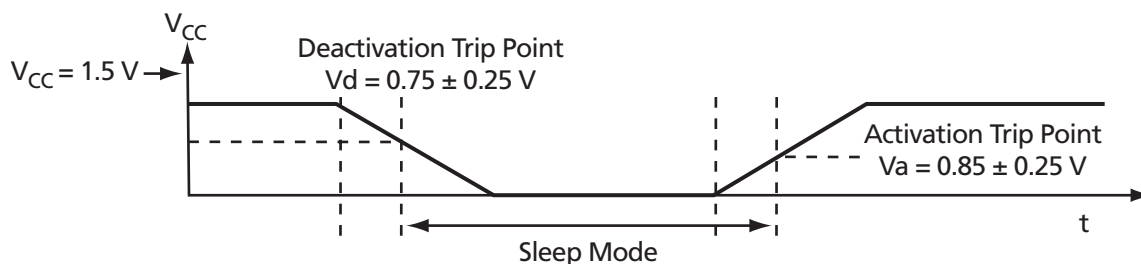
Figure 5 • **Entering and Exiting Sleep Mode—Typical Timing Diagram**

Shutdown Mode

For all ProASIC3E, all ProASIC3 nano, and the A3P030 and A3P015 devices, shutdown mode can be entered by turning off all power supplies when device functionality is not needed. Cold-sparing and hot-insertion features enable the device to be powered down without turning off the entire system. When power returns, the live at power-up feature enables immediate operation of the device.

Using Sleep Mode or Shutdown Mode in the System

Depending on the power supply and components used in an application, there are many ways to turn the power supplies connected to the device on or off. For example, Figure 6 shows how a microprocessor is used to control a power FET. It is recommended that power FETs with low on resistance be used to perform the switching action.
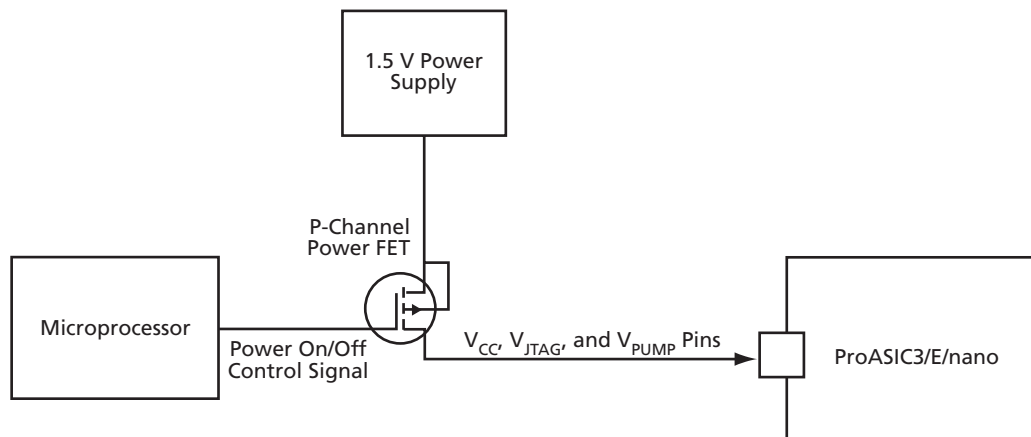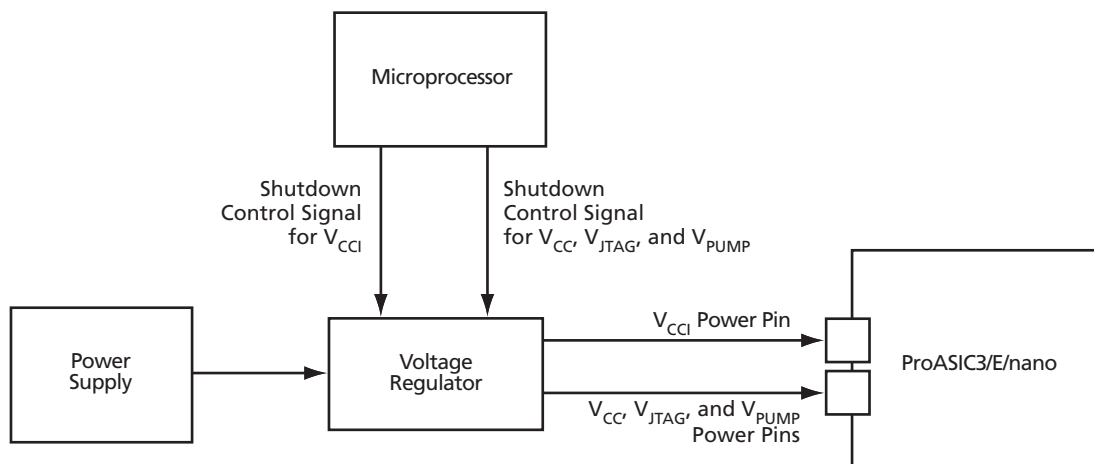

Figure 6 • **Controlling Power On/Off State Using Microprocessor and Power FET**

Alternatively, Figure 7 shows how a microprocessor can be used with a voltage regulator's shutdown pin to turn the power supplies connected to the device on or off.

Figure 7 • **Controlling Power On/Off State Using Microprocessor and Voltage Regulator**

Though Sleep mode or Shutdown mode can be used to save power, the content of the SRAM and the state of the registers is lost when power is turned off if no other measure is taken. To keep the original contents of the device, a low-cost external serial EEPROM can be used to save and restore the device contents when entering and exiting Sleep mode. In the *Embedded SRAM Initialization Using External Serial EEPROM* application note, detailed information and a reference design are provided to initialize the embedded SRAM using an external serial EEPROM. The user can easily customize the reference design to save and restore the FPGA state when entering and exiting Sleep mode. The microcontroller will need to manage this activity, so before powering down V_{CC}, the data must be read from the FPGA and stored externally. Similarly, after the FPGA is powered up, the microcontroller must allow the FPGA to load the data from external memory and restore its original state.

Conclusion

Actel ProASIC3/E and ProASIC3 nano FPGAs inherit low-power consumption capability from their nonvolatile and live-at-power-up flash-based technology. Power consumption can be reduced further using the Static (Idle), User Low Static (Idle), Sleep, or Shutdown power modes. All these features result in a low-power, cost-effective, single-chip solution designed specifically for power-sensitive electronics applications.

Related Documents

Application Notes

Power-Up/Down Behavior of Low-Power Flash Devices

http://www.actel.com/documents/LPD_PowerUp_HBs.pdf

Embedded SRAM Initialization Using External Serial EEPROM

http://www.actel.com/documents/EmbeddedSRAMInit_AN.pdf

Handbook Documents

SRAM and FIFO Memories in Actel's in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_SRAMFIFO_HBs.pdf

Part Number and Revision Date

This document was previously published as an application note describing features and functions of the device, and as such has now been incorporated into the device handbook format. No technical changes have been made to the content.

Part Number 51700094-003-2

Revised August 2009

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (February 2008)	References to ProASIC3 nano devices were added to the document where appropriate.	N/A
	V_{JTAG} and V_{PUMP} were noted as "Off" in the Sleep Mode section of Table 1 • ProASIC3/E/nano Low-Power Modes Summary.	2
	The "Sleep Mode" section, including Table 3 · Sleep Mode—Power Supply Requirements for ProASIC3/E/nano Devices, was revised to state that V_{JTAG} and V_{PUMP} are powered off during Sleep mode.	5
	The text above Table 4 • A3P250 Current Draw in Sleep Mode and Table 5 • A3PE600 Current Draw in Sleep Mode was revised to state "$V_{CC} = V_{JTAG} = V_{PUMP} = GND$."	6
	Figure 6 · Controlling Power On/Off State Using Microprocessor and Power FET and Figure 7 · Controlling Power On/Off State Using Microprocessor and Voltage Regulator were revised to show shutdown of V_{JTAG} and V_{PUMP} during Sleep mode.	7, 8
v1.0 (January 2008)	The part number for this document was changed from 51700094-002-0 to 51700094-003-1.	N/A
51900138-2/10.06	The Power Supplies / Clock Status description was updated for Static (Idle) in Table 1 · ProASIC3/E/nano Low-Power Modes Summary.	2
	Programming information was updated in the "User Low Static (Idle) Mode" section.	3
51900138-1/6.06	The "User Low Static (Idle) Mode" section was updated to include information about allowing programming in the ULSICC mode.	3
	Figure 2 · User Low Static (Idle) Mode Application—Internal Control Signal was updated.	4
	Figure 3 · User Low Static (Idle) Mode Application—External Control Signal was updated.	5
51900138-0/6.05	In Table 4 · A3P250 Current Draw in Sleep Mode, "$V_{CCI} = 1.5 V$" was changed from 3.6158 to 3.62.	6
	In Table 5 · A3PE600 Current Draw in Sleep Mode, "$V_{CCI} = 2.5 V$" was changed from 5.6875 to 3.69.	6