Implementing an OLED Controller Parallel Interface
Using IGLOO or ProASIC3 FPGAs Design Example

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General Description

This document describes a design that enables Microsemi®'s low-power FPGAs to interface with an organic light emitting diode (OLED) display.

The FPGA used in this design example belongs to Microsemi's low-power, reprogrammable IGLOO® family of FPGAs. The design is tested and verified on the IGLOO Icicle Kit Rev. B with Microsemi's AGL125-QNG132 device, using OSRAM's green organic LED module with parallel interface, OSRAM part number OS096016PP08MG1B10. This display module supports a display resolution of 96 columns × 16 rows and the 0.8 inch OLED display has pixels of size 0.22 mm × 0.22 mm with a viewing angle of 180 degrees. The combination of a low-power Microsemi IGLOO device and a small form factor organic LED graphical display is well-suited for low-power, portable applications.

This design enables you to display any image with a pixel size of 128×16. This application note explains how true text characters can be displayed with the help of the design. The interface logic accepts data through a UART, so can be easily adapted for use in a microprocessor-based system.

The accompanying application software, which runs on a PC, prompts you to choose the input type: image or text. Images of size 128×16 can be loaded with the image option. You can also type in your own text characters in text input mode. The first 42 characters appear on the display. If the number of characters entered is less than 42, the trailing pixels display as blank.

Design Description

The top-level block diagram of the IP is shown in Figure 1.

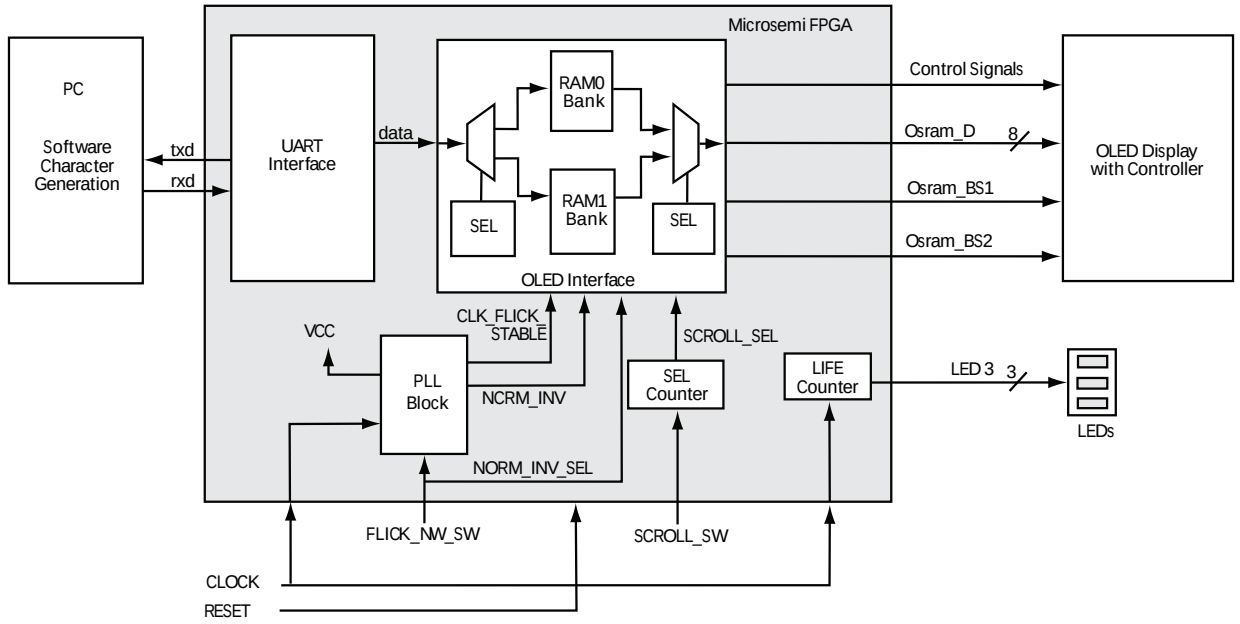

***Figure 1* • Top-Level Block Diagram**

Pixel creation is done using the software application provided along with this design example.

When the image or text is converted into pixels, it is sent to the Icicle board through the USB interface. An on-board USB-to-UART converter IC converts the data from a PC or laptop into UART format and feeds the UART core within the FPGA.

The data received at the UART interface is stored in two banks of internal RAM, FRBank0 and FRBank1, within the FPGA. The logic within the FPGA reads back the content and transfers this pixel information to the OLED, along with the necessary control signals. The current design uses the parallel interface to the display. All the initialization values are coded into the state machine and accessed after a board reset.

The OLED display has two graphic RAM banks on it. The graphics RAM in this document is designated GBank0 and GBank1. GBank0 contains the content for the upper 8 rows of the display and GBank1 contains the content for the lower 8 rows. The display can show only 96 columns at a time, but the graphics RAM can hold data for 128 columns. Columns 97 through 128 can be used for scrolling text or images.

> **Note**: Although each bank of OLED RAM supports 132 columns, the SSD0303 horizontal scroll is designed for 128 columns scrolling. The 4 remaining columns are reserved for computation and should be left blank.

During the initialization process, all 128 columns for both the graphics RAM banks are filled with zeros.

The data coming from the UART initially fills the internal RAM banks of the FPGA. Upon receiving 128 columns of information, the content is uploaded to the graphics RAM of the OLED and then data is displayed.

The display content can be refreshed with new content by resetting the board and then downloading the fresh content to the board.

Files for this design example can be downloaded from the Microsemi website: www.microsemi.com/download/rsc/?f=OLED_Design_DF.

The FPGA design is done using VHDL and the major design blocks are explained below.

Top Level (icicle_top.vhd)

The top-level block integrates all the lower level blocks in the hierarchy. It contains the following:

1. A PLL block to generate the required clocks for the logic from the external 20 MHz oscillator
2. CoreUART IP for interfacing with the external UART of the USB-to-UART chip. This design uses CoreUART version 3.1.103 with the default configuration options.
3. The state machine that generates the OLED side control signals
4. A counter interfaced to the on-board LEDs, to indicate the heartbeat pulse

Microsemi's PLL is used to derive the 1 MHz slow clock from the 20 MHz on-board clock source. Divider logic is used to generate a still slower clock of 125 KHz. The 125 KHz clock (CLK_OUT) is selected for flickering on the display, and the 20 MHz clock (CLOCK) is selected for the stable display modes.

Interface Description

The external interfaces of the OLED Interface design example are listed in Table 1.

Table 1 • **External Interface Descriptions**

Signal	Direction	FPGA Pin	Description
CLOCK	Input	A5	20 MHz input clock to the FPGA
RESET	Input	C1	Active low reset signal from SW1 push-button present on board
RXD	Input	C31	RS232 input from PC
TXD	Output	B34	RS232 output to PC
OSRAM_D[7]	Bidirectional	B40	Data line of OLED
OSRAM_D[6]	Bidirectional	C35	Data line of OLED
OSRAM_D[5]	Bidirectional	A41	Data line of OLED
OSRAM_D[4]	Bidirectional	A40	Data line of OLED
OSRAM_D[3]	Bidirectional	C29	Data line of OLED
OSRAM_D[2]	Bidirectional	B19	Data line of OLED
OSRAM_D[1]	Bidirectional	B18	Data line of OLED
OSRAM_D[0]	Bidirectional	C15	Data line of OLED
OSRAM_BS1	Output	A45	Interface Selection Pin 1: Logic '1' for 8080 parallel interface
OSRAM_BS2	Output	A47	Interface Selection Pin 2: Logic '1' for 8080 parallel interface
OSRAM_RESn	Output	A38	Active low OLED reset signal
OSRAM_CSn	Output	B35	Active low OLED chip select signal
OSRAM_D_C	Output	B43	HIGH = Bus contains data for DDRAM LOW = Bus contains command

Table 1 • **External Interface Descriptions**

OSRAM_R_W	Output	C39	Read/write selector for 68 series; write strobe for 80 series
OSRAM_E_RD	Output	A48	E Clock for 68 series; RD strobe for 80 series
FLICK_INV_SW	Input	C9	Active high reset signal from SW4 push-button present on board
SCROLL_SW	Input	A13	Active high reset signal from SW5 push-button present on board

Utilization Details

This design was verified in the IGLOO AGL125V5-QNG132 but can be instantiated in other IGLOO and ProASIC®3 devices that contain the minimum required resources. The following device utilization values are for the AGL125V5-QNG132 device:

Table 2 • **Device Utilization Values for AGL125V5-QNG132**

Resource	Used/Total	Percentage
Core	949/3072	30.89%
Global (chip plus quadrant)	4/18	38.10%
PLL	1/1	100%
RAM/FIFO	2/8	25%

Software Interface and Design Details

The software for testing the design example is in C on a Windows® platform. The software is run from a PC with the IGLOO Icicle Kit interfaced via a USB port on the PC. The software program is used to send ASCII characters and BMP images to the OLED. The program can display up to 42 characters at once on the display. The input image should be in bitmap format having a size of 128x16 with 8 bits per pixel.

Program Execution (LCD.exe)

The executable program is run from a Windows environment. After the program runs, menu options are displayed.

Select the communication port corresponding to the USB port where the IGLOO Icicle Kit is connected. Select data format 1 for image and 2 for character.

Image Display

If the image option is selected, specify the name of the BMP image. The software verifies whether the attributes of the image are compatible for display on the OLED. The program can support only BMP files of 128x16 (width × height) with a depth of 8 bits per pixel. If the BMP file satisfies the conditions, the image is displayed on the OLED.

Character Display

If the character option is selected, the program prompts you to enter the ASCII characters to be displayed on the OLED. The program has support for all 95 ASCII characters that can be entered from the keyboard. The OLED can display a maximum of 42 characters at a time. When the characters are entered, they are sent to the OLED.

Program Source

The program is written in C using Visual C++ compiler v6.0. The source files are listed below.

Dex_Main.c

This file provides the main functionality of the program. User interaction, BMP image validation, and communication with the USB port are done inside this file. User input is validated and send to the USB port sequentially.

UsbCom.c

This source file takes care of USB communication.

Char_Map.h

The pixel map for the characters (font) is defined in this file. There are definitions for 95 characters, which can be entered from the keyboard in this file.

Dex_Bmp.h

This file contains definitions for the BMP file format.

LCD.dsp

This is the Visual C++ 6.0 project file for the OLED project.

Testing Scheme

This design is tested and verified on the IGLOO Icicle Kit. Download and extract the design files to your local machine. Connect the Icicle board to the PC or laptop with a USB cable. Install the application. The setup should look similar to Figure 2.

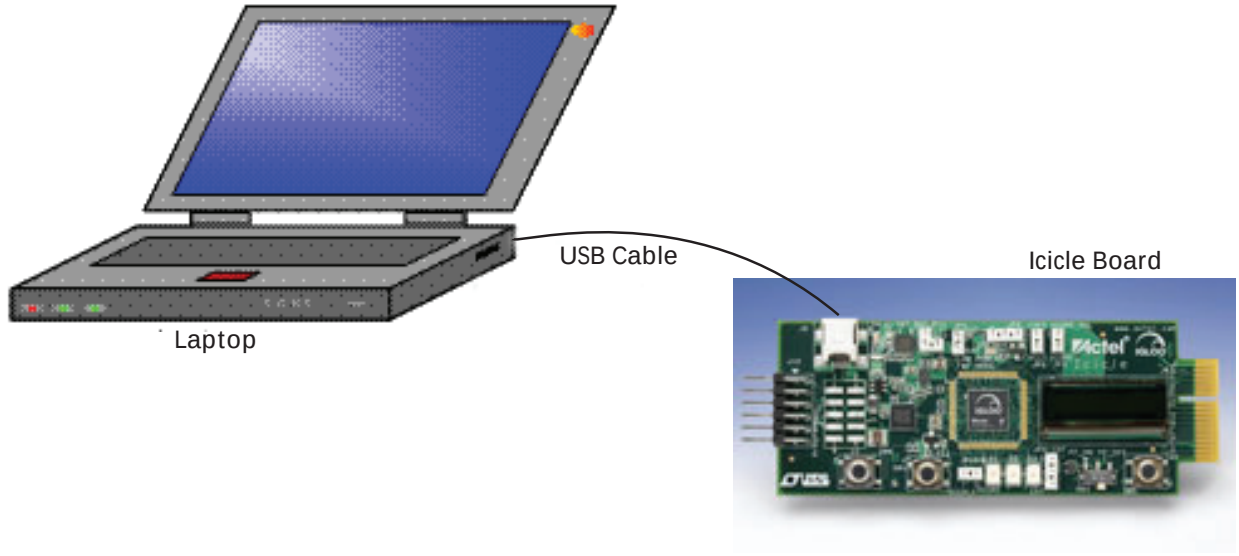

***Figure 2* • Icicle Board Interface**

For the subsequent sections of this document, it is assumed that you are familiar with the Microsemi FPGA design flow.

Running the Demo

Finding the COM Port

Before running any demos, program the Icicle board with the included *.stp file located in the programming_files directory.

Note: These instructions are for Rev. B with green OLED only. Rev. D has a different OLED display interface and will not work for this demo.

Connect the programming stick and both USB cables to the board according to the board's documentation.

Once the Icicle board is programmed and connected to the PC or laptop, configure the COM port. The COM port number can be determined from the Windows Control Panel.

Click **Start** > **Settings** > **Control Panel** > **System** > **Hardware** > **Device Manager** > **Ports**. In Figure 3, the Icicle Board is connected to the USB port, which is detected by the PC as COM3.

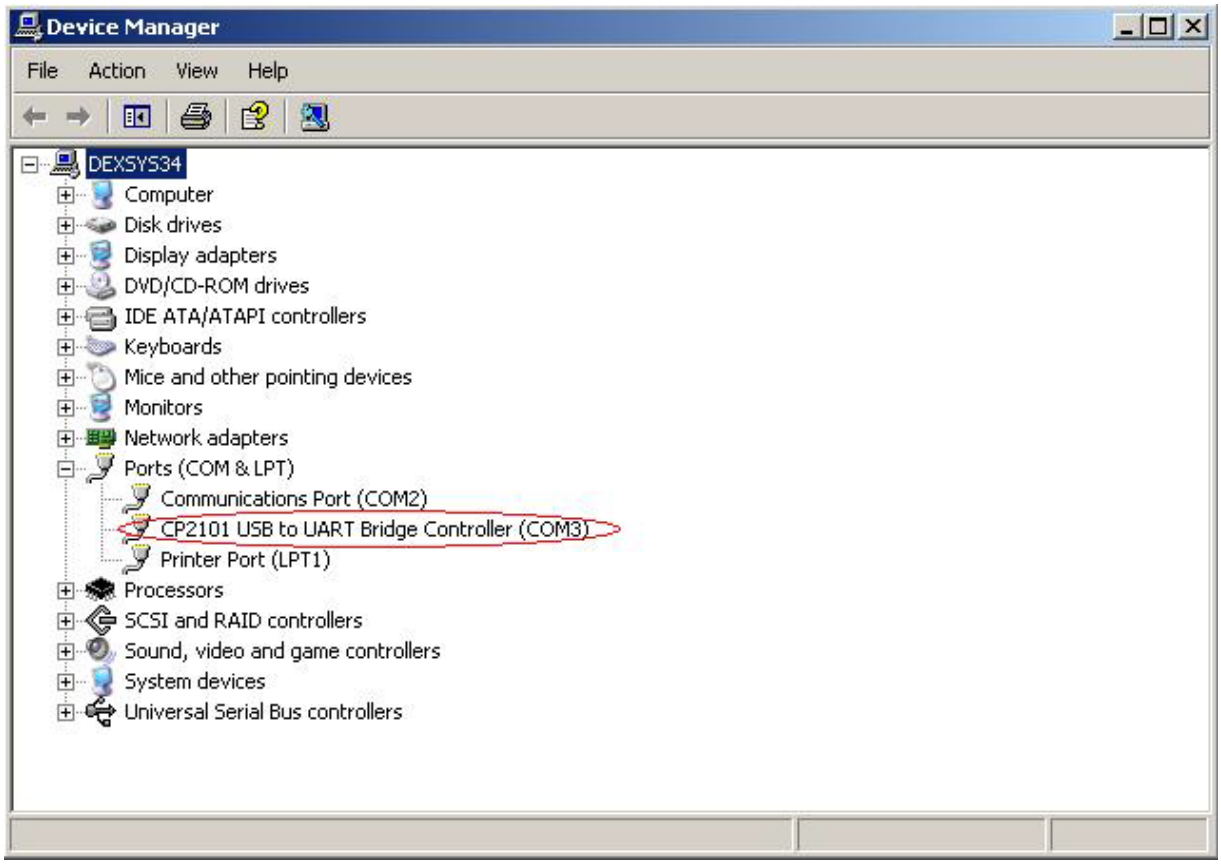

***Figure 3* • COM Port Identification**

Once the LCD.exe application program is executed, the following screen appears on the PC or laptop monitor (Figure 4).

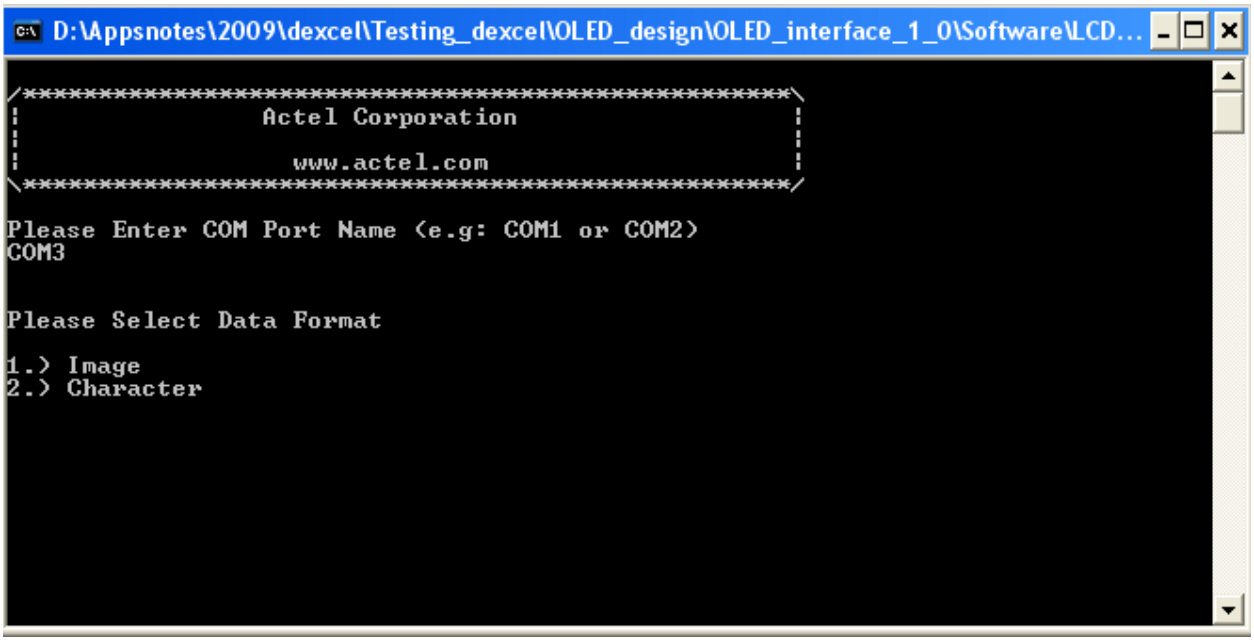

***Figure 4* • Entering the COM Port**

Enter the COM port name found in Device Manager. In this example, assume it is COM3.

Once the COM port is specified, the screen shown in Figure 5 appears.

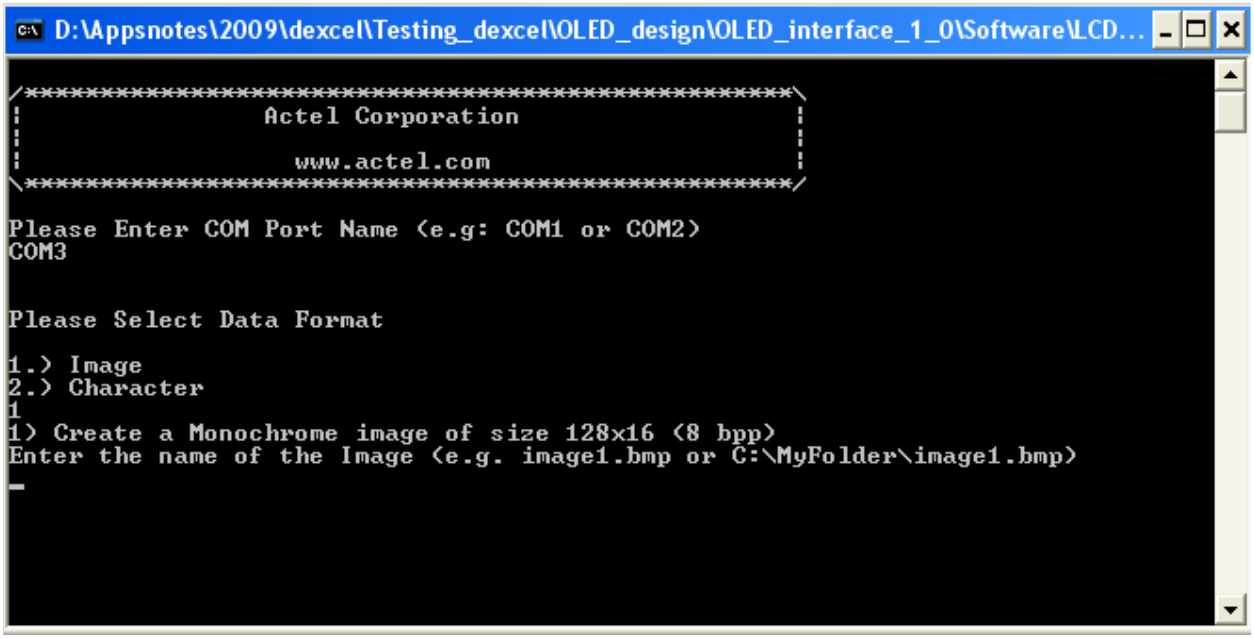

***Figure 5* • Input Data Format Selection**

Press Reset (SW1) on the Icicle board before loading a new image or character string.

Enter 1 for image format or 2 for character format.

The program asks for the name of the image if the image format is selected (examples of answers: image1.bmp or C:\MyFolder\image1.bmp). The program can support only BMP files of dimensions 128×16 (width × height) with a depth of 8 bits per pixel. If the BMP file satisfies the conditions, the image is displayed on the OLED with the computer screen, as shown in Figure 6.

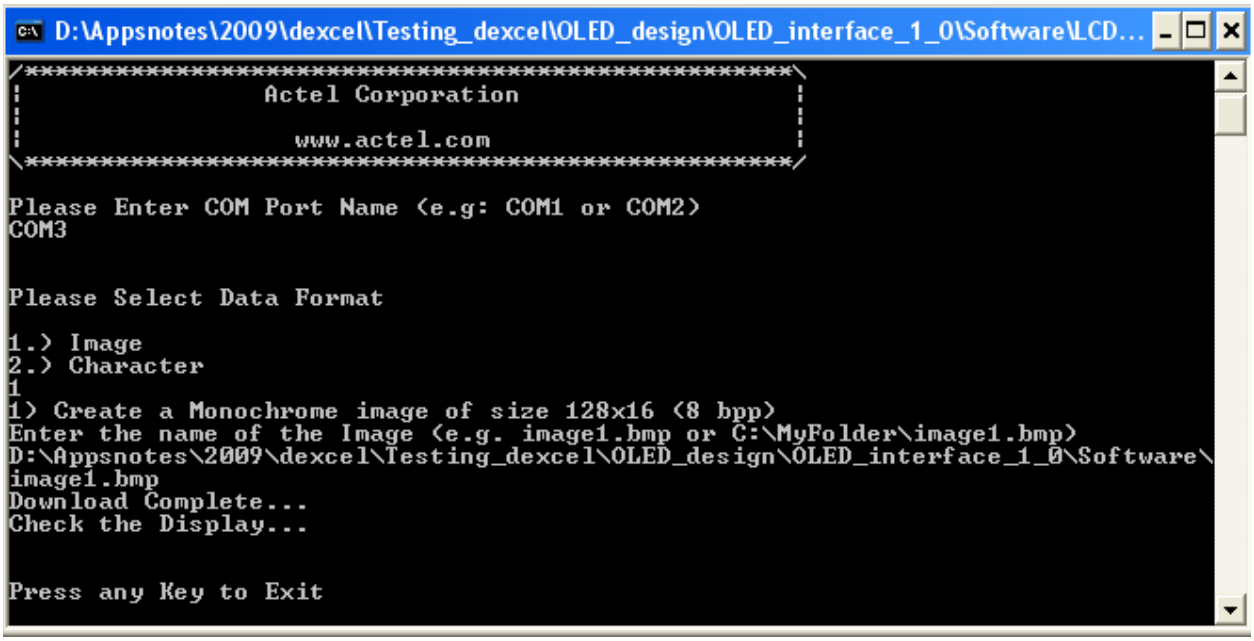

***Figure 6* • Data Being Downloaded**

Similarly, if character format is selected, enter the characters after the command prompt, and they will be displayed on the OLED after pressing <Enter>. You will have to press the Reset button in between subsequent image or character displays.

Display Options

Once a character string or image is displayed on the Icicle board, you can make the image flicker, invert colors, or scroll, by using SW4 and SW5 as follows:

- Pressing SW4 causes the contents of the display to flicker. On pressing it again, it inverts the color of the content (black becomes green and green becomes black). On pressing SW4 again, the inverted image flickers. On pressing again, it inverts the image back to the original color.
- Pressing SW5 scrolls the display and inhibits any other activity except reset. Pressing SW5 again freezes the scrolling display. On pressing SW5 again, the display starts scrolling from the first character.
- SW1 is the reset switch. On pressing this, the device is reset and the display goes blank until another image or character string is loaded.

Timing Diagram

Figure 7 shows the system timing diagram. Table 3 defines the signals.

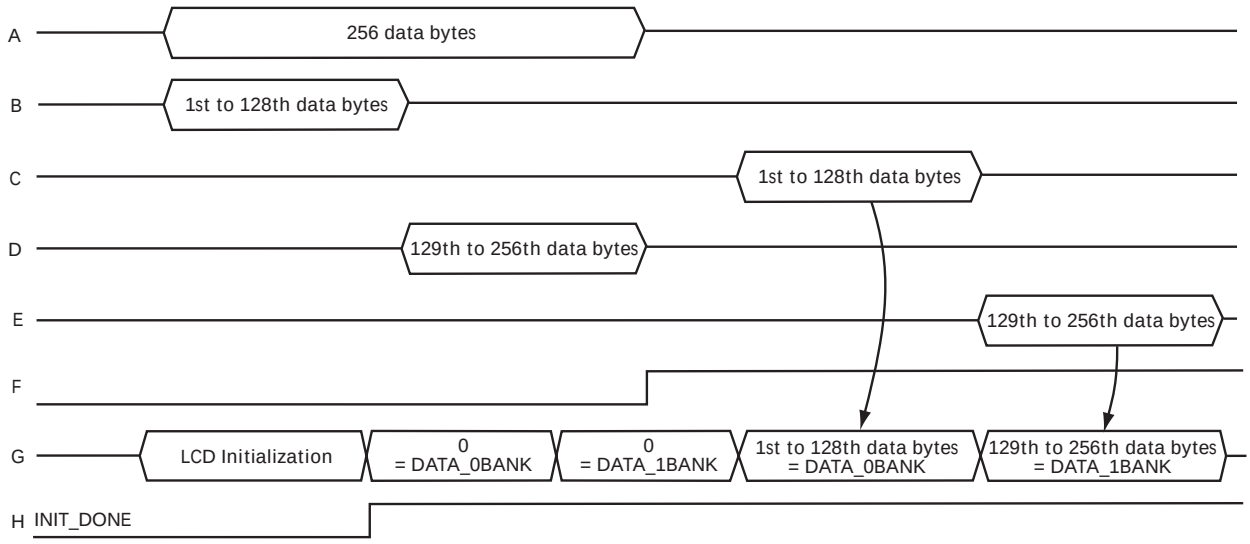

***Figure 7* • Timing Diagram of the System**

***Table 3* • Signal Descriptions**

Signal	Description
A	256 Data bytes from UART
B	128 bytes of Write data for FRBank0
C	128 bytes of read back data from FRBank0 going to data lines of OLED
D	128 bytes of Write data for FRBank1
E	128 bytes of read back data from FRBank1 going to data lines of OLED
F	Shows that writing data in both the RAMs (FRBank0, FRBank1) is over
G	Shows the data lines of OLED. At the time of initialization, GRAM of OLED filled with 0s, and then by FRBank0 data and then FRBank1 data.
H	INIT_DONE signal goes high when the initialization process is completed.

Conclusion

This design, used with the Icicle board, becomes a demonstration display platform for hand held devices and measuring equipment. The software application source code and the VHDL hardware design can be easily modified for supporting different sized displays of a similar nature.

List of changes

Date	Changes	Page
Revision 2 (July 2015)	Non-technical Updates.	NA
Revision 1 (April 2009)	Initial Release.	NA

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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