42MX Family Devices Power-Up Behavior

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Purpose

This application note describes the 42MX Family device power-up characterization. It also explains the transient current on V_{CCA} and functional voltage level during power-up.

Introduction

Microsemi antifuse field-programmable gate array (FPGA) families offer the advantage of non-volatility by attaining immediate functionality during power-up. As the programmed design is retained, there is no requirement for additional configuration devices. This application note describes the results of the 42MX device power-up characterization in detail and recommends appropriate power-up sequences and ramp-rates. Tristate behavior of the device I/Os during the power-up cycle offers the flexibility of applying voltages to the I/Os during power-up.

The characterization measurement is performed in a laboratory environment and the reported data is typical. Therefore, the maximum and minimum values under best and worst conditions are not guaranteed.

All the 42MX devices have two power supplies namely: V_{CCA} and V_{CCI}. They can operate in 5 V only, 3.3 V only, and 5 V / 3.3 V mixed systems. Table 1 shows the voltage levels of these power supplies and corresponding I/O voltage level.

Table 1 • **Power Supply Levels for Different Operations**

V_{CCA}	V_{CCI}	Input	Output
5 V	5 V	5 V	5 V
3.3 V	3.3 V	3.3 V	3.3 V
5 V	3.3 V	3.3 V, 5 V	3.3 V

As shown in Table 1, V_{CCA} also acts as an input tolerance voltage while V_{CCI} is used as an I/O module voltage. In single voltage operations, V_{CCA} and V_{CCI} are usually tied to each other, but for the mixed 5 V / 3.3 V systems (V_{CCA} = 5 V and V_{CCI} = 3.3 V), $V_{CCA} \geq V_{CCI}$ throughout the power-up sequence. Therefore, V_{CCA} must always be powered up before V_{CCI} to avoid excessive currents and/ or damage to the device.

If V_{CCI} is 0.5 V greater than V_{CCA} when both are above 1.5 V, the input protection junction on the I/Os is forward biased, causing them to draw large amounts of current. When V_{CCA} and V_{CCI} are in the 1.5 -2.0 V region, and $V_{CCI} > V_{CCA}$, all I/Os momentarily behave as outputs that are in a logical high state, and I_{CC} rises to high levels.

The A42MX24 and A42MX36 devices contain an internal power-on reset (POR) circuitry used to reset the JTAG state machine. Microsemi recommends that V_{CCA} is monotonic so that the POR can issue a proper JTAG reset. If V_{CCA} is not monotonic, the internal JTAG POR may not operate as expected. In this case, the device may enter in to a JTAG test mode after power-up instead of normal operation mode. The JTAG state machine can be reset externally using any of the following methods:

- After power-up, issue at least five TCK cycles with TMS pulled high.
- If JTAG is not used in the design, JTAG can be permanently disabled by clearing the check box for the **Reserve JTAG** pin option in Designer. This causes the JTAG state machine to remain in an asynchronous reset state, bypassing the POR. However, in this case the JTAG circuitry is permanently disabled and JTAG testing cannot be performed on the device.

Transient Current

Due to the simultaneous random logic switching activity during power-up, a relatively large transient current may appear on the core supply (V_{CCA}). The amount and duration of the transient current depends on the V_{CCA} voltage level (3.3 V or 5 V) and its ramp-rate during power-up. As the transient current is not due to I/O switching, its value and duration are independent of the V_{CCI} level.

Transient current is measured under the following operating conditions:

- 5 V only— $V_{CCA} = V_{CCI} = 5$ V
- 3.3 V only— $V_{CCA} = V_{CCI} = 3.3$ V
- Mixed 5 V / 3.3 V— $V_{CCA} = 5$ V (powered up first), $V_{CCI} = 3.3$ V (powered up second)

Different ramp-rates have been applied to the power supplies. Additionally, in the mixed-voltage operating conditions, different delays between V_{CCA} and V_{CCI} have been tested, ranging from 100 µs to 250 ms. Table 2 indicates the amount of the transient current peak in single-voltage operating conditions for the A42MX family devices.

The average pulse width of the transient current spike, which can be derived from the measured data, is 350 ns, with its value increasing as the power supply ramp-rate increases. The transient current peak value is also related to the number of logic modules in the device, meaning that larger devices have higher transient current. For instance, A42MX36 has higher transient current than A42MX24, which in turn has higher transient current than A42MX16.

The transient currents were reduced with the slower ramp-rates. Figure 1 on page 3 shows the relation between ramp rates and the transient current peak for the 42MX family devices.

For mixed-voltage systems, the transient current is similar to that of the 5V only operation.

Table 2 • **Transient Current for 42MX Parts at Different Ramp-Rates[1]**

Operating Systems	Products	Transient Current on V_{CCA} (mA) at Different Ramp-Rates (Average Values)						
		0.5 V/µs	0.05 V/µs	10 V/ms	5 V/ms	0.5 V/ms	0.2 V/ms	0.05 V/ms
5 V only systems	A42MX16	600	447	357	231	142	133	129
	A42MX24	686	651	476	350	182	152	154
	A42MX36	755	744	500	485	212	164	157
	Products	**Transient Current on V_{CCA} (mA) at Different Ramp-Rates (Average Values)**						
3.3 V only systems		0.33 V/µs	0.033 V/µs	6.6 V/ms	3.3 V/ms	0.33 V/ms	0.132 V/ms	0.033 V/ms
	A42MX16	275	265	257	208	136	133	126
	A42MX24	394	387	371	303	181	159	150
	A42MX36	454	458	450	398	174	157	154

Note: 1. Use a regulator for the V_{CC} supply that can source a minimum of 100 mA transient current during power-up. Failure to provide enough power can prevent the system from powering up properly and

result in functional failure. However, there are no reliability issues, as transient current is not confined to a localized spot and distributed across the die.

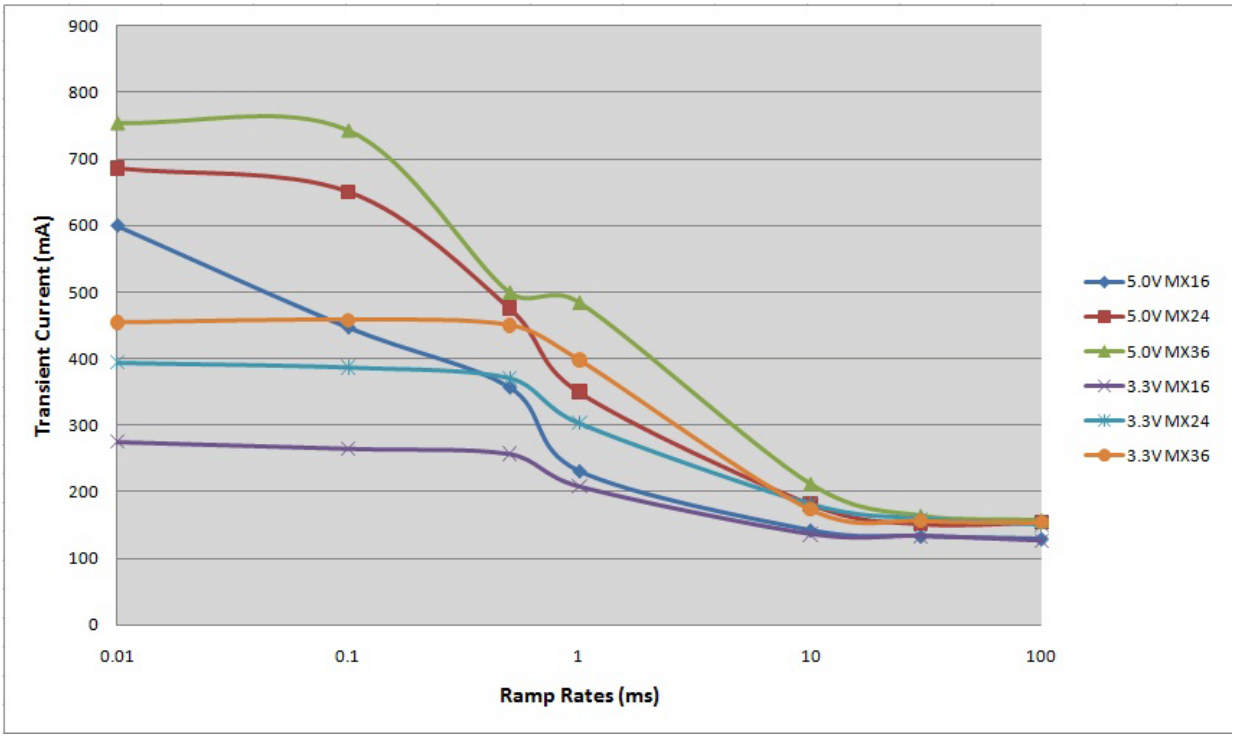

Figure 1• **Transient Current vs. Ramp-Rates for A42MX16, A42MX24, and A42MX36 at 5 V and 3.3 V Operating Conditions**

I/O Behavior During Power-Up

This section describes the behavior of the 42MX device family I/Os during power-up cycles. One of the important parameters during power-up is the voltage level at which the I/Os are functional. As the functionality of I/Os is defined by the time the internal logic is functional, the power-up to functional time depends on the ramp-rates of V_{CCA} and not V_{CCI}. However, the proper data cannot be read from or written into the device unless V_{CCI} reaches the value where I/Os are active. After the I/Os are active, there is some additional delay for the input data to propagate to the output pins. In single voltage operations, there is only one power supply. Therefore, the power-up to functional times and I/O functional times are equal. Table 3 and Table 4 present the power-up to functional voltage levels for the single-voltage operation mode. They indicate the amount that the power-up to functional voltage level increases for faster ramp-rates and larger arrays.

Table 3 • **V_{CCA} Voltage Where I/Os Become Active in 5 V Only Operation**

Ramp-Rate	0.5 V/µs	0.05 V/µs	10 V/ms	5 V/ms	0.5 V/ms	0.2 V/ms	0.05 V/ms
A42MX16	5.00	4.65	3.13	2.81	2.41	2.31	2.25
A42MX24	5.00	4.81	3.63	3.16	2.41	2.40	2.34
A42MX36	5.00	4.91	3.92	3.73	2.54	2.38	2.36

Table 4 • **V_{CCA} Voltage Where I/Os Become Active in 3.3 V Only Operation**

Ramp-Rate	0.33 V/µs	0.033V/µs	6.6 V/ms	3.3 V/ms	0.33 V/ms	0.132 V/ms	0.033 V/ms
A42MX16	3.30	3.30	2.88	2.66	2.33	2.30	2.25
A42MX24	3.30	3.30	3.19	2.93	2.40	2.34	2.28
A42MX36	3.30	3.30	3.30	3.07	2.46	2.41	2.34

In a mixed-voltage operation mode, as the array voltage (V_{CCA}) is 5 V, and power-up to functional time depends on the V_{CCA} ramp-up, Table 3 applies for mixed-voltage mode. However, there are two cases that should be taken into consideration during the power-up in a mixed-voltage mode.

The first case occurs when the power-up delay between V_{CCA} and V_{CCI} is larger than the power-up to functional time. In this case, the internal modules are functional and the I/Os are inactive. Therefore, each I/O's functional time is defined as the time when V_{CCI} is powered up. The second case is more critical and happens if the power-up delay between V_{CCA} and V_{CCI} is less than the power-up to functional time. In other words, it happens when the I/Os are functional but the internal logic modules are not. Therefore, the I/Os are driven to their designated voltage level as soon as the power-up to functional time is reached. In such a condition, there is a short period of time (after I/O activation and before array functionality) that the I/Os might be driven into an unknown state. Therefore, Microsemi recommends to power-up V_{CCI} after V_{CCA} has reached its functional level.

During the characterization procedure, the inputs and outputs of the 42MX family devices are tested to determine their behavior during power-up, specifically before they are functional. The results of different measurements demonstrate that the I/Os are tristated during the power-up. In other words, a voltage can be applied to the 42MX device I/O before and during power-up of the device.

Conclusion

For proper power-up of the 42MX family devices, V_{CCA} must always be greater than V_{CCI} during power-up. This document describes the transient current on V_{CCA} and functional voltage level during power-up. The transient current in the 42MX devices is reduced by increasing the power-up rise time. For faster power-up, the voltage level in which the device becomes functional is high. The 42MX device I/Os are also tristated before reaching the functionality point, which makes it possible to apply voltage on I/Os during power-up.

List of Changes

The following table shows important changes made in this document for each revision.

Revision	Changes	Page
Revision 3 (August 2015)	Removed all instances of and references to x39 device (SAR 49122).	NA
	Added "Purpose" section.	1
	Updated "Introduction" section.	1
	Updated "Transient Current" section.	2
	Updated Table 2, Table 3, and Table 4.	2 and 4
	Added Figure 1• Transient Current vs. Ramp-Rates for A42MX16, A42MX24, and A42MX36 at 5 V and 3.3 V Operating Conditions.	3
Revision 2 (March 2005)	Updated "Introduction" section.	1
Revision 1 (March 2003)	Updated "Transient Current" section.	2

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