

### Overview

This application note provides the information needed for seamless migration of a design from the 1200XL and 3200DX families to the 42MX family.

The Actel 42MX device architecture is based on the Actel 1200XL and 3200DX families; thus, it shares the same library of basic cells and does not require a re-synthesis of the design for migration. The 1200XL family is implemented on a 0.80 µm double-layer metal CMOS process, while the 42MX family uses a 0.45 µm triple-metal CMOS process, enabling significant improvements in performance. Similar to the 1200XL and 3200DX devices, the 42MX FPGAs are Oxide-Nitride-Oxide (ONO) antifuse-based, single-chip solutions. The 42MX devices are 5 V and JTAG compliant.

## Comparison

Table 1 on page 2 shows the recommended migration path for architecturally compatible devices. For a given 1200XL or 3200DX device, the recommended 42MX device is shown in the same colored grouping. In most cases, an equivalent package is available in the 42MX family; however, there are some packages in 1200XL and 3200DX that do not exist for the recommended 42MX device. In such scenarios, you must change to a different package. If the same package is available in 42MX, logic placement and I/O assignments can be preserved by using the TCL script, which is described later in the "Migrating Using TCL Script migrate\_to\_mx.tcl" section on page 5. If the same package is not available in 42MX, logic placement and I/O assignments may need to be altered from the original design.

Table 2 on page 2 shows the recommended migration path for 3200DX devices that do not have an exact architecture match in 42MX devices. If you are using an A3265DX device, you can switch to the A42MX16 device if the design does not use the wide decode modules, or you can switch to the A42MX24 device if the design does use the wide decode modules. If you are using an A32100DX device, you can switch to the A42MX24 device if the design does use the wide decode modules. If you are using an A32100DX device, you can switch to the A42MX24 device if you do not use SRAM or quadrant clocks, but you must use the A42MX36 device if any of these features are utilized in the design. For all of these scenarios, you must migrate to a larger device, and as a result, logic placement cannot be preserved. In some scenarios, such as migration from A3265DX-PQ100 with wide decode to A42MX24, you may need to select a different package in the 42MX family. In such cases, I/O assignments cannot be preserved.

For both tables, the packages highlighted in black have no direct compatible packages in the 42MX family. Refer to the "Appendix" on page 11 for a complete list of suggested migrations.

**Note**: The number of user I/Os for compatible 42MX devices and packages is always greater than or equal to those of 1200XL/3200DX devices. Refer to the 40MX and 42MX Family FPGAs datasheet for the exact number.

Devices	A1225XL	A1240XL	A42MX09	A1280XL	A42MX16	A32140DX	A42MX24	A32200DX	A42MX36
SRAM bits	0	0	0	0	0	0	0	2,560	2,560
Logic Modules									
Seq.	231	348	348	624	624	954	954	1,230	1,230
Comb.	220	336	336	608	608	912	912	1,184	1,184
Decode	0	0	0	0	0	24	24	24	24
SRAM Modules (64×4 or 32×8)	0	0	0	0	0	0	0	10	10
Dedicated Flip-Flops	231	348	348	624	624	954	954	1,230	1,230
Clocks	2	2	2	2	2	2	2	6	6
User I/Os (maximum)	83	104	104	140	140	176	176	202	202
Packages (by pi n counts)									
PLCC	84	84	84	84	84	84	84	-	_
PQFP	100	100, <b>144</b>	100, 160	160, 208	100, 160, 208	160, 208	160, 208	208	208, 240
VQFP	100	_	100	_	100	_	_	-	_
TQFP	-	176	176	176	176	176	176	-	_
CQFP	-	_	-	172	-	256	-	208, 256	208, 256, 272
PBGA	-	-	-	-	-	-	-	-	-
CPGA	100	132	-	176	-	_	-	-	-
RQFP	-	-	-	-	-	-	-	208, 240	-

Table 1	<ul> <li>Device Comparison Between</li> </ul>	n 1200XL, 3200DX, and 42MX (excluding A3265DX and A32100DX	()
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#### Table 2 • Device Comparison for A3265DX and A32100DX

Devices	A3265DX	A42MX16	A42MX24	A32100DX	A42MX24	A42MX36
SRAM bits	0	0	0	2,048	0	2,560
Logic modules						
Seq.	510	624	954	700	954	1,230
Comb.	475	608	912	662	912	1,184
Decode	20	0	24	20	24	24
SRAM Modules (64×4 or 32×8)	0	0	0	8	0	10
Dedicated Flip-Flops	510	624	954	700	954	1,230
Clocks	2	2	2	6	2	6
User I/Os (maximum)	126	140	176	152	176	202
Packages (by pin counts)						
PLCC	84	84	84	84	84	_
PQFP	<b>100</b> , 1 <mark>60</mark>	100, 160, 208	160, 208	<b>160</b> , 208	160, 208	208, 240
VQFP	_	100	_	-	-	_
TQFP	176	176	176	176	176	_
CQFP	_	_	_	84	-	208, 256
PBGA	-	-	-	—	-	272

## **Pin-to-Pin Comparison**

### **Power Supply Pin Comparison**

The supply voltage pins of the 42MX family are fully compatible with 1200XL and 3200DX devices. There are several new pins in the 42MX devices that did not exist in the 1200XL and 3200DX devices:

- $V_{CCA}$  and  $V_{CCI}$ : In the 42MX family, the supply voltage for the array is  $V_{CCA}$ , and the supply voltage ٠ for I/Os is V<sub>CCI</sub>. Both the array and I/Os are supplied by V<sub>CC</sub> in the 1200XL and 3200DX families.
- LP: Low Power Mode pin. In this mode, all I/Os are tristated, all input buffers are turned off, and the core of the device is turned off. This feature is particularly useful for battery-operated systems where battery life is a primary concern.
- NC: No Connection. This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

Table 3 lists power supply recommendations for the new pins in 42MX devices.

3200DX/1200XL Pin	42MX Pin	Recommendation
V <sub>CC</sub>	V <sub>CCA</sub>	Connect to board V <sub>CC</sub> supply
V <sub>CC</sub>	V <sub>CCI</sub>	Connect to board V <sub>CC</sub> supply
V <sub>CC</sub>	NC	Connect to board V <sub>CC</sub> supply
GND	LP/GND	Connect to GND

Table 3 • Power Supply Pin Recommendation

### **I/O Comparison**

All I/Os are at the same location for compatible devices that have the same package.

### **Special Pins Comparison**

MODE, PROBE, SDI, SDO, TDI, TDO, and JTAG pins are fully compatible in terms of location, default configuration, and functionality.

### **Quadrant Clocks**

Quadrant clocks are only available in A42MX36 devices. If you are using 3200DX devices with guadrant clocks, you must migrate to the A42MX36 device. Otherwise, the design must be modified to remove the guadrant clocks.

## **Power Supply Voltages**

Compatible devices run on the same voltage level of 5 V or 3.3 V. 42MX devices can also operate in mixed 5 V / 3.3 V systems (Table 4). For additional information about operating conditions and electrical specifications, refer to the *Integrator Series FPGAS: 1200XL and 3200DX* and *40MX and 42MX FPGA* datasheets.

Device	V <sub>cc</sub>	V <sub>CCA</sub>	V <sub>CCI</sub>	Maximum Input Tolerance	Nominal Output Voltage
1200XL and 3200DX	5.0 V	-	-	5.5 V	5.0 V
	3.3 V	_	_	3.6 V	3.3 V
42MX	-	5.0 V	5.0 V	5.5 V	5.0 V
	_	3.3 V	3.3 V	3.6 V	3.3 V
	_	5.0 V	3.3 V	5.5 V	3.3 V

Table 4 • Power Supply Voltage Comparison

## **Power-Up Recommendation**

When powering up 42MX in mixed-voltage mode, V<sub>CCA</sub> must be greater than or equal to V<sub>CCI</sub> throughout the power-up sequence. If V<sub>CCI</sub> exceeds V<sub>CCA</sub> during power-up, either the I/O input protection junction on the I/Os will be forward-biased or the I/Os will be at logical HIGH, resulting in I<sub>CC</sub> rising to high levels. Actel strongly recommends this power-up sequence to ensure the device's functionality. For the purpose of migrating to 42MX, this will not be an issue, since V<sub>CCA</sub> and V<sub>CCI</sub> will be connected to the same board V<sub>CC</sub> supply.

## **Configuration of Unused I/Os**

The same configuration applies to both families (Table 5).

Legacy Device	Comparable Device	Configuration
1200XL	A42MX09, A42MX16	Pulled LOW
3200DX	A42MX24, A42MX36	Tristated

Table 5 • Unused I/Os for All Families

Unused I/Os are automatically configured by Actel Designer software. In all cases, Actel recommends you tie all unused 42MX I/Os to LOW on the board. For more information, refer to the Knowledge Base document, "Default Settings for Unused I/Os and Clocks".

## **Design Migration Procedure**

The 42MX family is fully supported by Actel Libero<sup>®</sup> Integrated Design Environment (IDE) and Actel Designer FPGA development software. This section provides instructions for using the Actel Libero IDE / Designer tool suite to migrate a 1200XL or 3200DX design to the 42MX family. Design files such as an ADB file or ADL, EDN, and PIN files are required to complete the process. An independent script is provided to help you migrate automatically to a 42MX ADB file without manual intervention. This script resolves several issues that need to be carefully handled in the manual procedure, such as timing constraints, compatible packages, operating conditions, etc. Actel strongly recommends using the script flow as the primary method of design migration to the 42MX family.

If the original design was created with Designer v3.1 or older, it requires the Object Store server to be running in order to convert the design to a newer version of Designer. This can be done if Designer v3.x is available by following the installation and setup instruction manual for that release of Designer. If the Object Store server is not available, Actel Technical Support can perform the conversion for you. Contact Technical Support by email at tech@actel.com or call 1-800-262-1060 for assistance.

### Migrating Using TCL Script migrate\_to\_mx.tcl

Download the *migrate\_to\_mx.tcl* script file from http://www.actel.com/documents/migrate\_to\_mx\_DF.zip. This script will automatically find the compatible die and package in the 42MX family. If your 3200DX/1200XL package does not have a compatible 42MX pin-to-pin package, the script will try to migrate your 3200DX/1200XL package to the largest 42MX package of the same type.

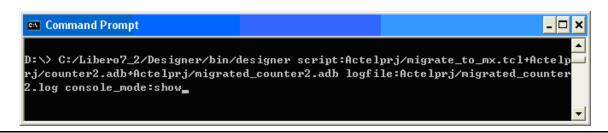
This TCL script can be run in batch mode or the Designer GUI.

#### 1. Running TCL in Batch Mode

#### Usage:

<pl/>designer script:<p2/>migrate\_to\_mx.tcl+<p3/original.adb>+<p4/newname.adb> logfile:<p4/newname.log> console\_mode:show

In order to specify the path to your files, use a forward slash (/), as shown in Figure 1.



#### Figure 1 • Example TCL Script

The console\_mode argument is optional and can only be used in Windows. When console\_mode is used, a transcript window is invoked, as shown in Figure 2.

```
🏶 C:/Libero7_2/Designer/bin/designer script:Actelprj/migrate_to_mx.tcl+Actelprj/counter2....
                                                                               - 🗆 🗙
Variable SPEED = -2
Post-Combiner device utilization:
                                 Total: 624
    SEQUENTIAL
                    Used:
                                                (0.32%)
                              2
    LOGIC
                                 Total: 1232
                    Used:
                              5
                                                (0.41%) (sea+comb)
    10
                    Used:
                              8
                                 Total:
                                        125
    CLOCK
                    Used:
                                 Total:
                              1
                                           2
          Previous family '3200DX' package data is not compatible with current
Warning:
          family '42MX'.
There were 0 error(s) and 1 warning(s) in this design.
The Compile command succeeded ( 00:00:01 )
Design saved to file D:\Actelprj\migrated_counter2.adb.
1igrated design from 3265-2_qfp160 to 42mx16-2_qfp160
Pin assignments transferred from the original design.
Please run Layout and verify timing.
The Execute Script command succeeded ( 00:00:18 )
Design closed.
> Designer execution ended.
  It is now okay to close this window.
```

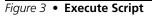
#### Figure 2 • Transcript Window

After running this command, an ADB, ADL, PIN, and LOG file will be generated in the specified directory.

#### 2. Running TCL Script in Designer GUI

Open the 3200DX/1200XL ADB file in Designer and select **File** > **Execute Script**. Enter the destination where you want to save the new 42MX ADB file into **Arguments**. Make sure you have a forward slash (/) in the path. Click **Run** (Figure 3).

Execute Script	X
Script <u>f</u> ile:	D:/Actelprj/migrate_to_mx.tcl
	Browse
<u>A</u> rguments:	D:/Actelprj/migrated.adb
Help	<u>R</u> un Cancel



Click **Save**, if the script succeeds with the migration procedure. Otherwise, the new ADB file will be at the original state of the design before the execution of the script.

### **Manual Migration Procedure**

#### Step 1: Opening an Existing 1200XL/3200DX Project in Designer

This step assumes that the 1200XL/3200DX ADB file has complete information up to Layout. If you only have the netlist ADL/EDN and other constraint source files, skip to "Step 3: Creating a New 42MX Project in Designer" on page 7.

Open the Designer software and select **Open Existing Design** to open the project ADB file. When the project is opened, the Compile and Layout icons should be green (Figure 4). If you experience any difficulty opening an old 1200XL or 3200DX ADB file, contact Actel Technical Support by email at tech@actel.com or call 1-800-262-1060 for assistance.

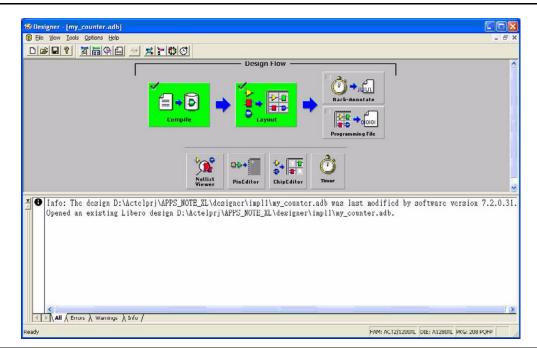


Figure 4 • Compile and Layout Icons in Designer



#### Step 2: Exporting Netlist and Pinout List from Designer

Select **File > Export > Netlist Files** to export the ADL netlist (Figure 5). Choose **File > Export > Constraint files** to export the pinout list, \*.PIN, from Designer. Accept the defaults to export the ADL and PIN files.

Export Netlist F	iles	? 🛛
Save jn:	🗁 synthesis 💌 🔶	🗈 🕂 🎟 -
My Recent Documents Desktop	📄 syntmp 📾 newCore.adl	
My Documents		
My Network Places	File newCore.adl Save as type: Actel ADL Netlist Files (".adl)	▼ <u>S</u> ave ▼ Cancel

Figure 5 • Export Netlist Files

If you want to preserve the timing constraints, you can export a DCF file from the 3200DX/1200XL design.

#### Step 3: Creating a New 42MX Project in Designer

In Designer, choose **File > New**. Enter the design name and select the family **42MX**, as shown in Figure 6.

Setup Design		
Design <u>n</u> ame:	new	
Select family:	42MX 💌	
Working <u>directory</u> :	C:\Actelprj\	Browse
Help	ОК	Cancel

Figure 6 • Setup Design

### Step 4: Importing Netlist and Pinout List Back into the New 42MX Project

Choose **File > Import Source Files**. Add the ADL or EDN netlist and PIN files of the 1200XL/3200DX project into this new 42MX project, as shown in Figure 7.

Import	Import Source Files						
When in	e relative order of the same type of files is important. porting multiple EDIF or VHDL files, the top-level file must be last (at Up and Down buttons to specify the relative order of the files.	the bottom).					
	Source Files	Туре		Add			
1	D:\Actelprj\APPS_NOTE_XL\synthesis\my_counter.adl	adl					
2	D: \Actelprj\APPS_NOTE_XL\designer\impl1 \APPS_NOTE_42MX.pir	pin		Modify			
3							
4				Delete			
5							
6							
7 8							
9				<u>+</u>			
10	4			4			
10	4		~	<b>–</b>			
Audit tim	estamp:	Audit options.					
He	lp	OK		Cancel			

Figure 7 • Importing Source Files

#### Step 5: Follow the Design Flow

Click the **Compile** button and the Device Selection Wizard will open. Choose the compatible 42MX die/package, as shown in Figure 8.

A42MX16 A42MX24 A42MX36	84 PLCC 100 PQFP 100 VQFP 160 PQFP 176 TQFP
Speed: -3	Die <u>v</u> oltage (VCCi/VCCa):

Figure 8 • Device Selection Wizard

You also need to set identical operating conditions and carefully choose the device speed grade for the new 42MX design. Examples of operating conditions are  $V_{CCI}/V_{CCA}$ , Restrict-Probe-pins, TEMP range, and VOLT range. If you export the DCF file from your 1200XL/3200DX design, you need to import this DCF file into the 42MX design after the Compile step. From here, follow the Designer flow to complete migrating the 1200XL/3200DX design.

## **Timing Concerns**

The 42MX family is faster than the 3200DX/1200XL families. Therefore, Actel recommends that you perform a new timing analysis and pay attention to the hold time, cross clock domain paths, clock-to-out and multi-cycle paths. Refer to the *Static Timing Analysis Using Designer's Timer* application note for more information on performing timing analysis using the Actel SmartTime tool. You should also verify the potential simultaneously switching outputs by checking whether various adjacent outputs have enough timing differences (staggered timing) to avoid negative effects. The manual migration procedure does not preserve all placements, even for compatible packages. If you want to preserve the timing constraints, you can export the DCF file from the 3200DX/1200XL design, which is described in the "Manual Migration Procedure" section on page 6. You need to import this DCF file into the 42MX design after the Compile step. The *migrate\_to\_mx.tcl* script automatically preserves timing constraints as well as all placements if possible.

## Programming

#### **Programming Software**

Programming files are not compatible between the two families. You need to generate a new programming file (AFM) from the migrated design.

#### **Programming Hardware**

Silicon Sculptor: Uses the same module for both families.

Activator: Actel no longer supports this programmer. Refer to the Actel website for a list of Silicon Sculptor modules.

### **Summary**

The minimum steps to migrate from the 1200XL and 3200DX to 42MX are as follows:

- 1. Find the compatible 42MX device and package from Table 1 on page 2 and Table 2 on page 2.
- 2. Connect the  $V_{CCA}$ ,  $V_{CCI}$ , and NC pins to the board power supply  $V_{CC}$ .
- 3. Migrate to A42MX36 if you have a 3200DX design that uses quadrant clocks, or modify the design to remove the quadrant clocks.
- 4. Update to the latest version of software and follow the "Design Migration Procedure" section on page 4.
- 5. Redo timing analysis.
- 6. Generate a new 42MX programming file.

### Conclusion

The 42MX family shares numerous architectural features and the library of basic elements with the 1200XL and 3200DX families, and offers higher speed and special functionalities. Understanding the differences between the two families makes a seamless migration from the 1200XL and 3200DX families to the 42MX family possible.

## **Related Documents**

#### **Datasheets**

Integrator Series FPGAs: 1200XL and 3200DX Families http://www.actel.com/documents/IntegratorSeries\_DS.pdf 40MX and 42MX FPGA Families http://www.actel.com/documents/MX\_DS.pdf

### **Application Notes**

42MX Family Devices Power-Up Behavior http://www.actel.com/documents/MX\_PowerUp\_AN.pdf Static Timing Analysis Using Designer's Timer http://www.actel.com/documents/Static\_Timing\_Analysis\_AN.pdf

### **Other Documents**

Default Settings for Unused I/O and Clocks http://www.actel.com/kb/article.aspx?id=SL1058 Libero IDE Design Flow http://www.actel.com/products/tools/libero/flow.html

# Appendix

 Table 6
 Migration Packages

Legacy Die	Suggested Migration	Legacy Package	Migration Package	Notes
A1225XL	A42MX09	PG100	N/A	
		PL84	PL84	
		PQ100	PQ100	
		VQ100	VQ100	
A1240XL	A42MX09	PG132	N/A	
		PL84	PL84	
		PQ100	PQ100	
		PQ144	TQ176	
		TQ176	TQ176	
A1280XL	A42MX16	CQ172	PQ208	
		PG176	N/A	
		PL84	PL84	
		PQ160	PQ160	
		PQ208	PQ208	
		TQ176	TQ176	
A3265DX	A42MX16	PL84	PL84	No fast and wide decodes
		PQ100	PQ100	No fast and wide decodes
		PQ160	PQ160	No fast and wide decodes
		TQ176	TQ176	No fast and wide decodes
	A42MX24	PL84	PL84	Fast and wide decodes
		PQ100	PQ160	Fast and wide decodes
		PQ160	PQ160	Fast and wide decodes
		TQ176	TQ176	Fast and wide decodes
A32100DX	A42MX24	PL84	PL84	No RAM or QCLK
		PQ160	PQ160	No RAM or QCLK
		PQ208	PQ208	No RAM or QCLK
		TQ176	TQ176	No RAM or QCLK
		CQ84	PQ208	No RAM or QCLK
	A42MX36	PL84	N/A	If RAM and/or QCLK are used
		PQ160	CQ256	If RAM and/or QCLK are used
		PQ208	PQ208	If RAM and/or QCLK are used
		CQ84	CQ256	If RAM and/or QCLK are used
A32140DX	A42MX24	CQ256	N/A	
		PL84	PL84	
		PQ160	PQ160	
		PQ208	PQ208	
		TQ176	TQ176	

Legacy Die	Suggested Migration	Legacy Package	Migration Package	Notes
A32200DX	A42MX36	CQ208	CQ208	
		CQ256	CQ256	
		PQ208	PQ208	
		RQ208	PQ240	PQ240 does not have a heatsink.
		RQ240	PQ240	PQ240 does not have a heatsink.
A32300DX	N/A	CQ256	N/A	
		RQ208	N/A	
		RQ240	N/A	

#### Table 6 • Migration Packages (Continued)

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