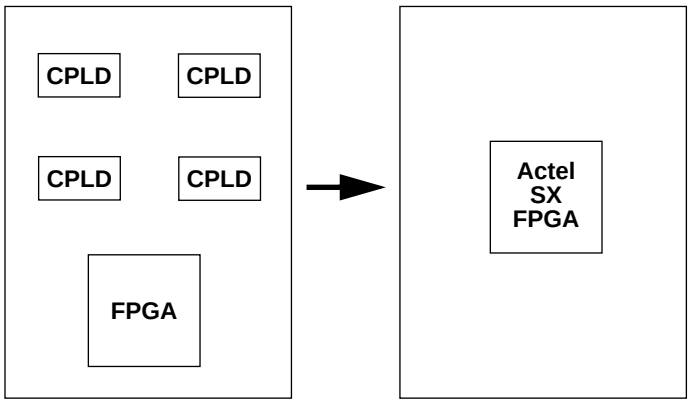
Integrating Multiple CPLD Functions in an Actel SX Device



Introduction

This application brief describes a configurable DMA Controller design for a Motorola 68060 and compares the implementation of the design in an Actel SX FPGA with implementations of the same design in multiple CPLDs. This application brief demonstrates that Actel SX FPGAs offer improvements in integration and performance over CPLDs, and allow logic designers to avoid the high cost, high power consumption, and excessive board space associated with designs implemented in CPLDs.

Limitations of Multiple CPLD Designs

Designers have traditionally used multiple high-speed CPLDs to integrate functions such as DMA controllers in embedded systems to avoid using a masked ASIC. This method of logic integration for these applications in the past has been restricted to CPLDs because they were the only devices that offered the necessary high performance combined with user programmability.

However, there are many limitations associated with a high-speed logic solution using multiple CPLDs. The CPLDs needed for high performance systems are expensive. The CPLDs also occupy a large amount of board space because the design is partitioned into multiple devices. The partitioning itself can cause design and verification complications, as well as impact the reliability of the system because of the large number of soldered connections. Finally, there is the risk of exceeding the system power budget or of creating thermal problems in the system enclosure because of the relatively high power consumption of CPLDs.

Configurable DMA Controller

Figure 1 shows a system block diagram of a configurable dual-channel synchronous DMA controller consisting of a microprocessor interface, register bank, internal FIFO and overall controller state machine. The microprocessor interface is designed to work with the full 33MHz bus bandwidth of the 68060 and uses a processor clock of 66MHz for all internal state machines. It has bus mastering capability and can burst four 32-bit data words in succession (although this feature is not used due to the limited FIFO size). The microprocessor also has read-through capability on the DMA side of the device. This allows the microprocessor access to any configuration registers in the device utilizing the DMA channel. The register bank consists of eight 32-bit registers that perform receive pointers, transmit pointers, control, status, interrupt vectors, and receive and transmit counters. The FIFO consists of two sets of long word buffers. These buffers can then be sent or received on the DMA bus in 8-bit wide format. The controller state machine controls the various blocks within the design, ensuring that data is transferred among all the blocks successfully.

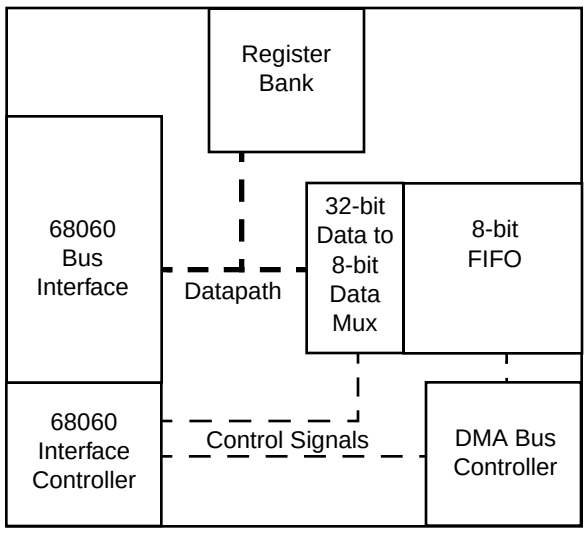


Figure 1 • *DMA Controller Block Diagram*

The CPLD Solution

CPLDs from Xilinx and Altera were considered as alternative solutions for this application. In both cases, more than one CPLD had to be used to implement the design. The Xilinx solution required 5 devices and the Altera solution required 10. Because the register bank in the design is substantial and the register count on the biggest device in both CPLD families was insufficient, the CPLD solutions explored had problems accommodating the design. In fact, these registers were generally reduced in size so that the design could be fitted to allow a speed comparison to be made.

As the number of devices increases, the number of I/Os used to interconnect the multiple devices also increases, leading to inefficient use of I/O pins. Also, when a design has been partitioned across multiple devices, the limiting performance factor is often the speed of the interconnecting I/Os rather than the speed of the I/Os interfacing to the outside world. The CPLDs were short on I/O pins and didn't have the registers available to implement the additional FIFO size necessary for a wider data bus.

The speed of the multiple CPLD solutions ranged from a worst case of 26MHz, well short of that required for this system, to a best case of 45MHz. However, even this best case speed only represents the internal speed of a device, and must be reduced to take into account the delays of the inter-device connections of the complete system.

The Actel SX Solution

The full function design was placed and routed in a single Actel A54SX16-PQ208 device, using only 72% of the device logic resources. The remaining 28% of the device could be used to implement additional functionality in the Actel part, further improving the level of logic integration in the target system. Unlike CPLDs, 100% of the logic of SX devices can be utilized and the design will still route with good performance.

The worst case performance of the Actel part in this application was found to be 79MHz, which was comfortably above the 66 MHz specification needed for operation in the target system. Neither optimization of the design code nor manual intervention at the physical layout stage was necessary to achieve the performance goal. In addition, the Actel SX part could have implemented a 16-bit DMA data bus width, but an 8-bit DMA data bus width was used so that the SX design would be equivalent to the multiple CPLD designs.

Power Consumption

Power consumption is a critical factor for the DMA Controller design, so the power consumption of each solution was compared. The Actel SX solution consumed 3.5X less power than the Altera solution and 5X less power than the Xilinx solution. An added benefit is that the SX solution provides higher system reliability than the CPLD solutions.

Conclusion

Here is how the CPLD solutions matched up against the SX solution:

Altera MAX 7000 Family:

FIFO and Registers:	Four EPM7096QC100-7
Controller and uP interface:	Four EPM7096QC100-7
DMA Bus interface and control:	Two EPM7096QC100-7
Internal Performance:	45MHz
System Performance:	33.2MHz
Power Consumption:	1.98W
Synthesis, Place and Route:	MaxPlusII

Xilinx XC9500 Family:

FIFO and Registers:	Two XC95216-10-HQ208
Controller and uP interface:	Two XC95216-10-HQ208
DMA Bus interface and control:	One XC95216-10-HQ208
Internal Performance:	35MHz
System Performance:	26MHz
Power Consumption:	2.75W
Synthesis:	FPGA Express
Place and Route:	Xilinx Foundation Series

Actel SX Family:

(FIFO and Registers, Controller and uP interface, DMA Bus interface and control)

DMA Controller Design:	One A54SX16-PQ208
Utilization:	72%
System Performance:	79MHz
Power Consumption:	537.9mW
Synthesis:	Synplicity Synplify
Place and Route:	Actel Designer Series

Now there is an alternative to using multiple CPLDs to integrate microprocessor system logic that provides dramatic cost and space savings. The Actel SX family of FPGAs can be used to implement the high-speed logic blocks typical of microprocessor embedded systems. SX devices have the density and performance to integrate high performance designs into a single device, saving component cost, board space, and power consumption, as well as increasing system reliability.

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