Improving Fusion ADC Throughput

Table of Contents

Introduction

Microsemi Fusion® is the world's first mixed-signal FPGA family. Among many built-in analog peripherals, Fusion includes an analog to digital converter (ADC) with a configurable 32:1 input analog MUX. The ADC supports 8-, 10-, and 12-bit modes of operation with a cumulative sample rate up to 600 ksps in 8-bit mode. By default, when users setup the sample sequence using the Libero® Integrated Design Environment (IDE) analog system builder (ASB), all active analog input channels share the full ADC bandwidth (throughput) evenly. If the application requires more throughput for some channels than others, users can enter the specific throughput requirements in the ASB, and the tool will automatically adjust. However, when some channels require much more throughput than others and, especially when there are many active channels, users can apply additional techniques to achieve the goal.

This application note describes a methodology that users can implement for improving the throughput of individual analog input channels.

The sample Libero IDE project that was used to develop this application note can be downloaded from the Microsemi web site:*http://soc.microsemi.com/download/rsc/?f=Improving_Fusion_ADC_AN_DF*. Users may consider this sample project as an example of how to configure the sample sequence controller in Libero's IDE Analog System Builder.

Background Information

ADC Throughput Calculation

Fusion ADC throughput is determined by two elements: conversion time (t_conv – the time needed by associated acquisition or sample and hold circuitry, and the time needed to do actual conversion), and turnaround time (t_turnaround –the time needed to process data and give a start signal for another conversion). Figure 1 illustrates the concept of conversion time and turn around time. EQ 1 on page 2 summarizes the sample rate calculation.

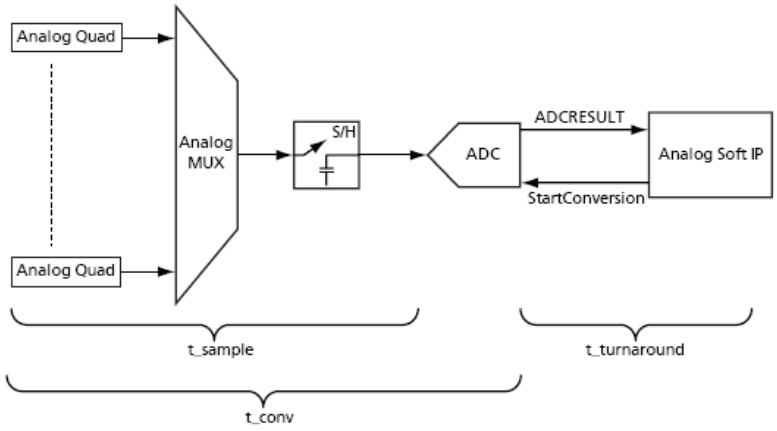

***Figure 1* • Simplified ADC Diagram**

$$SampleRate = \frac{1}{ConversionTime + TurnaroundTime}(S/s)$$

EQ 1

where

S = samples

s = second

The conversion time can vary greatly, depending on the SYSCLK frequency (100 MHz maximum), the ADCCLK frequency (10 MHz maximum, determined by the clock divider, or TVC), the sample time control (STC) settings, and the conversion bit resolution (see equation EQ 2, EQ 3, and EQ 4.)

$$t\_conv = t\_sync\_read + t\_sample + t\_distrib + t\_post\_cal + t\_sync\_write$$

EQ 2

$$T\_conv = SYSCLCK\ period + ((2 + stc) * ADCCLK\ period) + (8, 10, or\ 12 * ADCCLK\ period) + (2\ 8\ ADCCLK\ period) + SYSCLK\ period$$

EQ 3

$$ADCCLK = SYSCLL / (4 * (1 + TVC))$$

EQ 4

where

TVC = 0 ~255

For more information on the sample rate (ADC throughput) calculation, refer to the "Designing the Analog System" chapter of the *Fusion FPGA Fabric User's Guide*.

Sample Rate Calculator

The *sample_rate_calculator.xls* spreadsheet simplifies the sample rate calculation and all necessary components have been pre-compiled in it.

The *Max Signal Frequency Calculator* worksheet (Figure 2 on page 3) calculates the channel throughput based on the input parameters (system clock rate, ADC resolution, acquisition time, and monitor type). When the users enter the input parameters, the calculator reports the total time to process the sample and the allowed maximum input analog signal frequency.

The *Acquisition Time Calculator* worksheet (Figure 3 on page 3) calculates the maximum acquisition (sample) time given the frequency, resolution, and type of monitor. The maximum acquisition time calculated can be entered in the maximum signal frequency calculator to determine the total conversion time for the channel (Figure 2 and Figure 3.)

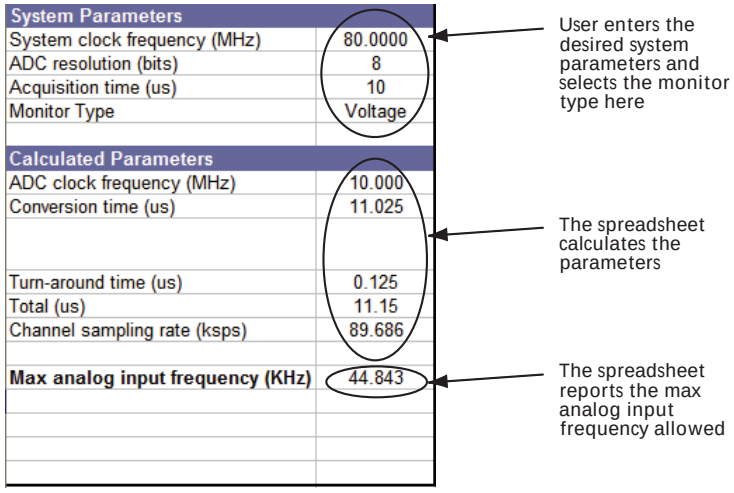

***Figure 2* • Max Signal Frequency Calculator**

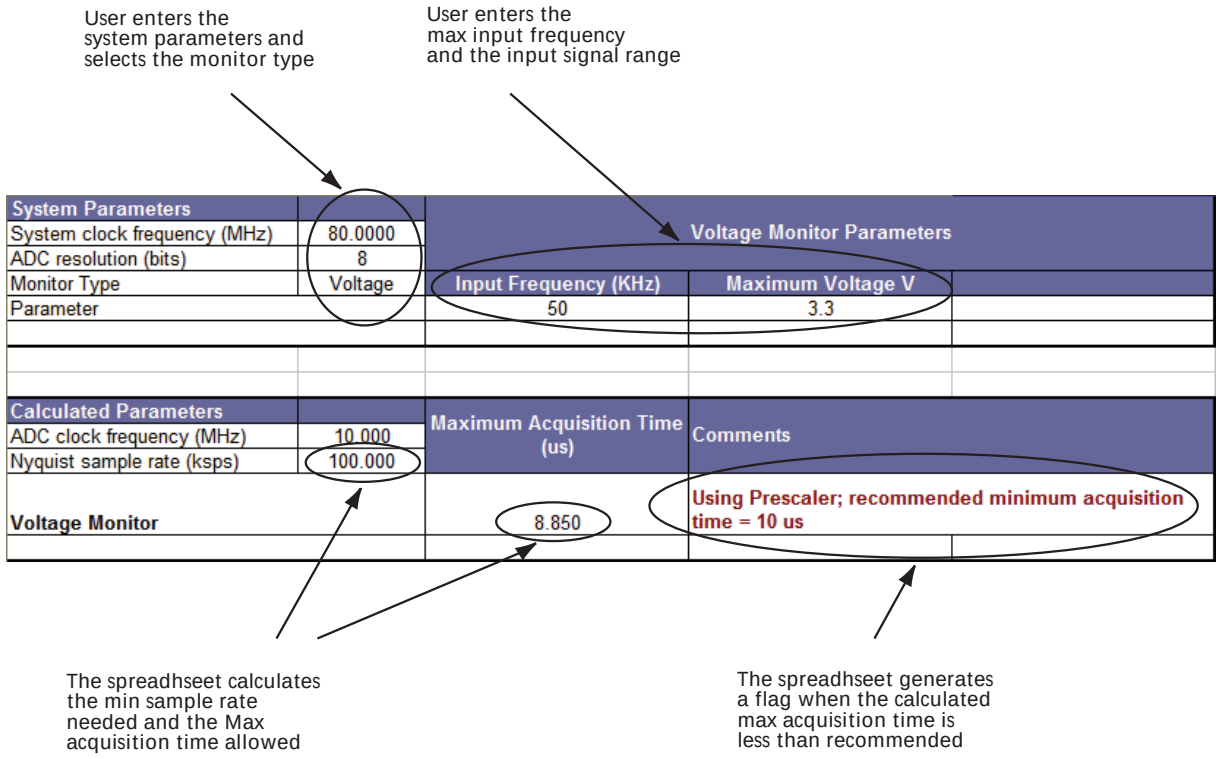

***Figure 3* • Acquisition Time Calculator**

ADC Throughput Allocation

When the application utilizes more than one analog input channel, the total throughput is shared by all active channels. Users can enter the system clock frequency, ADC resolution, and pre-calculated acquisition time into the ASB for each active channel, the sample sequencer will calculate the throughput for each channel automatically. By default, the throughput for each channel is equal to its weight sampling. Figure 4 gives a throughput calculation example of equal weight sampling for 20 active channels.

```
********************************************************************************
                        Throughput Report
********************************************************************************

Procedure:   Main
                      Sampling     Conversion                                  Throughput     Throughput
         Channel      Time(us)       Time(us)  ASSC(us)  SMEV(us)  SMTR(us) Required(Ksps)   Actual(Ksps)
--------------------------------------------------------------------------------------------------------
           Volt1|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt2|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt3|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt4|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt5|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt6|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt7|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt8|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596
           Volt9|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt10|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt11|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt12|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt13|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt14|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt15|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt16|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt17|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
          Volt18|        10.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
INTERNAL_TEMPERATURE|     5.000|        11.250|    0.250|    0.000|    0.000|         0.000|         6.596
INTERNAL_VOLTAGE|         0.200|         1.450|    0.250|    0.000|    0.000|         0.000|         6.596

--------------------------------------------------------------------------------------------------------
Procedure Total Throughput (Ksps) :  131.926
```

***Figure 4* • Equal Weight Sampling Throughput Report**

If some channels have higher throughput requirement than others, or unequal weight sampling, users should enter the required throughput value into the sample sequencer, and then the ASB will recalculate to try to meet the requirements.

To achieve the unequal weight sampling throughput requirements, the analog system builder sample sequencer allocates – within the total 64 time slots for a given procedure –more time slots for channels that require higher throughput, and less time slots for channels that require lower throughput. The example in Figure 5 on page 5 shows that more time slots are assigned to some sample channels than others; as a consequence Volt1 and Volt2 get higher throughput than others, for example Volt5.

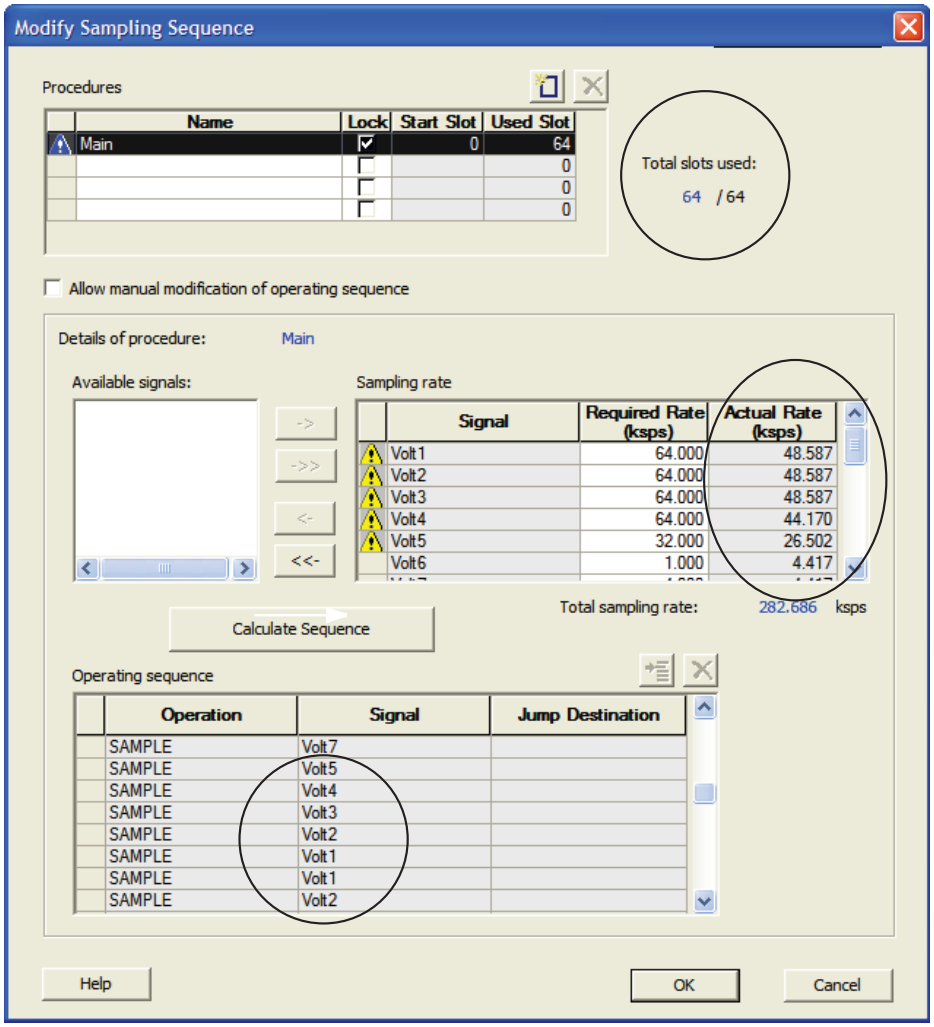

***Figure 5* • Default Unequal Weight Sampling Procedure**

When there are many active channels and some of them have much higher throughput requirements than others, the ASB may not be able to meet all the requirements. Figure 6 on page 6 gives a throughput calculation example of unequal weight sampling for 20 active channels. Channel Volt1, Volt2, Volt3, and Volt4 throughput requirements are not satisfied.

```
*******************************************************************************
                        Throughput Report
*******************************************************************************

Procedure:   Main
                 Sampling     Conversion                                Throughput     Throughput
         Channel Time(us)      Time(us)  ASSC(us)  SMEV(us)  SMTR(us) Required(Ksps)  Actual(Ksps)
-------------------------------------------------------------------------------------------------
           Volt1|     0.200|      1.450|    0.250|    0.000|    0.000|       64.000|       48.587
           Volt2|     0.200|      1.450|    0.250|    0.000|    0.000|       64.000|       48.587
           Volt3|     0.200|      1.450|    0.250|    0.000|    0.000|       64.000|       48.587
           Volt4|     0.200|      1.450|    0.250|    0.000|    0.000|       64.000|       44.170
           Volt5|     0.200|      1.450|    0.250|    0.000|    0.000|       32.000|       26.502
           Volt6|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
           Volt7|     0.200|      1.450|    0.250|    0.000|    0.000|        4.000|        4.417
           Volt8|     0.200|      1.450|    0.250|    0.000|    0.000|        4.000|        4.417
           Volt9|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt10|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt11|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt12|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt13|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt14|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt15|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt16|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt17|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
          Volt18|    10.000|     11.250|    0.250|    0.000|    0.000|        1.000|        4.417
INTERNAL_TEMPERATURE|     5.000|     11.250|    0.250|    0.000|    0.000|        0.000|        4.417
INTERNAL_VOLTAGE|     | 0.200|      1.450|    0.250|    0.000|    0.000|        0.000|        4.417

-------------------------------------------------------------------------------------------------
Procedure Total Throughput (Ksps) :  282.686
```

Figure 6 • **Unequal Weight Sampling Throughput Report**

Design Example

In this design example, there are 20 active analog input channels, Volt [18:1], internal temperature, and internal voltage. The parameters of the design are listed in Table 1. The goal is to achieve the desired throughput for each channel.

Table 1 • **Sample Design Parameters**

Channel Name	Voltage Range (V)	Prescaler	Sampling Time (µS)	Conversion Time (µS)	Turnaround Time (µS)	Time Budget per Sample (µS)	Desired Channel Throughput (ksps)
Volt1	0-2.5	N	0.2	1.45	0.25	1.7	64
Volt2	0-2.5	N	0.2	1.45	0.25	1.7	64
Volt3	0-2.5	N	0.2	1.45	0.25	1.7	64
Volt4	0-2.5	N	0.2	1.45	0.25	1.7	64
Volt5	0-2.5	N	0.2	1.45	0.25	1.7	32
Volt6	0-4	Y	10	11.25	0.25	11.5	1
Volt7	0-2.5	N	0.2	1.45	0.25	1.7	4
Volt8	0-2.5	N	0.2	1.45	0.25	1.7	4
Volt9	0-10	Y	10	11.25	0.25	11.5	1
Volt10	0-10	Y	10	11.25	0.25	11.5	1
Volt11	0-5	Y	10	11.25	0.25	11.5	1
Volt12	0-4	Y	10	11.25	0.25	11.5	1
Volt13	0-4	Y	10	11.25	0.25	11.5	1
Volt14	0-4	Y	10	11.25	0.25	11.5	1

Table 1 • **Sample Design Parameters (continued)**

Channel Name	Voltage Range (V)	Prescaler	Sampling Time (µS)	Conversion Time (µS)	Turnaround Time (µS)	Time Budget per Sample (µS)	Desired Channel Throughput (ksps)
Volt15	0-4	Y	10	11.25	0.25	11.5	1
Volt16	0-4	Y	10	11.25	0.25	11.5	1
Volt17	0-4	Y	10	11.25	0.25	11.5	1
Volt18	0-4	Y	10	11.25	0.25	11.5	1
Internal temperature	N/A	N/A	5	11.25	0.25	11.5	1
Internal voltage	0-2.5	N	0.2	1.45	0.25	1.7	1

Notes:

1. *System Clock = 40 MHz*
2. *ADC Resolution = 10 bit*
3. *Conversion time, turnaround time, and time budget per sample can be calculated by the sample_rate_calculator.xls spreadsheet with system clock frequency, ADC resolution, and required acquisition time.*

The default unequal weight sampling cannot meet the throughput requirement for Volt[5:1] (Figure 5 on page 5).

Throughput Improvement

To improve the throughput of Volt[5:1], more time slots need to be assigned to these channels in the unequal weight sampling procedure (Figure 5 on page 5). But a given procedure created in the ADC sample sequencer of the ASB has a maximum of 64 time slots. To overcome this, users can create multiple procedures and jump sequences.

Since Volt[4:1] require the same high throughput (64 ksps), they are grouped together as the *main* procedure. Volt5 requires the second highest throughput (32 ksps), so it is standalone in the *jump1* procedure. Volt[4:1] and Volt5 have same conversion time, but Volt[4:1] requires twice the throughput of Volt5, so the *main* procedure should also execute twice as often as the *jump1* procedure. Volt[8:7] are grouped in the *jump2* procedure for the next level of throughput requirement (4 ksps). The remaining channels (Volt6, Volt9, Volt[108:10], internal temperature, internal voltage) form their individual *jump* procedures (*jump3*, *jump4*, …). Figure 7, Figure 8, Figure 9, Figure 10, and Figure 11 on page 8 show how to create these procedures in the ASB sample sequencer.

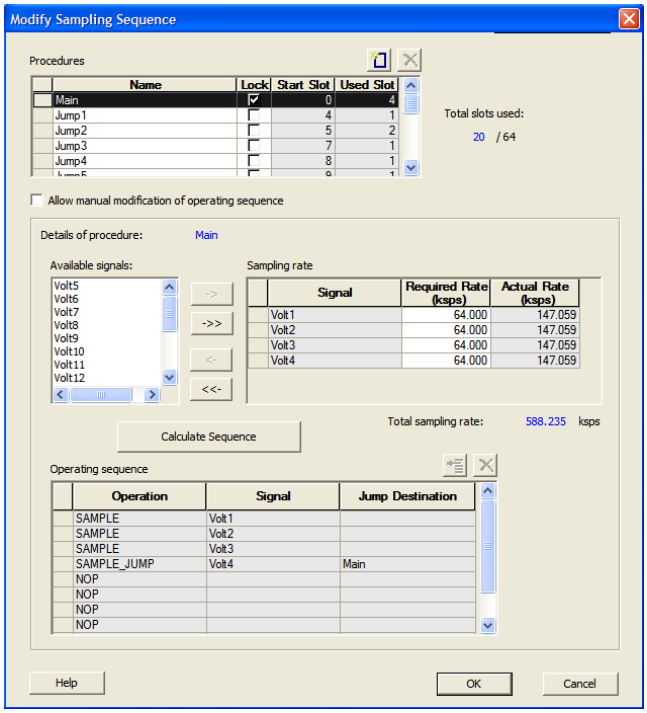

***Figure 7 • Main* Procedure**

Operation	Signal	Jump Destination
SAMPLE_JUMP	Volt5	Main

***Figure 8 • Jump1* Procedure**

Operation	Signal	Jump Destination
SAMPLE	Volt7	
SAMPLE_JUMP	Volt8	Main

***Figure 9 • Jump2* Procedure**

Operation	Signal	Jump Destination
SAMPLE_JUMP	Volt6	Main

***Figure 10 •* Jump3 Procedure**

After creating all these procedures, each channel is assigned to a given time slot. 20 time slots are used throughout the procedures (Figure 11), that solves the time slot overflow issue.

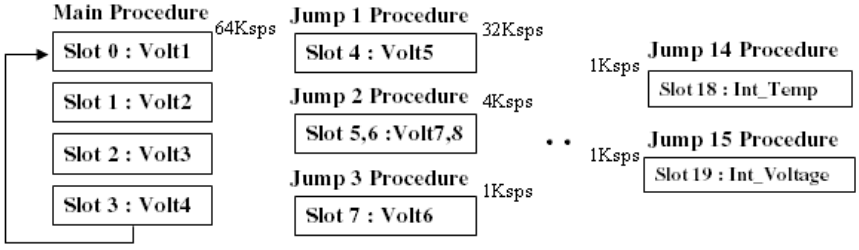

***Figure 11 •* Time Slot Allocation**

In order to meet the throughput requirements, the *main* procedure (M) is executed every other sample time, *jump 1* (J1) is executed every 4 sample times, *jump 2* (J2) is executed every 32 sample times, and other jump sequences are executed one time each in the whole sample loop, interspersed in the sequence. The outlook of the sample loop is shown in Figure 12.

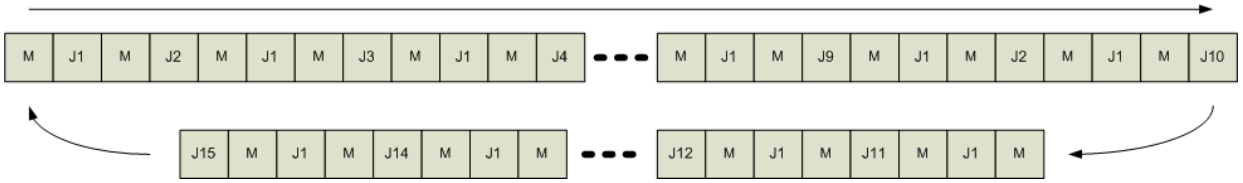

***Figure 12* • Procedure Sequence**

According to this procedure sequence, 152 samples are taken in a loop within 376 µs. The total system sampling rate is 404.255 ksps. Each channel sample rate is:

Volt[4:1] (M)	(30/152) * 404.255 ksps = 79.78 ksps
Volt[5] (J1)	(15/152) * 404.255 ksps = 39.89 ksps
Volt[8:7] (J2)	(2/152) * 404.255 ksps = 5.32 ksps
All others	(1/152) * 404.255 ksps = 2.66 ksps

All channels meet throughput requirements.

The sample sequence is executed by ADC sample sequence controller (ASSC), part of the ASB block IP. In this design example, the procedure sequence is controlled by a state machine through ASSC (Figure 13). The state machine is implemented in the Fusion FPGA core logic.

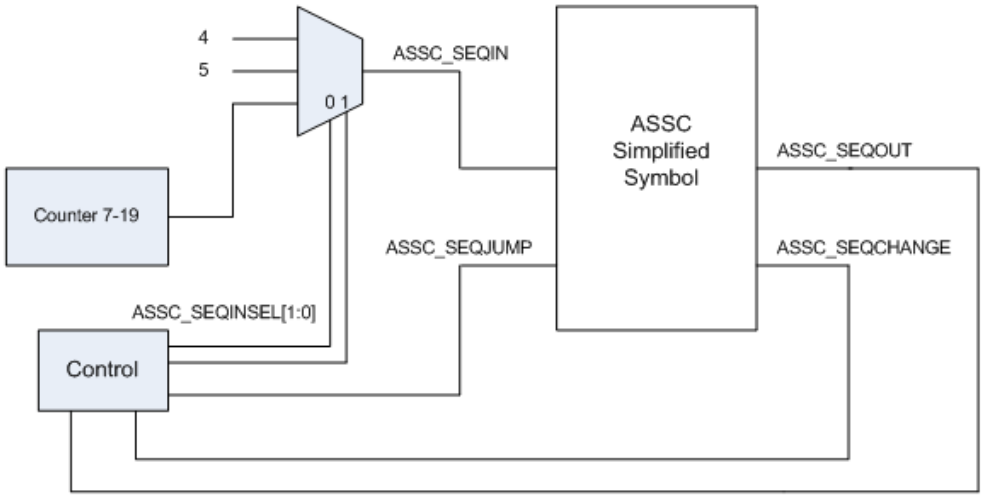

***Figure 13* • Procedure Sequence Control State Machine and ASSC Interface**

Table 2 on page 10 describes the ASSC interface for jump sequence control.

Table 2 • **ASSC Jump Sequence Control Interface Signals**

ASSC Jump Sequence	Signal	Description
ASSC_SEQJUMP	Input	Sequence Jump Enable: Setting this signal to logic 1 will jump to the sequence number indicated in the ASSC_SEQIN input pins after the current sequence timeslot has completed. This signal must be high for one system clock cycle, and it is controlled by the state machine in this design example.
ASSC_SEQIN	Input	Sequence Number In: These inputs are used in conjunction with the ASSC_SEQJUMP signal to jump from the current sequence to a particular sequence number after the current sequence timeslot has completed. This signal is controlled by the state machine in this design example.
ASSC_SEQOUT	Output	Sequence Number Out: These outputs denote the current sequence timeslot.
ASSC_SEQCHANGE	Output	Sequence Change: This output indicates that the ASSC_SEQOUT outputs are about to change after the very next rising edge of the system clock.

The state machine controls the sample sequence following the pattern described in Figure 12. The multiplexing of the state machine is illustrated in Figure 14. For more details on the jump sequence, refer to Figure 15 on page 11.

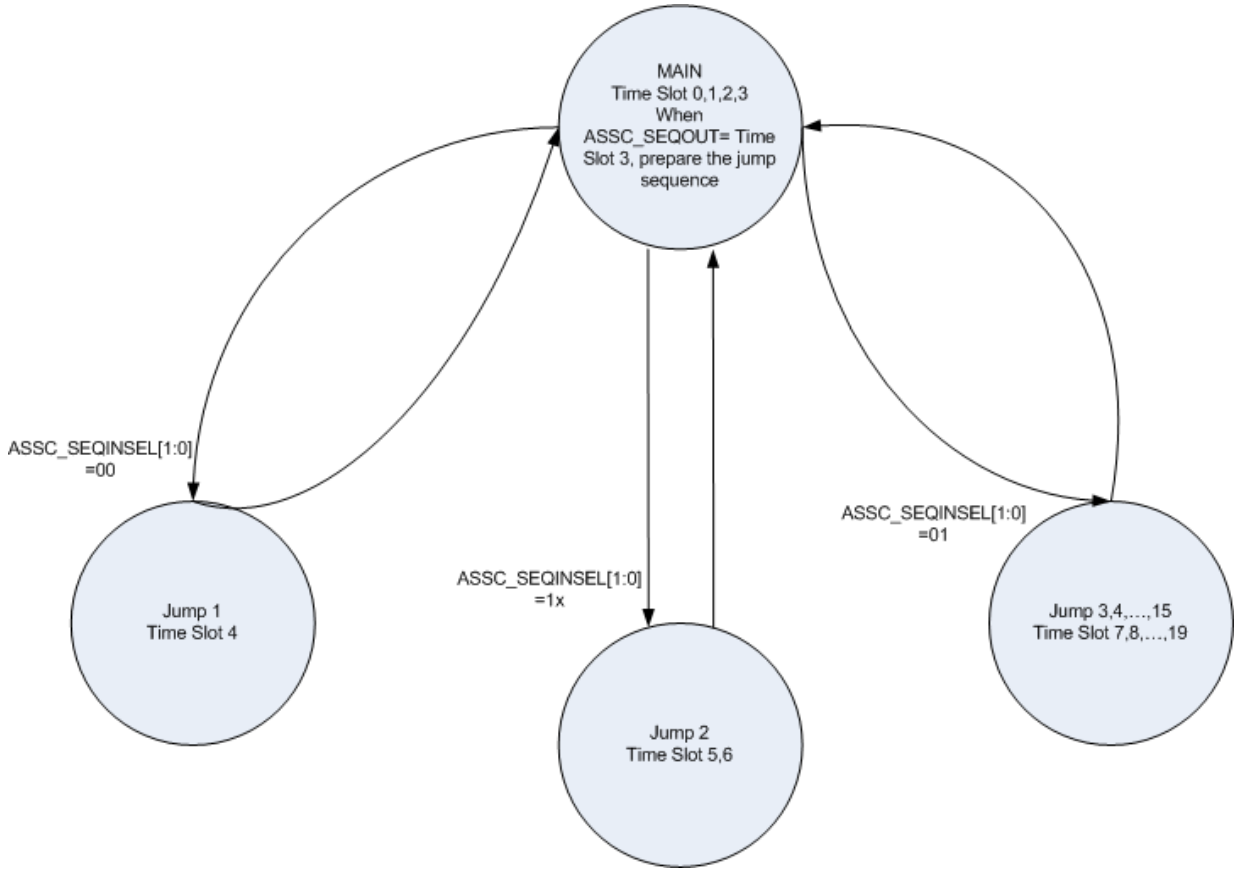

Figure 14 • **Figure 10. State Machine Multiplexing Scheme**

This design contains 20 active channels and 20 sample time slots. By controlling the ASSC_SEQINSEL[1:0] signal, the state machine sets the ASSC_SEQIN value that dictates the next time slot, or sample sequence number. Volt[4:1] are in the *main* procedure and they are sampled by default, so their corresponding time slot values 0-3 are not directly controlled by this state machine. Value 4 triggers time slot 4, or *jump1* (Volt[5]). Value 5 triggers time slot 5 and 6 for *jump2* (Volt[5:6]). The counter outputs 7 to 19 are for time slots 7 to 19, which trigger *jump3* to *jump15* respectively. For more details on the state machine, refer to the sample design files. Figure 15 shows the simulation result.

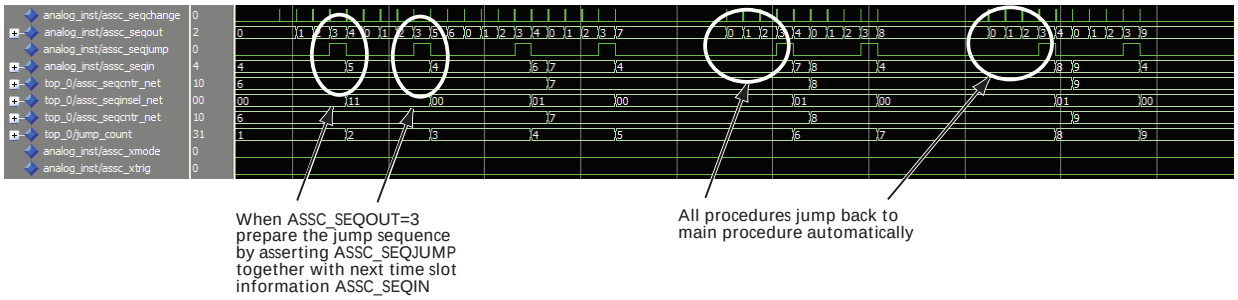

***Figure 15* • Simulation Result**

Summary

Fusion ADC throughput is determined by conversion time and turnaround time. Individual channel's conversion time, turnaround time, and sample rate (throughput) can be calculated by the *sample_rate_calculator.xls* spreadsheet with system clock frequency, ADC resolution, and required acquisition time info.

In designs with many active channels in which some have much higher throughput requirements than others, the ASB may not be able to meet all requirements. Users need to assign more time slots to sample higher throughput requirements for some channels than others. If the accumulated time slot number overflows the limit of a single procedure, users can create multiple procedures and jump sequences to achieve the desired throughput.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision	Changes	Page
Revision 1 (March 2015)	Non-technical Updates.	N/A
Revision 0 (June 2009)	Initial Release.	N/A

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