Bidirectional Level Shifter

Table of Contents

Introduction

Semiconductor technology advancements, proliferating I/O standards, legacy support requirements, and the relentless drive to design and manufacture lower power systems require most applications to utilize a mix of power supply and I/O drive voltages. Today's lower power devices have to work in this ecosystem with the older, higher voltage devices, requiring solutions that interface with the multiple voltages that are in widespread use today. Level-translator integrated circuits (ICs) are a common solution, but they do not necessarily provide the flexibility to support multiple simultaneous translations to different voltages or I/O interface standards. Level-translator ICs can add unnecessary cost if the system already contains an FPGA on board.

All IGLOO® and ProASIC®3 low power FPGAs support multiple voltage options for I/O banks. The input/output supply voltage (VCCI) of each bank determines the voltage level of it is I/Os. The IGLOO series of FPGAs supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V mixed-voltage operations, including several flexible wide range I/O voltage options. In addition to these features, flash-based IGLOO FPGAs also offer other unique features, such as high reliability, being a single-chip solution, live at power-up, nonvolatile, and available in small footprint packages. These features make IGLOO devices more suitable for level-translator applications than SRAM-based CPLDs/FPGAs. IGLOO and ProASIC3 low power FPGAs can also be used as unidirectional or bidirectional level shifters. Examples are 3.3 V to 2.5 V or 2.5 V to 3.3 V level translations. Refer to the *Level Shifter Design Example* application note for more details on the unidirectional level shifter.

The level translator used in a bidirectional digital circuit such as the I^2C bus must also be bidirectional with no requirement for a direction control signal. This application note describes the design of a bidirectional level shifter on an IGLOO FPGA with no direction control signal, although the design can be easily adapted to work with any of the Fusion, ProASIC3, or SmartFusion devices. This bidirectional level shifter design example provides a low cost, low power, highly flexible solution that utilizes IGLOO low power FPGAs.

Design Example Overview

This design example demonstrates the bidirectional level shifter with no direction control signal using the IGLOO nano Starter Kit. Figure 1 shows the system-level interface signals used in this design example. Bidirectional PAD A is connected to ASIC A with 3.3 V signaling; bidirectional PAD B is connected to ASIC B with 1.2 V signaling.

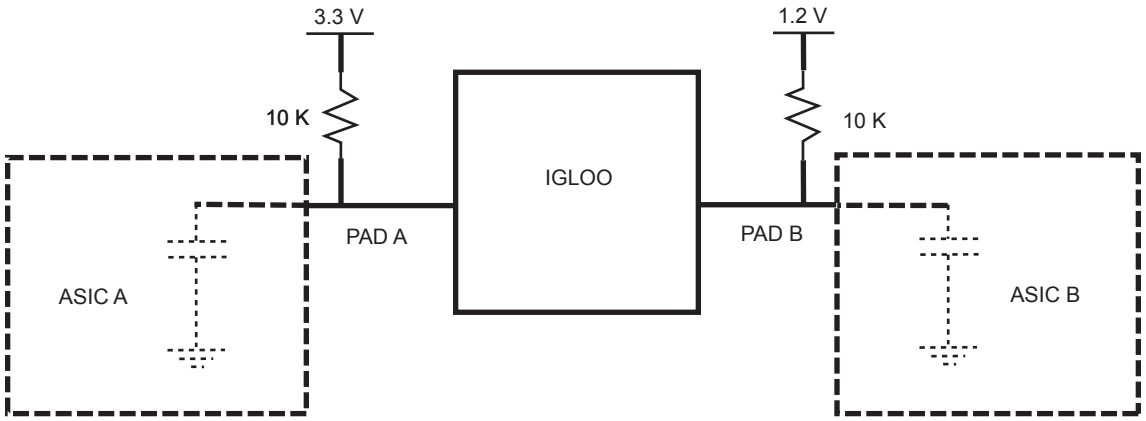

Figure 1 • **System Level Interface Signals**

Description of the Design Example

Figure 2 shows the bidirectional level shifter circuit diagram, which consists of an active high latch with active high preset and clear, bidirectional buffer, 2-input OR gate, inverter, and 2-input AND gate. All these components are available for IGLOO, ProASIC3, SmartFusion, and Fusion devices. Refer to the *IGLOO, ProASIC3, SmartFusion and Fusion Macro Library Guide* for more details.

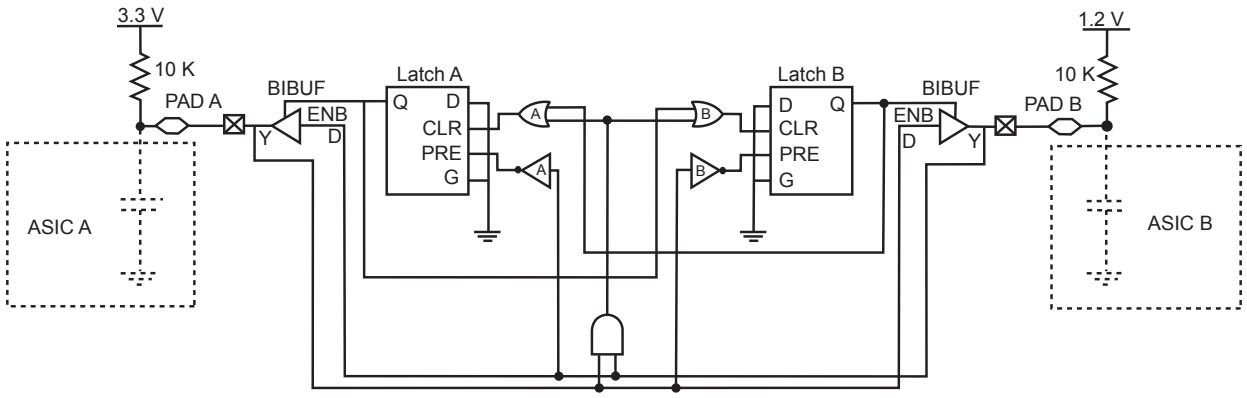

Figure 2 • **Bidirectional Level Shifter Circuit Diagram**

Operation of the Bidirectional Level Shifter

The following states are considered for explaining the operation of the bidirectional level shifter (Table 1).

Table 1 • **Bidirectional PAD States**

Sl No.	PAD A States	Latch A State	PAD B State	Latch B State
1	Hi-Z	0	Hi-Z	0
2	Hi-Z -> (drives)	0	Hi-Z -> 0	1
3	0 -> 1 (drives)	0	0 -> 1 -> Hi-Z (External pull-up that pulls the PAD B High)	1 -> 0
4	Hi-Z -> 0	1	Hi -> Z -> 0 (drives)	0
5	0 -> 1 -> Hi-Z (external pull-up that pulls the PAD A High)	1 -> 1	0 -> 1 (drives)	0

- Initially both PADs are in tristate (Hi-Z). The AND gate output clears Latch A and Latch B via the OR gates, which in turn tristates PAD A and PAD B. This state is continued until any of the PADs are driven externally by a 0 input.
- When any of the PADs are driven externally from Hi-Z to 0, the latch on the other side is RESET, enabling bidirectional pad. Hence 0 is transferred to the other output.
- When any of the PADs are driven externally from 0 to 1, then 1 is transferred on the other pad. This starts charging the load driven by the other pad. When the output voltage level reaches above threshold, the AND gate output goes High. This clears Latch A and Latch B, leaving the output in Hi-Z state.

Both Verilog and VHDL design files are provided (refer to "Appendix A – Design Files" on page 4) with this design example. IGLOO FPGAs support several drive strengths and slew rates. You can choose these parameters while running Designer in Libero IDE, based on the characteristics of the chips that need to be driven.

Figure 3 shows the bidirectional level shifter output waveform for the 1.2 V to 3.3 V translation at 400 KHz clock frequency. The green waveform indicates the input clock frequency with 1.2 V signaling and the yellow waveform indicates the output with 3.3 V signaling. The delay between input and output is measured as 8 ns under typical conditions.

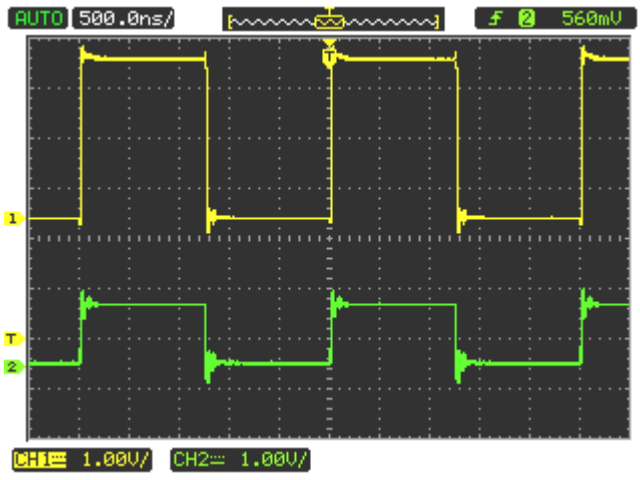

Figure 3 • **Voltage Translation from 1.2 V to 3.3 V**

If the external circuit has high capacitance and must be charged by a Strong One, the BUFD macro can be used to delay the Hi-Z state on the output, as shown in Figure 4.

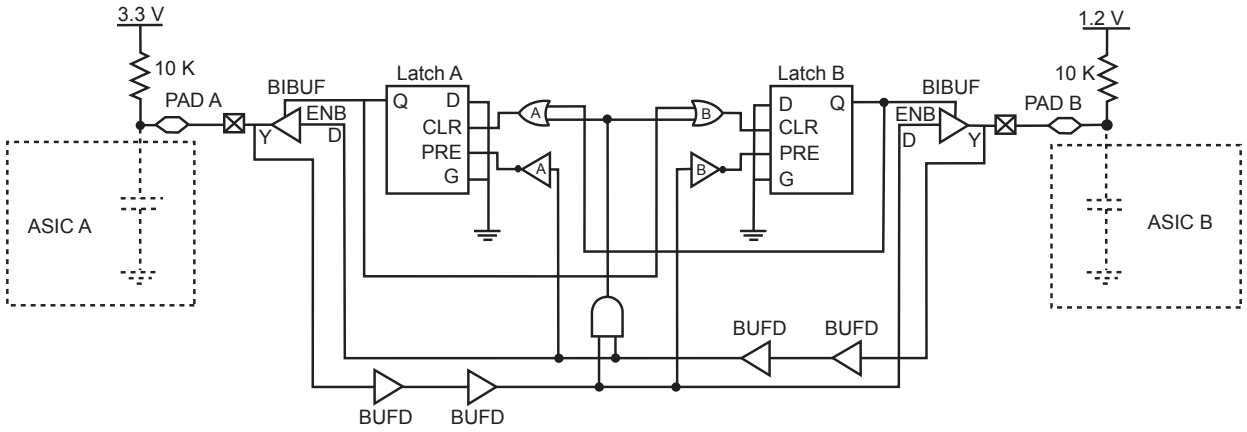

Figure 4 • **Bidirectional Level Shifter with Input Path Delay**

Figure 5 shows the bidirectional level shifter output waveform for the 1.2 V to 3.3 V translation at 400 KHz clock frequency with two BUFD delay macros.

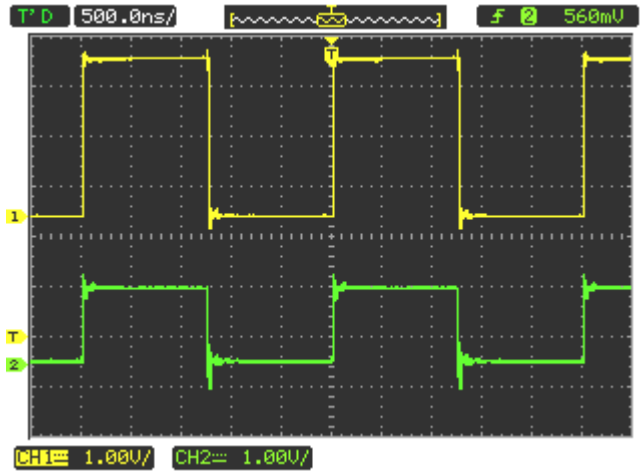

Figure 5 • **Voltage Translation from 1.2 V to 3.3 V with Two BUFD Delay Macros**

Conclusion

This application note discussed the need for level shifters and the use of IGLOO and ProASIC3 low power FPGAs for multiple simultaneous translations to different voltages or I/O interface standards. The design example demonstrated a bidirectional level shifter with no control signal on an IGLOO FPGA, although the design can be easily adapted to work with any of the Fusion, ProASIC3, and SmartFusion devices.

Appendix A – Design Files

The design files are available for download at www.actel.com/download/rsc/?f=IGLOO_AC349_DF.

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