AC292
Application Note
IBIS/IBIS-AMI Models: Background and Usage

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.0

Added chapter IBIS-AMI Models: Background and Usage, page 11.

1.2 Revision 3.0

Reliability information has been added to the I/O Source and Sink Currents, page 9.

1.3 Revision 2.0

There were no changes to the technical content in revision 2.0 of this document.

1.4 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Overview

For better understanding of the signal integrity on printed circuit boards (PCBs), hardware designers often need to simulate the design with I/O characteristic models. The designer must carefully consider signal integrity issues such as deformation of electronic signals as they travel on the PCB, cross talk, groundbounce and simultaneously switching outputs (SSO).

Input/Output buffer information specification (IBIS) models developed to address the above issues by providing I/O parameters in analog terms.

IBIS algorithmic modeling interface (IBIS-AMI) models required to simulate multi-gigabit serial links having very large bit streams with very fast and accurate equalization models. A high-speed digital system uses various signal processing techniques within transmitter and receiver to achieve high data rate. It provides a standard mechanism for modeling Tx/Rx equalization and clock recovery algorithms for SerDes transceiver. IBIS-AMI models are used to predict a serial link performance with an eye diagram and bit error rate.

Traditional SPICE models are slow and it is not useful to simulate Gigabit channels which needed fast and accuracy. IBIS-AMI model is a emerging preferred approach to simulate in most efficient way and can be used when different chip manufacturers are used at each end of the link.

This application note explains how to use IBIS models. In addition, this document discusses information contained in an IBIS model, explains what can be extracted from the model and provides examples of Microsemi IBIS models.

3 IBIS Models: Background and Usage

3.1 Background

IBIS is the input/output buffer information specification from the electronics industry alliance. It is a modeling technique that provides a simple table-based buffer model for semiconductor devices. The IBIS models can be used to characterize I/V output curves, rising/falling transition waveforms, and package parasitic information of the device. However, it is important to note that an IBIS model is intended to provide non-proprietary information about I/O buffers; it is not a delay model for timing analysis purposes. Generation of IBIS models is part of the documentation package of new field-programmable gate array (FPGA) devices. Designers able to save time by easily generating prototype circuit boards even before they receive the device. This enhances time-to-market for their products. SPICE models can be used to model various components on PCBs. However, the SPICE netlist of the I/O transistors of various components contains proprietary information. Furthermore, there are many different SPICE formats in the industry today, and not all are compatible with one another. This method is also time consuming and therefore, a non-proprietary component model was needed for rapid simulations. IBIS is that model.

3.2 IBIS Characteristics

3.2.1 Operating Conditions (Typical/Minimum/Maximum)

In a IBIS model, three device conditions are usually specified: typical, minimum, and maximum. The simulations obtained within the IBIS model have the minimum and maximum ranges being the boundaries and the typical being the nominal range/value.

The following table summarizes the three conditions.

Table 1 • **Ranges and Operating Conditions**

Range	Operating Condition	Temperature	%VCC
Minimum	Weakest	High, 70 °C	90% VCC
Typical	Nominal	25 °C	VCC
Maximum	Strongest	Low, 0 °C	110% VCC

Refer to the waveforms in Figure 2 on page 5, showing the simulated values in the three ranges.

Notice that the minimum range occurs at the I/Os maximum temperature, whereas maximum range occurs at minimum temperature. Designers must be careful while analyzing the data, bearing in mind that the temperature range would be different for military vs. industrial vs. commercial.

3.2.2 File Structure

A standard IBIS model file consists of three sections:

- **Header info**: Contains basic information about the IBIS file and what data it provides.
- **Component, package, and pin info**: Contains all information regarding the targeted device package, pin lists, pin operating conditions, and pin-to-buffer mapping.
- **V-I behavioral model**: Contains all data to recreate I-V curves as well as V-t transition waveforms, which describe the switching properties of the particular buffer.

Microsemi IBIS file contains the following information for each section, as shown in the following table.

Table 2 • **Typical Contents of an Microsemi IBIS File**

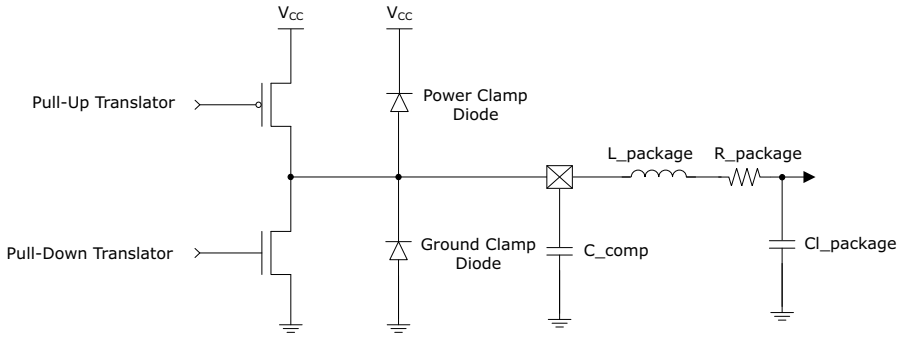
Header Information	Component, Package, Pin Information	Model
IBIS version	Component	Model Type
File name	Manufacturer	Temperature Range
File Revision	Package	Voltage Range
Date	Pin	Pull-down, Pull-up, GND Clamp, and POWER Clamp reference
Source	Pin Mapping	Mapping Ramp Rate
Notes		Rising/Falling waveform
Disclaimer		
Copyright		

3.3 IBIS Overview

3.3.1 Buffer I/V Characteristics

Every signal pin on an Microsemi FPGA contains a CMOS buffer that can be configured as an input, output, or bidirectional buffer. A simplified output buffer schematic is shown in Figure 1, page 4. When the PMOS output transistor turns OFF and the NMOS transistor ON, the output is placed in logic low.

Figure 1 • **Simplified Output Buffer Schematic**



When the PMOS transistor is turned ON, and the NMOS device is OFF, the output is placed in logic high. With both turned off, the output is in a high impedance state.

Table 3 • **Buffer Logic State Conditions**

PMOS	NMOS	Logic State
Off	On	Logic low
On	Off	Logic high
Off	Off	High impedance

Furthermore, the output buffer features GND and power clamp diodes. The main purpose of these diodes is to maintain the output buffer voltage between 0.7 V below ground (when logic low) and 0.7 V above VCC (when logic high). These diodes start to conduct when the pin is driven outside these limits. It must mention that for Microsemi device families with Hot Swapping I/Os there is additional circuitry that affects the operation of the diodes; specifically, the power clamp diode. The last portion of the buffer

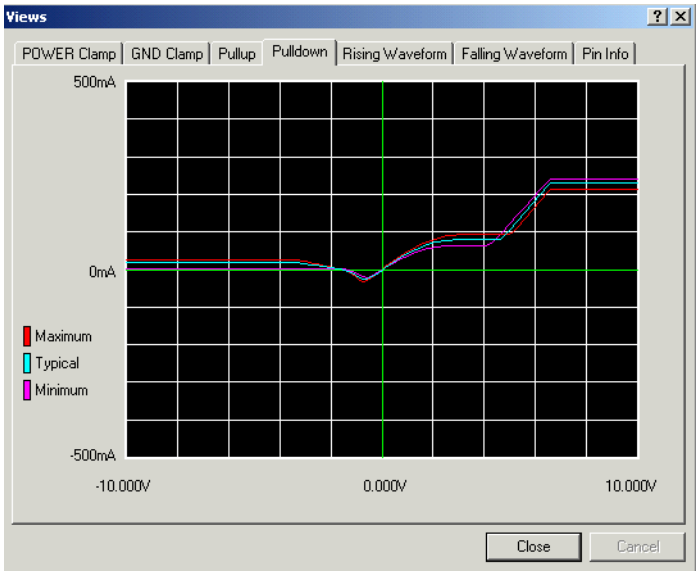
includes the capacitance of the silicon die (C_comp), the resistance (R_package), the inductance (L_package) and the capacitance (C_package) of the bond lead and package pin.

3.3.2 IBIS I/V Curves

By slowly increasing the voltage with an ammeter and voltmeter connected at the buffer, four different I/V curves can be derived. They are pull-up, pull-down, GND clamp, and power clamp curves. Since a buffer measurement is carried out with three configurations (min, typ, and max), the result is a set of 12 IBIS I/V curves.

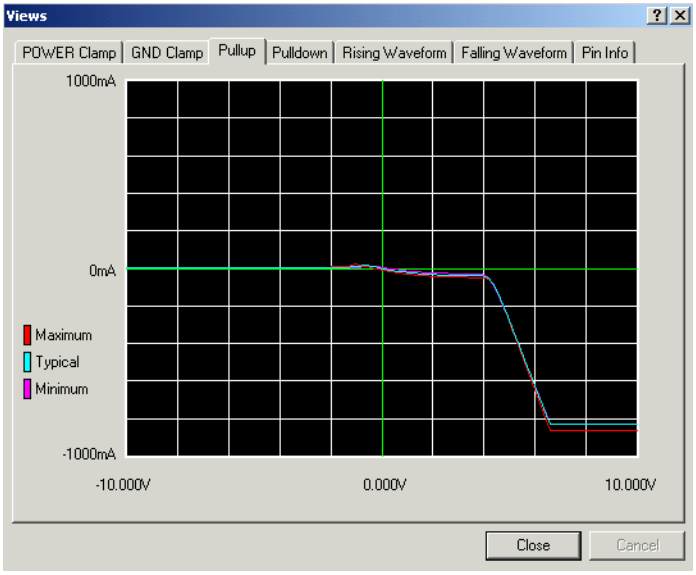
For MX and older FPGA families, the I/V curves are based on measured data but not the SPICE netlist. For SX and newer products (SX-S, SX-A, eX, and ProASIC) the curves are only based on SPICE models. The pull-down curve is a result of subtracting the GND clamp I/V curve from the logic-low I/V curve, since the pull-down transistor is active, as shown in the following figure. The full range of the measurement is from –VCC to 2VCC, which is the possible range of voltages that the output could see in a transmission line environment.

Figure 2 • **Sample Pull-Down Curve**



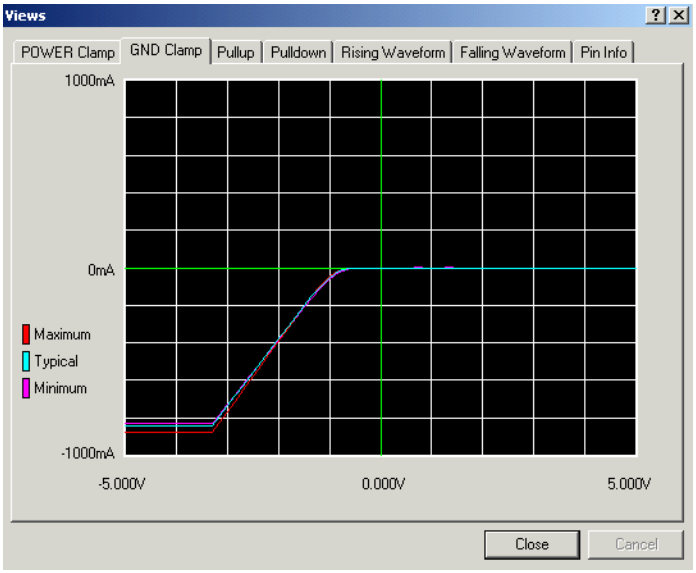
Similarly the pull-up curve is generated by subtracting the power clamp I/V curve from the logic-high I/V curve, since the pull-up transistor is active, as shown in the following figure. Again, the full range is from –VCC to 2VCC.

Figure 3 • **Sample Pull-Up Curve**



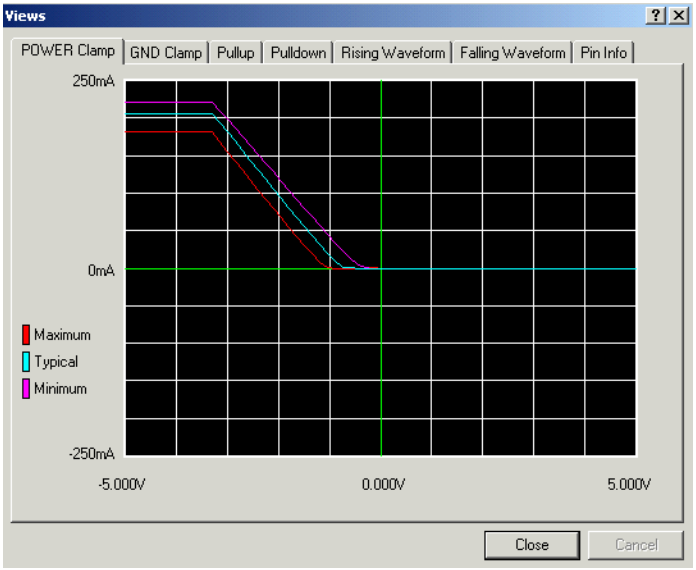
The GND clamp curve is derived from the ground relative data gathered while the buffer is in the high impedance state, and it shows the region where the ground clamp diode is active, as shown in the following figure. The range is from –VCC to VCC.

Figure 4 • **Sample GND Clamp Curve**



The power clamp curve is derived from the VCC relative data gathered while the buffer is in a high impedance state, and it shows the region where the power clamp diode is active. This measurement ranges from VCC to 2VCC, as shown in the following figure.

Figure 5 • **Sample Power Clamp Curve**



The pull-up and power clamp curves are VCC relative, meaning that the voltage values are referenced to the VCC pin. The output current of a pull-up or power clamp configuration depends on the voltage between the output and VCC pin but not the voltage between the output and ground pins. The voltages in IBIS data tables are derived from the following equations:

V_{table} = VCC – V_{output} (for pull-up and power clamp)

V_{table} = V_{output} (for pull-down and GND clamp)

Therefore, for a 3.3 V component, –3.3 V in the table means an actual +6.6 V on the output pin, and so on.

The preceding samples of each of four types of IBIS I/V curves were generated using Hyperlynx IBIS Viewer. The flat end portion of the curves is due to the current clamping during the measurement.

For Microsemi SmartFusion2/ Igloo2 devices:

- All MSIOs have clamp diodes and a circuitry to inhibit the power clamp diode. This circuit inhibits the diode if the voltage across the diode exceeds the forward voltage of the diode. For PCI this circuitry is disabled and thereby the power clamp functions normally. This enablement/disablement happens with flash bits.
- The clamp diodes for the MSIOs could draw a small amount of current in a short amount of time (before the clamp inhibit circuit inhibits the diode). This has negligible effect on the functionality of the hot insertion feature for these I/Os and has no impact on reliability. This behavior may be seen in IBIS models (clamp curves) and can be safely ignored.

3.3.3 IBIS Transition Waveforms

The IBIS model can also provide rising and falling V-t waveforms, which shows the transitions from GND to VCC and from VCC to GND. These curves are always taken from Spice simulations. The ramp rates are taken when the output voltage varies from 20% to 80% VCC (rising), and from 80% to 20% VCC (falling). The following figures show the rising and falling waveforms, respectively (generated using Hyperlynx). Designers must notice that the ramp rates given by [Ramp] in the IBIS file are different from slew rates. In calculation of the ramp rates, the package parasitics are ignored. These ramp rates are much faster than slew rates in which the package parasitics are taken into account.

Figure 6 • **Sample Rising Waveform**

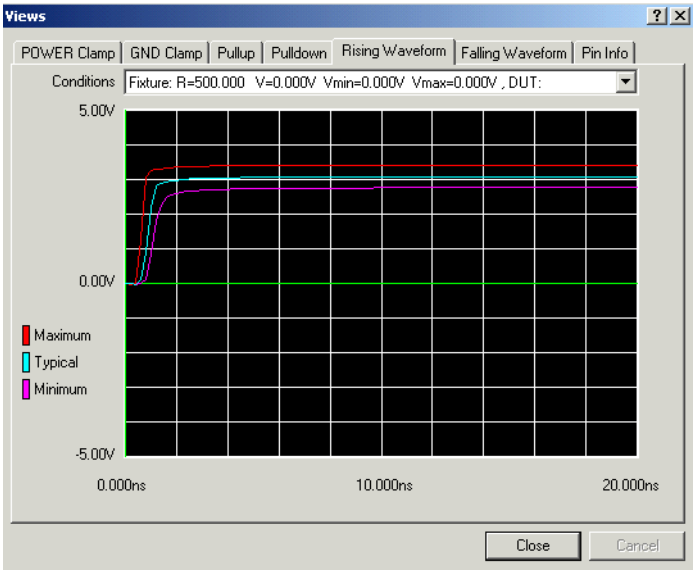
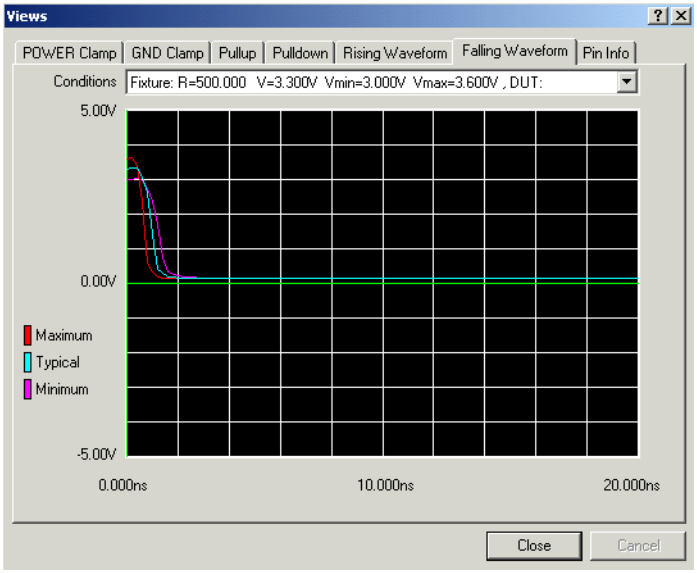


Figure 7 • **Sample Falling Waveform**



3.4 How to Use Microsemi IBIS Models

Microsemi developed many different families of Antifuse and flash-based FPGAs. They come in a variety of packages. However, IBIS models for Microsemi products are developed with a single model pin, called ALLIO. This pin can serve as a signal pin during board level simulations and can model all of the I/Os on the device. The designer simply replicates the pin as many times as needed to suit the design. For each Microsemi family, IBIS models are created for each I/O mode, then the package parasitics for all allowable packages are included in the IBIS model. The designer can simply uncomment the applicable package parasitics before performing simulation and analysis. Different IBIS simulators are available in the industry today, some of the vendors include:

- Cadence
- Mentor
- Microsim
- VeriBest
- Innoveda (Hyperlynx)

3.4.1 Information Extracted from an IBIS Model

IBIS data can be exploited to extract useful information on I/O characteristics. One is determining the current drive capability of the I/O in terms of source and sink currents. Another is defining a simple I/O equivalent circuit for board-level calculations.

3.4.2 I/O Source and Sink Currents

Source and sink currents are two important characteristics of I/O buffers. IBIS pull-up and pull-down I/V data are reliable sources to determine the source and sink currents, respectively. However, note that the source and sink currents obtained from IBIS models are not suitable for reliability assessment. In other words, the IBIS models merely represent the I/V characteristic of the I/O buffers but do not take into account reliability factors such as electro-migration. Sink current at a particular voltage can be obtained from the pull-down minimum current (Imin) set of IBIS data. Similarly, the minimum current extracted from pull-up data is a reliable source for determining the source current of the I/O for each voltage level. For example, the IBIS file for the SX-A device family illustrates that the device is capable of sourcing and sinking 35 mA and 30 mA, respectively, at a 3.3 V LVTTL operating voltage based on the following equations:

V_{table} = 3.3 V–VOH (min) (for source current)

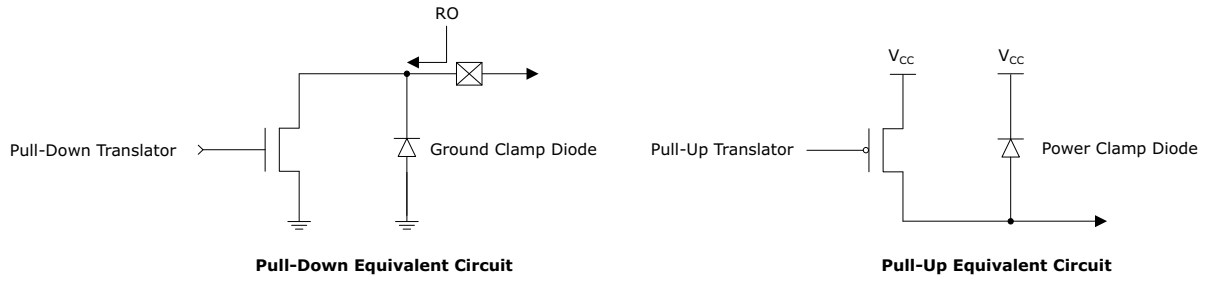
V_{table} = VOL (max) (for sink current)

To derive more accurate estimates for source and sink current, the effect of clamp curves should be taken into account. However, Power and GND clamp diodes have minor effects within the operational range of voltage.

3.4.3 Simple I/O Equivalent Model

Many designers find it very useful to replace the I/O buffer with a simple equivalent circuit for board-level calculations. The most important parameter of this model is the output resistance, Ro, seen from outside of the pin. IBIS models themselves do not take package effects into consideration (during model generation). The package data is provided for the simulators only and therefore the IV data DOES NOT include effects of package parasitics.

Figure 8 • **Pull-Down and Pull-Up Equivalent Resistors**



To calculate Ro, the linear part of the pull-up and pull-down IBIS curves can be used. The first step is to locate the linear portion. For example in the pull-down curve of Figure 2, page 5, it can be seen that the I/V relation is almost linear in the 0 V to 1.5 V range. For voltages more than 2 V the current enters in saturation mode. The amount of the current in the linear range can be obtained either by the curve or IBIS file values. For the typical pull-down I/V curve, the value of Ro can be calculated as 1.35V / 53.4 mA = 25.2 Ù Similarly, a typical Ro for pull-up IBIS curve can be obtained as 1.35 V / 26.3 mA = 51.3 Ù. These impedances are only first order approximations. Also, all the curves that are ON, need to be taken into account, that is, pull-up + both clamps when driving a Hi and pull-down + both clamps when driving a Lo. However, the first order approximation provides enough accuracy for most of applications.

4 IBIS-AMI Models: Background and Usage

IBIS-AMI models required to simulate multi-gigabit serial links having very large bit streams with very fast and accurate equalization models. IBIS-AMI models are used to predict a serial link performance with an eye diagram and bit error rate.

4.1 File Structure

A high-speed serial link can be divided into transmitter, channel, and receiver functional blocks. An IBIS-AMI model consists of three parts for Tx and Rx:

- ***.ibs**: Represents the analog model of the IC and accounts for impedance mismatch between the Tx and Rx channels. Also, specifies the file names of .ami, .dll, and compilation platform.
- ***.ami**: It is the control interface to the executable model. Reserved and model specific parameters files are used by the signal processing functionality of Tx and Rx.
- ***.dll**: Executable file, algorithmic model in C++.

IBIS-AMI model is in the format of a standard IBIS model, as defined in IBIS Models: Background and Usage, page 3. The `.ibs` file contains keywords for referencing the algorithmic executable. Under the section (algorithmic_Model), algorithmic shared library file (.dll). The AMI parameter file and the operating system specific platform_compiler_bits declaration is given. The platform compiler bits define the operating system and compiler for the shared library file. The entry also defines whether the OS is 32 or 64 bits. IBIS supports multiple operating systems for the executable shared library. All supported versions of a given model are listed under the (algorithmic model). A top-level `.ibs` file references both Tx and Rx algorithmic files.

The IBIS algorithmic parameter file is a ASCII text file with an AMI extension. The parameter file contains two main sections:

- **Reserved_Parameters**: It define the models of standardized capabilities such as the Init_Returns_Impulse and GetWave_Exists declarations.
- **Model_Specific (optional)**: It is used to pass simulation parameters to the executable for controlling model specific settings such as equalization, CDR, and signal swing. The usage rules of the parameters listed under these keywords are controlled by the arguments (in, out, inout, and info).

The IBIS-AMI standard defines three functions, which provides a means of communication with an EDA tool.

- **Init ()**: is used to initialize the memory and compute impulse response of the device and communicate with an EDA tool. Analog channel is exercised in SPICE to produce an impulse response. Impulse response is convoluted with the bit stream to produce raw waveforms.
- **Getwave ()**: communicates the time domain voltage waveform between EDA tool and the IBSI-AMI model.
- Close ().

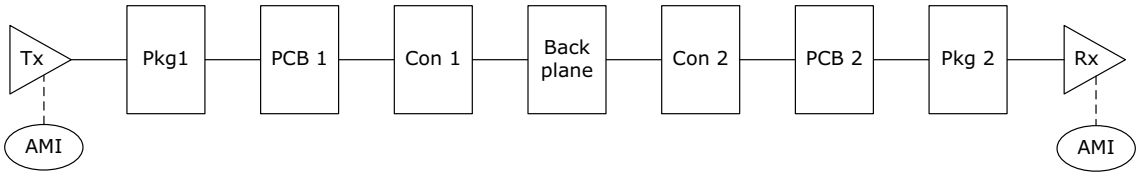
The IBIS-AMI standard, defines the communication mechanism between an EDA tool and the IBIS-AMI model. This standard does not provide any guidance on how to represent various signal processing blocks used to represent SerDes device, such as this is a feedback equalizer, feed forward equalizer (FFE), continuous time linear equalizer (CTLE) or transmitter de-emphasis.

All IBIS files are assumed to be located in the same directory so that the EDA tool can resolve the location pointers.

4.2 SerDes Channel Simulation Topology

The example of SerDes channel topology for the simulation is shown in the following figure.

Figure 9 • **SerDes Channe**



The high-speed SerDes interface has performance optimization in high-speed serial channels. The transmitter has pre and post-cursor controls for implementing pre and post emphasis. The receiver has a CTLE to compensate for channel loss. All these controlling features are available through the IBIS-AMI model and are user controllable.

4.2.1 SerDes Transmitter Equalization

The SerDes transceiver is equipped to provide a 3-tap transmitter equalizer. The equalizer pre-conditions the signal to compensate for any channel loss by boosting the high-frequency components (preemphasis) and suppressing the amplitude of the low-frequency components (de-emphasis).

Figure 10 • **Transmit Equalizer Block Diagram**

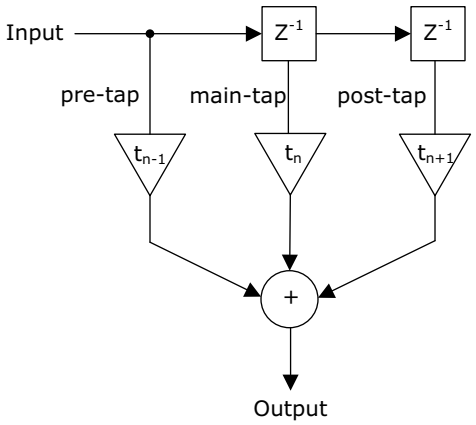
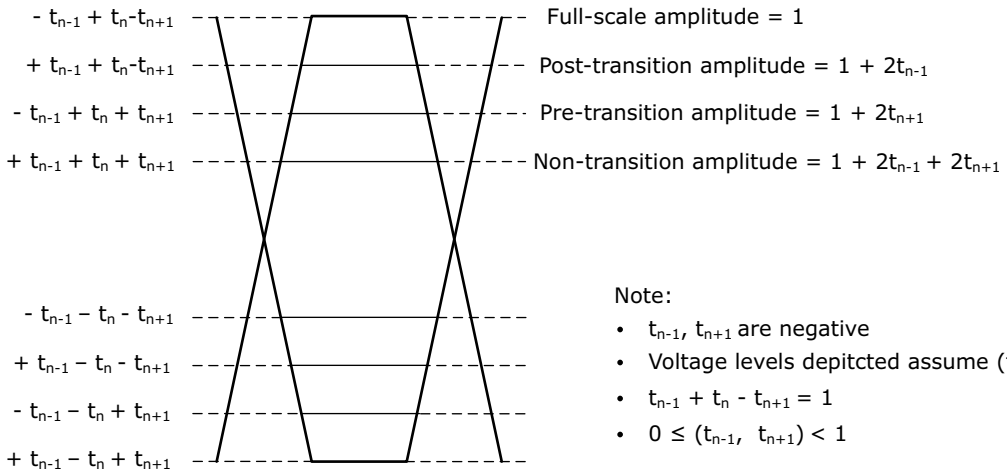


Figure 11 • **Transmitter Waveform**

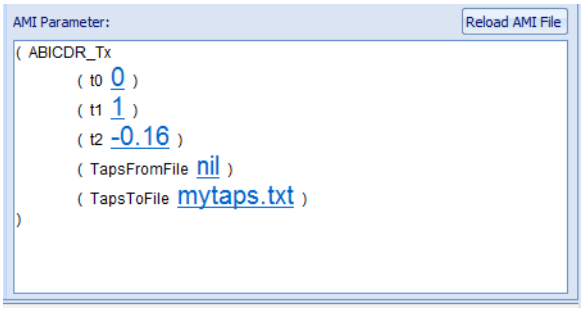


Note:

- t_{n-1}, t_{n+1} are negative
- Voltage levels depitcted assume (t_{n+1}) > (t_{n+1})
- t_{n-1} + t_n - t_{n+1} = 1
- 0 ≤ (t_{n-1}, t_{n+1}) < 1

The following figure shows the AMI parameters for Tx equalization settings.

Figure 12 • **AMI Parameters for Tx**



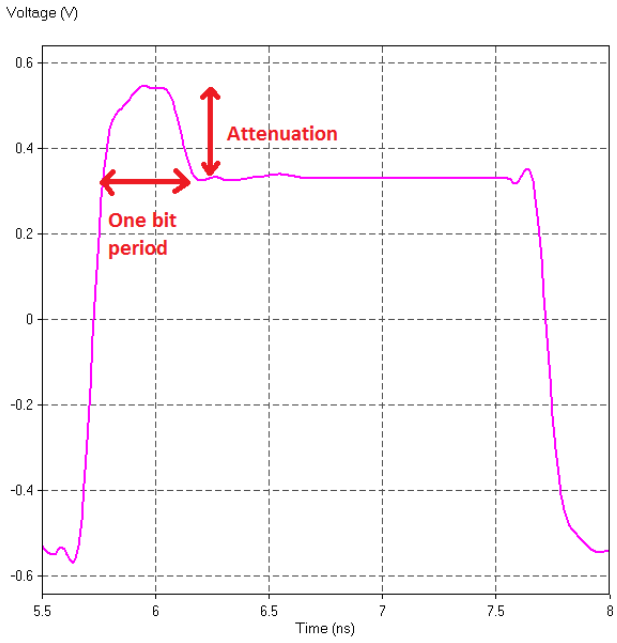
Transceiver contains 3-tap FFE filter settings, which are used to modify the transmitter waveform. A tap is a point at which the weighting is applied to each cursor. 3-tap equalization applies energy at the bit before and the bit after the main bit. The taps are named as t0, t1 and t2.

- t_0 (pre-cursor tap): The range is from -0.4 to -0.01 (default is -0.01); set to -0.01 for automatic generation.
- t_1 (main tap): The value is 1 (default: 1); set to 1 for automatic generation.
- t_2 (post-cursor tap); The range is from -0.5 to -0.01 (default is -0.01); set to -0.01 for automatic generation.

The following figure shows the effect of post-cursor. The attenuation controlled using the value from -0.5 to 0.0 corresponds to Zero attenuation.

Note: IBIS-AMI model does not support programmable transmit amplitude of -2.

Figure 13 • **Effect of Post-Cursor Tap**



The attenuation is calculated by using following equation:

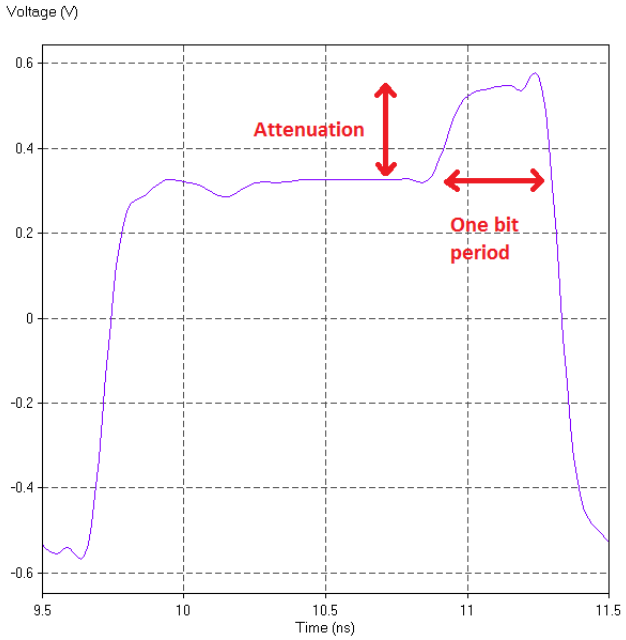
$$\text{Attenuation (De-emphasis in dB)} = 20 \times \log (1 - 2 \times \text{postCursor\_ratio})$$

EQ 1

The preceding equation is valid, only if main and post-cursor tap are used.

The following figure shows the effect of pre-cursor. The attenuation controlled using the value from -0.4 to 0.0 corresponds to zero attenuation.

Figure 14 • **Effect of Pre-Cursor Tap**



The attenuation is calculated by using following equation:

$$\text{Attenuation (De-emphasis in dB)} = 20 \times \log (1 - 2 \times \text{preCursor\_ratio})$$

EQ 2

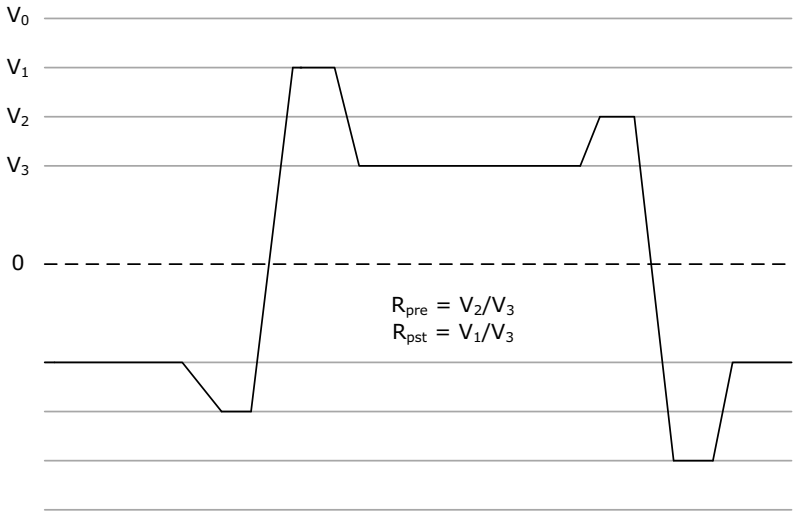
The preceding equation is valid, only if main tap and pre-cursor tap are used.

preCursor_ratio = - t_{n-1}

postCursor_ratio = - t_{n+1}

The following figure shows the transmitter output for 3-tap emphasis.

Figure 15 • **Example Transmitter Output for 3-tap Emphasis**



If both pre and post-cursor are used, the attenuation is calculated by the following equations.

$$Rpre = (1 - 2 \times postCursor\_ratio)/(1 - 2 \times preCursor\_ratio - 2 \times postCursor\_ratio)$$

EQ 3

$$Rpst = (1 - 2 \times preCursor\_ratio)/(1 - 2 \times preCursor\_ratio - 2 \times postCursor\_ratio)$$

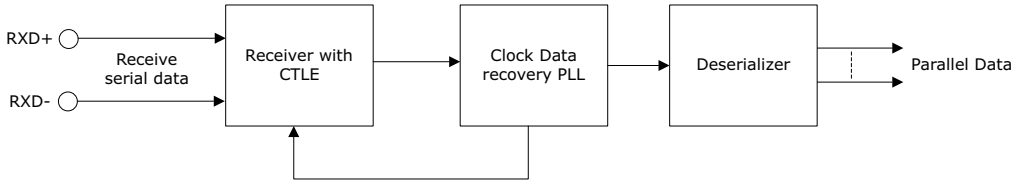
EQ 4

Designer to choose an appropriate value of de-emphasis for best overall system signal integrity. Designer must adjust the pre and post-cursor de-emphasis and simulate with SI tool. However, designer needs to know how to adjust these parameters for desired tx performance. For example, what must be the settings of t0, t1, and t2 to achieve -3.5 dB post-cursor de-emphasis.

4.2.2 SerDes Receiver Equalization

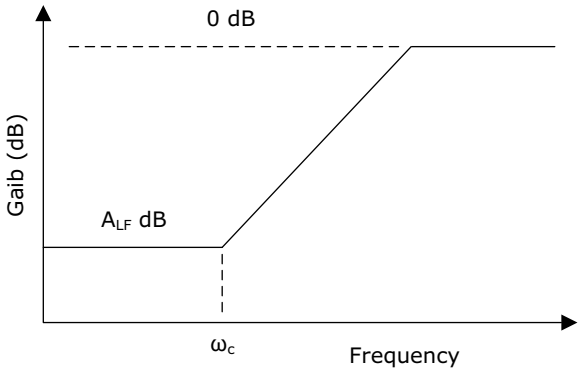
The receiver equalization is another signal conditioning feature to provide extra equalization for high loss channels. If channel is not high loss and enabling receiver equalization may adversely enhance the return loss due to discontinuities in channel. Board level simulation is required to determine whether the SerDes channels are in high loss condition, so that the Rx equalization is configured properly.

Figure 16 • **SerDes Receiver Block Diagram**



The SerDes receiver supports programmable single pole CTLE at the receiver. The CTLE within SmartFusion2/ Igloo2 devices, has no gain stages and it just uses attenuation filtering for linear equalization adjustments, as shown in the following figure.

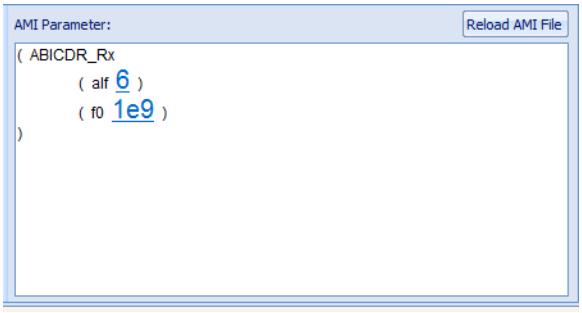
Figure 17 • **Receiver Equalization Frequency Response**



A_{LF} (low-frequency dB loss of the filter) and ω_c (high-pass cut-off frequency) can set by the user to maximize the signal quality of the receiver for achieving the highest possible bit error rate (BER).

- A_{LF}: The range is from 0 to 50; default value is 6.
- ω_c: The range is from 1e6 to 5e10; default value is 1e9.

Figure 18 • **AMI Parameters for Rx**



Qualification of simulation results is done based on the eye-height, eye-width, and BER curves. Check the eye-height and eye-width at target BER of 10e-12. These results are found in the report generated by the simulation tool.

The following table lists the possible receiver equalization combinations.

Table 4 • **Possible Receiver Equalization values**

rx_equalization_amp_ratio	rx_equalization_cut_frequency	ω_c (MHZ) rounded 10s place	A_{LF} (dB) round
103	12	200.00	9.54
74	17	200.00	12.04
57	22	300.00	13.98
47	27	400.00	15.56
40	31	400.00	16.90
119	32	400.00	10.88
119	31	500.00	8.52
103	37	500.00	12.04
35	36	500.00	18.06
103	36	500.00	9.54
91	42	500.00	13.06
31	41	500.00	19.08
91	41	600.00	10.46
81	47	600.00	13.98
27	46	600.00	20.00
81	46	600.00	11.29
74	52	600.00	14.81
25	50	600.00	20.83
74	50	700.00	12.04
70	55	700.00	15.56
23	55	700.00	21.58
67	55	800.00	12.74
64	60	800.00	16.26

Table 4 • **Possible Receiver Equalization values *(continued)***

rx_equalization_amp_ratio	rx_equalization_cut_frequency	ω_c (MHZ) rounded 10s place	A_{LF} (dB) round
21	60	800.00	22.28
62	60	800.00	13.38
60	64	800.00	16.90
19	64	800.00	22.92
128	69	900.00	11.48
57	64	900.00	13.98
55	69	900.00	17.50
18	69	900.00	23.52
120	74	900.00	12.04
53	69	900.00	14.54
52	74	900.00	18.06
5	245	900.00	24.08
112	79	1000.00	12.57
50	74	1000.00	15.07
15	254	1000.00	18.59
124	69	1100.00	8.20
106	84	1100.00	13.06
15	245	1100.00	15.56
116	74	1100.00	8.67
125	88	1100.00	11.60
35	254	1100.00	13.53
109	79	1200.00	9.12
44	249	1200.00	12.04
103	83	1200.00	9.54
55	254	1200.00	10.88
34	252	1300.00	9.95
75	254	1400.00	9.17
82	254	1400.00	8.52
95	254	1500.00	7.96
91	254	1500.00	7.47
115	254	1600.00	7.04
120	254	1700.00	6.66
72	254	1800.00	6.02

4.2.3 Configuring De-Emphasis Values in SI Configurator (Libero)

Tap settings provided in SI configurator are converted into equivalent register value of SerDes as shown in the following figures.

Figure 19 • **High Speed Serial Interface Configurator**

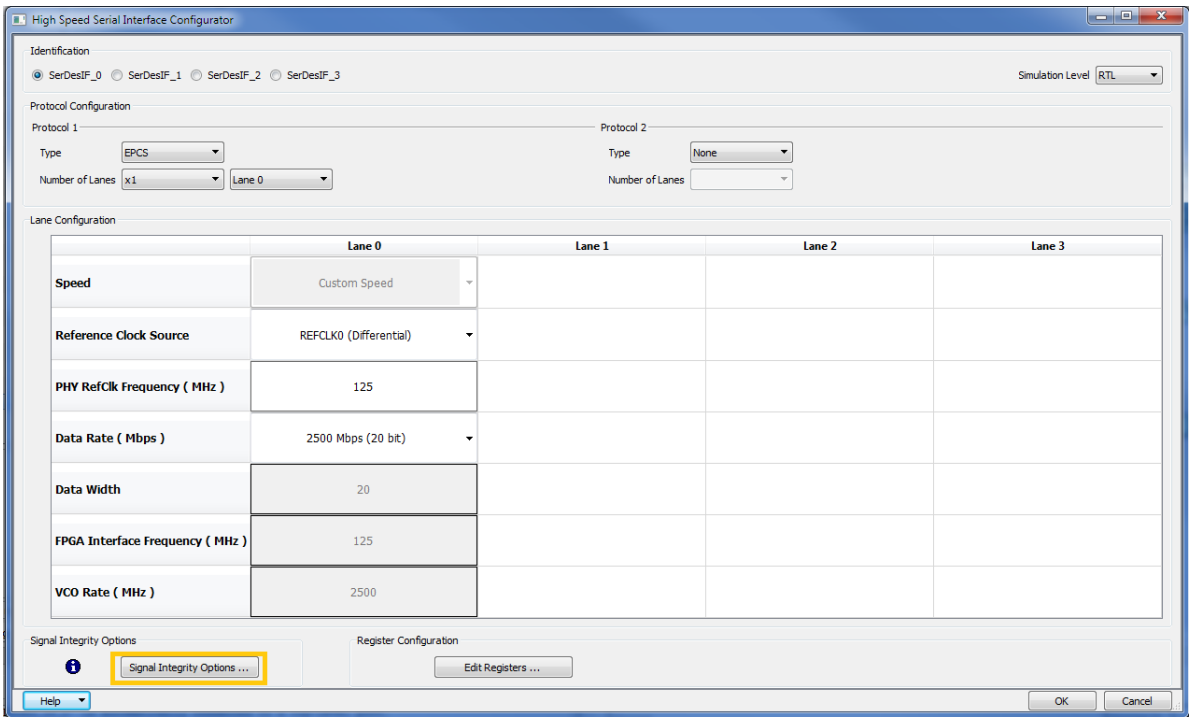
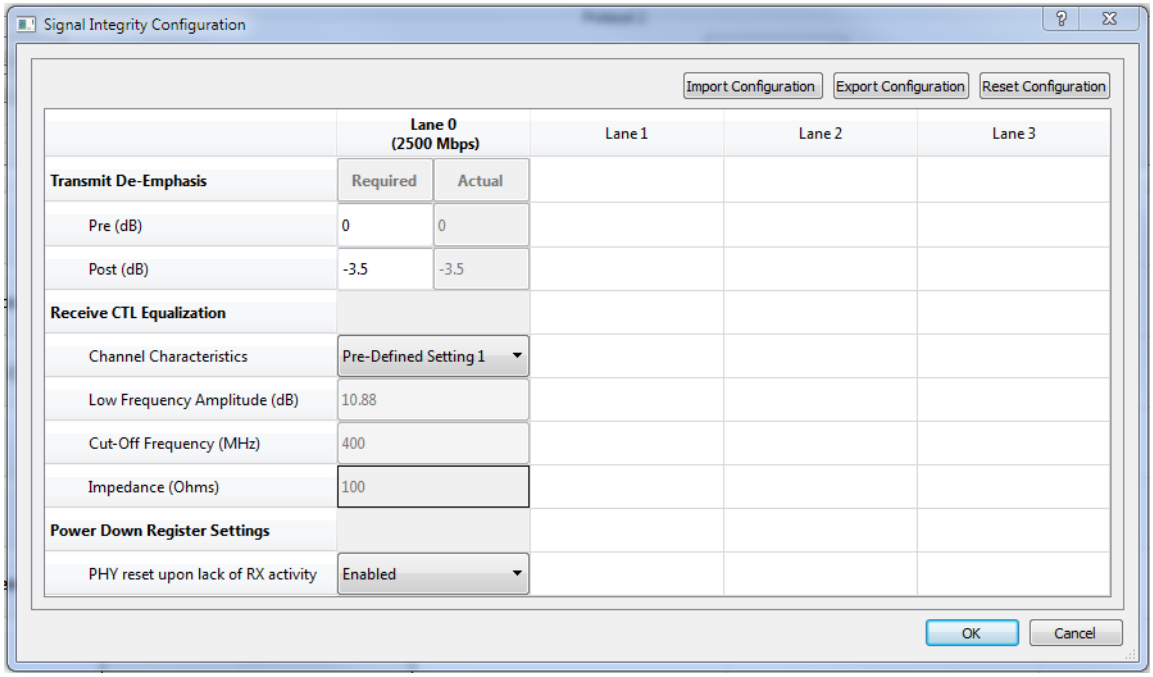


Figure 20 • **Signal Integrity Configuration**



For information on signal integrity options in Libero, see the *SmartFusion2 and IGLOO2 High Speed Serial Interface Configuration*.

4.3 Conclusion

Designers often need to prototype their PCBs before they have any devices to test. IBIS models allow designers to conveniently simulate I/O behavior and characteristics and thus more accurately analyze various components on their board. This is achievable through the generation of various I/V output curves, rising and falling transition waveforms, and package parasitic information. Microsemi IBIS models are internally developed, generated from SPICE simulations, and compared with the silicon data to model the real device as closely as possible. By providing Microsemi customers with the IBIS models, designers can analyze device I/O behavior before having the physical device available for test.

5 Appendix: Sample Microsemi IBIS File for the MX Family

```
|*********************************************************************
| IBIS file mx09_33v.ibs aided by s2ibis2 version 1.1
| North Carolina State University Electronics Research Laboratory 1995
|*********************************************************************
|
[IBIS ver] 2.1
[File name] mx09_33v.ibs
[File Rev] 2.x5
[Date] March 31 1998
[Source] V/I curve data extracted from silicon lab measurements. Ramp
data extracted from SPICE netlist. All performed at Microsemi.
[Notes] V/I max min curve data was measured in the lab under max and
min Vcc and Temp conditions. The measurements were done on
pre-production parts. Please see User's Area" section of
Microsemi Webpages for more information regarding product or
package data. Microsemi Homepage URL is http://www.Microsemi.com
Check for the availiability of a rev 2.1 mx09_33v.ibs in
September 1998.
[Disclaimer] This information is for modeling purposes only, and is not
guaranteed.
[Copyright] Copyright 1998, Microsemi Corporation, All Rights Reserved.
|
|*********************************************************************
| Component mx09_0.5um_33v
|*********************************************************************
|
[Component] mx09_0.5um_33v
[Manufacturer] Microsemi Corporation
[Package]
| variable typ min max
| Un-comment the appropriate package
|
|R_pkg 104m 97m 111m | PLCC 84
|L_pkg 10.3nH 8.29nH 12.31nH | PLCC 84
```

```
|C_pkg 2.04pF 1.84pF 2.24pF | PLCC 84
|…….cont'd
|
[Pin] signal_name model_name R_pin L_pin C_pin
ALLIO IO1_out ALL_IO_PINS
| 1_in IO1_in INPUT1
| 1_en IO1_en ENABLE1
GNDP GND GND
VCCI VCCI POWER
|
[Pin Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref
|
ALLIO GND VCCI GND VCCA
| 1_in NC NC GND VCCA
| 1_en NC NC GND VCCA
GNDP GND NC
VCCI NC VCCI
VCCA NC VCCA
|
|*****************************************************************************
| Model ALL_IO_PINS
|*****************************************************************************
|
[Model] ALL_IO_PINS
Model_type I/O
Polarity Non-Inverting
Enable Active-Low
Cref = 35.00pF
Vref = 0.000V
C_comp 2.40pF 2.48pF 2.33pF
Vinl = 0.8V
Vinh = 2.0V
|
|
[Temperature Range] 25.00 70.00 0.000
[Pullup Reference] 3.30V 3.00V 3.60V
[Pulldown Reference] 0.000V 0.000V 0.000V
[POWER Clamp Reference] 3.30V 3.00V 3.60V
```

```
[GND Clamp Reference] 0.000V 0.000V 0.000V
[Pulldown]
| voltage I(typ) I(min) I(max)
|
-3.30E+00 1.83E-02 3.00E-03 2.59E-02
-3.15E+00 1.67E-02 2.82E-03 2.37E-02
-3.00E+00 1.51E-02 2.64E-03 2.14E-02
|......cont'd
[Pullup]
| voltage I(typ) I(min) I(max)
|
-3.30E+00 3.46E-03 3.34E-03 5.58E-03
-3.15E+00 3.38E-03 3.52E-03 5.52E-03
-3.00E+00 3.72E-03 3.26E-03 5.80E-03
|......cont'd
[GND_clamp]
| voltage I(typ) I(min) I(max)
|
-3.30E+00 -8.41E-01 -8.31E-01 -8.80E-01
-3.15E+00 -7.87E-01 -7.79E-01 -8.23E-01
-3.00E+00 -7.34E-01 -7.28E-01 -7.67E-01
|......cont'd
[POWER_clamp]
| voltage I(typ) I(min) I(max)
|
-3.30E+00 2.06E-01 2.21E-01 1.81E-01
-3.15E+00 1.93E-01 2.09E-01 1.68E-01
-3.00E+00 1.81E-01 1.98E-01 1.55E-01
|......cont'd
|
[Ramp]
| variable typ min max
dV/dt_r 1.98/0.23n 1.80/0.26n 2.16/0.14n
dV/dt_f 1.98/0.28n 1.80/0.35n 2.16/0.25n
R_load = 1.00M
|
[Rising Waveform]
R_fixture = 0.50k
```

```
V_fixture = 0.000
V_fixture_min = 0.000
V_fixture_max = 0.000
| time V(typ) V(min) V(max)
|
0.000S 0.000V 0.000V 0.000V
0.20nS -17.96mV -12.51mV -26.17mV
0.40nS -27.82mV -27.72mV 12.14mV
|......cont'd
|
[Falling Waveform]
R_fixture = 0.50k
V_fixture = 3.30
V_fixture_min = 3.00
V_fixture_max = 3.60
| time V(typ) V(min) V(max)
|
0.000S 3.30V 3.00V 3.60V
0.20nS 3.32V 3.01V 3.63V
0.40nS 3.33V 3.04V 3.42V
|......cont'd
|
| End [Model] ALL_IO_PINS
|
| End [Component] mx09_0.5um_33v
|
[End]
```