Multi-Channel Analog Voltage Comparator in Fusion FPGAs

Introduction

The Actel Fusion™ Programmable System Chip (PSC), the world's first mixed-signal FPGA, integrates mixed-signal analog, Flash memory, and FPGA fabric in a monolithic PSC. Among many other analog and system management features, the Fusion PSC integrates a successive approximation register (SAR) analog to digital converter (ADC), configurable for 8-, 10-, or 12-bit modes of operation. Supporting the ADC are up to 30 analog inputs. The output of the ADC is available to the FPGA core.

This document assumes that the reader is familiar with Fusion, SmartGen, and SmartGen IP. Features, blocks, and applications described in the *Fusion Family of Mixed-Signal Flash FPGAs* datasheet are used in this application note. Readers are referred to the datasheet for further details.

The analog voltage inputs of Fusion FPGAs can be used in tandem to implement a multi-channel voltage comparator. This comparator (Figure 1) can be used to determine the difference between voltage signals.

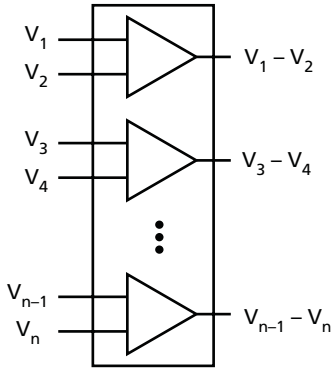

Figure 1 • **Multi-Channel Voltage Comparator with Voltage Difference Output**

As described in the *Fusion Family of Mixed-Signal Flash FPGAs* datasheet, in the analog block of Fusion PSC there is 32-to-1 MUX that selects the input of the ADC. Depending on the user design, if the MUX selection inputs are controlled directly by user access to the Analog Configuration MUX (ACM) or the user-defined sampling sequence in the SmartGen tool chain, the ADC converts one voltage input at a time and then moves to measure the next defined input. Therefore, in a voltage comparator application, the two compared voltages should be sampled successively to minimize any temporal distortion error. This is particularly important when the input voltage variation rate is comparable to the Analog Block (AB) sampling rate.

Once an analog signal has been sampled and converted, it can be retrieved by the user from three different locations:

1. ADC output directly

   In this case, ADC_CHNUMBER identifies the analog input that has been measured.
2. ADC Sample Sequence Controller (ASSC) RAM

   In this case, the ADC output is stored in the ASSC RAM (through SmartGen IP), in which specified addresses are allocated for each analog input.
3. System Monitor Evaluation (SMEV) RAM

   In this case, the averaged (or filtered) results for each analog input are stored in the SMEV RAM (through SmartGen IP), in which specified addresses are allocated for each analog input.

The voltage comparator in this application note is designed to get the analog voltage measurement results directly from the ADC output. This approach is slightly more complicated than other methods in which the ADC results are read from ASSC or SMEV RAM. In the ASSC or SMEV RAM blocks, analog voltage input conversion results are stored in specified addresses, whereas if the ADC output is accessed directly, there is only one digital output bus that is loaded with the latest conversion results. In this case, the ADC_CHNUMBER output of the AB defines which analog input the current ADC result corresponds to.

When ASSC or SMEV RAM blocks are used, the voltage comparators can be implemented easily by reading each voltage pair's values from the RAM (from each voltage pair's corresponding RAM address) and loading them into a subtractor.

Voltage Comparator Design Functionality

Figure 2 illustrates the high-level definition of the voltage comparator design. As shown in Figure 2, the inputs to the comparator are voltage pairs, each pair representing one comparison channel. The output of the voltage comparator design is composed of digital values showing the difference between the two inputs of a pair. The input pairs are designated with P and N polarity. The output of the comparator is simply a subtraction of voltage on the N port from the voltage on the P port.

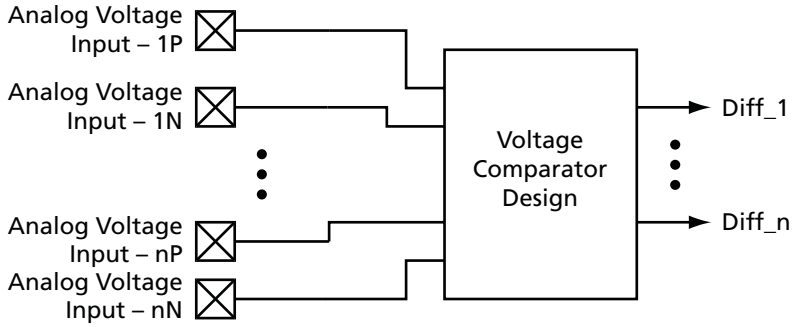

Figure 2 • **High-Level Definition of Voltage Comparator Design**

Inside the voltage comparator design of Figure 2, there is an AB, an embedded Flash memory block, and a state machine block. The embedded Flash memory performs the initialization of the AB after power-up. The core of the voltage comparator design is the state machine that connects to the AB, as shown in Figure 3.

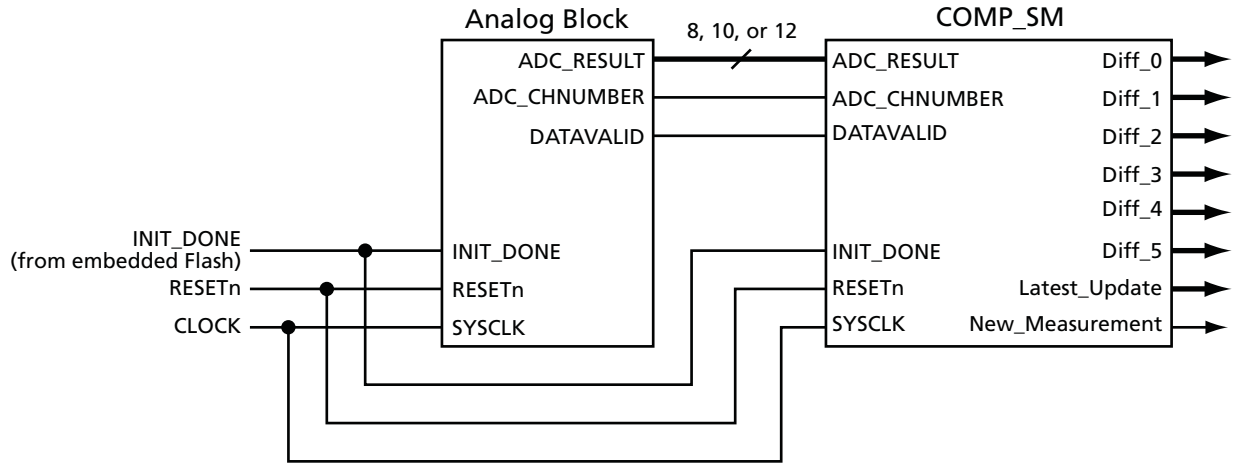

Figure 3 • **Voltage Comparator Design – Analog Block and State Machine**

Port Description of State Machine

The state machine in Figure 3 on page 2 (COMP_SM) has six inputs and eight outputs. The following is the description of these ports:

- ADC_RESULT (input): This port is directly connected to the ADC_RESULT output of the AB and is driven directly by the output of the ADC. The width of this port is 8, 10, or 12 bits, depending on the resolution of the ADC. The width of this port inside the state machine is set by a generic parameter, WIDTH, in the RTL.
- ADC_CHNUMBER (input): This is a 5-bit-wide port that is directly connected to the ADC_CHNUMBER output of the AB. It indicates to the state machine the analog channel number corresponding to the current value on ADC_RESULT.
- DATAVALID (input): This active high input indicates when the ADC conversion is complete and the ADC_RESULT value is valid. In the current design of the COMP_SM state machine, it is assumed that the DATAVALID input is active for only 1 clock cycle. This is compatible with the ASSC_DONE output of the AB. However, the DATAVALID output of the AB can be active for more than 1 clock cycle. In this case, a simple circuit (described in "Appendix" on page 6) can be used to convert the DATAVALID output of the AB to be compatible with the DATAVALID input of COMP_SM. If ASSC RAM is used, the DATAVALID input of COMP_SM can be directly driven by the ASSC_DONE output of the AB.
- INIT_DONE (input): Driven directly by the INIT_DONE output of the embedded Flash memory. Once the initialization of the AB is done after power-up, COMP_SM starts its normal functionality.
- RESETn (input): Active low system reset input
- SYSCLK (input): System clock input
- Diff_0 to Diff_5 (output): Comparator output results for each voltage input pair. The value on these outputs is the difference of each voltage pair. The width of this port is 8, 10, or 12 bits, depending on the resolution of the ADC. The width of this port inside the state machine is set by a generic parameter, WIDTH, in the RTL.
- Latest_Update (output): This 3-bit-wide output determines the Diff signal number that is most up-to-date (last updated).
- New_Measurement (output): Active high flag that is activated for 1 clock cycle every time a new comparator result is posted on any of the Diff_0 to Diff_5 outputs.

Functionality of COMP_SM Block

This section describes the functionality and implementation of the COMP_SM state machine.

Functionality of COMP_SM State Machine

The functionality of the COMP_SM block is summarized and illustrated in Figure 4 on page 4. The state machine starts off from an idle state monitoring the ADC_CHNUMBER and DATAVALID inputs to identify which analog voltage input of the Fusion device is being put out by the ADC. Once the ADC output corresponds to the "P" port of one of the comparators, the state machine registers the ADC result along with the channel number, moves to a waiting state, and waits for the next measurement from the ADC (by monitoring DATAVALID). At the next activation of the DATAVALID input, the state machine looks at the output channel number. If the new channel number does not correspond to the "N" port of the comparator whose "P" port was measured last, the state machine will invalidate the previous "P" measurement and move into the idle state. If the new ADC output matches the expected channel number, the state machine will record the new measurement and subtract it from the previous "P" port ADC result.

After completing the subtraction, the state machine will send the differential outcome to the corresponding output (Diff_n), indicate which output has been updated (Latest_Update port), and flag to the user that a new measurement is completed (New_Measurement).

After putting out the data, the state machine will move on and wait for another measurement from a comparator "P" port.

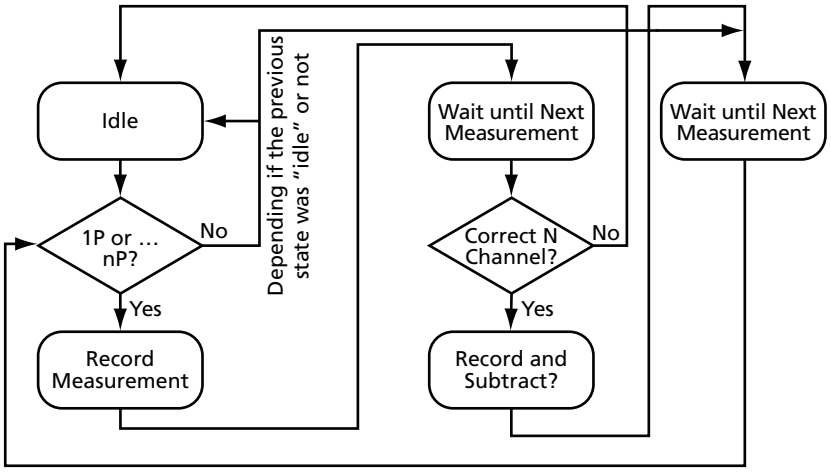

Figure 4 • **Functional Flow Chart of COMP_SM State Machine**

Implementation of COMP_SM State Machine

The COMP_SM state machine, as presented in this application note, consists of five states: idle, channel_xP, channel_xN, wait_next_result, and wait_next_channel. The following is a description of what these state are and how the flow chart of Figure 4 is implemented in them:

- idle: As mentioned in "Functionality of COMP_SM State Machine", the idle state is where the state machine start its operation. In addition, in the case of any error or unexpected behavior, the state machine moves into the idle state. At the idle state, all the measurement outputs (Diff_n) of the state machine will be reset to zero, and the Latest_Update output will be preset to '111' (users can modify this to their own requirements).
- channel_xP: Once the voltage on a "P" port of the comparator is put out by the ADC, COMP_SM moves into the channel_xP state. The state machine will remain in this state for only 1 clock cycle, in which the ADC outputs are recorded. On the next clock cycle, the state machine moves into the wait_next_result state.
- wait_next_result: This state is where COMP_SM waits between the "P" port and "N" port measurement of the AB. If the next ADC output is not from the expected "N" port, the state machine will move into the idle state as a sign of error. If the next ADC output is from the expected port, the state machine will move into the channel_xN state.
- channel_xN: Once the voltage on the expected "N" port of the comparator is put out by the ADC, COMP_SM moves into the channel_xN state. The state machine will remain in this state for only 1 clock cycle, in which the ADC outputs are recorded. On the next clock cycle, the state machine moves into the wait_next_channel state.
- wait_next_channel: The functionality of wait_next_channel state is very similar to the idle state. The only difference is that in this state (unlike the idle state), the outputs are not reset/preset. The state machine waits in this state till another "P" port of the comparator is measured by the ADC.

Specifications of COMP_SM Block

The COMP_SM block of the voltage comparator design is a simple state machine that can be easily modified to meet specific design requirements. However, the state machine as it is has some specifications that users should be aware of. This section of the application note describes these specifications and explains the modifications of the RTL code required to adjust them to match user-specific requirements.

Number of Comparator Channels

The current design, as shown in Figure 3 on page 2, supports six comparator channels (with twelve voltage inputs). If six or fewer channels are required, the unused outputs of the state machine can be left floating. If more output channels are required, the state machine design should be modified to support additional

outputs. In this case, users should also change the Latest_Update logic inside the state machine and its width (if the number of required channels is more than seven). The main Latest_Update logic inside the state machine is within the process in which the Latest_Update assignments are performed based on the ADC_CHNUMBER input.

Analog Input Channels

The state machine design assumes the analog voltage inputs to be from AV0, AC0, AV1, AC1, …, AV5, and AC5. It also assumes that AVn and ACn each form a voltage pair, where AVn and ACn are mapped to the "P" and "N" ports of the comparator (as defined in Figure 2 on page 2). These assumptions are critical, since ADC_CHNUMBER is used to determine the state machine operation according to the voltage measurements on each channel. If the user's design exploits different analog input ports from those specified above, the state machine should be modified accordingly. These modifications are to be done in statements in which ADC_CHNUMBER is compared against predefined channel numbers to define the next action of the state machine.

Sampling Sequence

In general, the state machine does not constrain any user-defined sampling sequence of analog inputs. However, it requires one specific condition: if the voltage input to the "P" port of the comparator input pair is measured and put out by the ADC, the next measurement must be on the "N" port of the same comparator. This is mainly to enhance the accuracy of the comparator, since the analog voltage inputs are measured sequentially. If the next voltage measurement is from a different input voltage than expected, the state machine will assume an incomplete pair measurement and invalidate the results.

State Machine States

The number and definition of the COMP_SM states and their transitions is indifferent to the number, location, and sequence of the voltage measurement channels. Therefore no modifications are necessary unless the user needs to fundamentally change the functionality of the COMP_SM.

Related Documents

Datasheets

Fusion Family of Mixed-Signal Flash FPGAs

http://www.actel.com/documents/Fusion_DS.pdf

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (51900160-1/1.07*)	Page
51900160-0/1.07	The "Voltage Comparator Design Functionality" section was updated with information P and N polarity.	2
	Figure 4 was updated to clarify the design.	4

Note: **The part number is located on the last page of the document.*

Appendix

This appendix describes a simple circuit that can convert the DATAVALID output of the AB to a signal, only active for one clock cycle, to be transmitted to the COMP_SM state machine. This circuitry is not needed in the voltage comparator design if the DATAVALID input of COMP_SM is driven by the ASSC_DONE output of the AB.

Circuit Implementation

Figure 5 shows the circuit implementation of the DATAVALID conversion function. Note that the output of the second register is not registered again with SYSCLK (to prevent metastability at the output of the circuit). This is mainly because the activation/deactivation of the DATAVALID output of the AB is synchronized with SYSCLK itself.

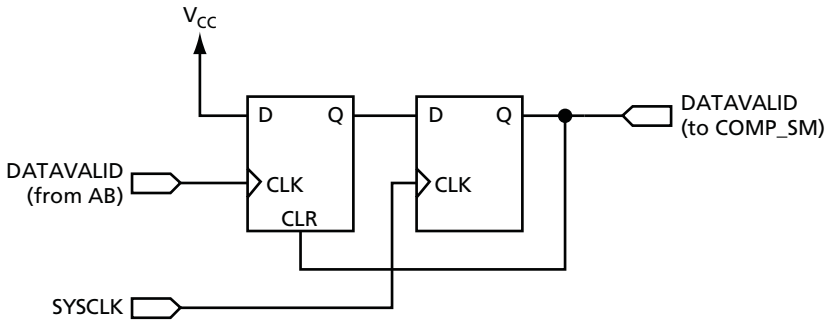

Figure 5 • **Simple Circuitry Connecting DATAVALID Output of AB to DATAVALID Input of COMP_SM**

HDL Implementation

```
library ieee;
use ieee.std_logic_1164.all;

entity Conversion is port
 (SYSCLK: in std_logic;          -- system clock input
  RESETn: in std_logic;          -- active low asynchronous reset
  DATAVALID: in std_logic;       -- driven by DATAVALID output of AB
  DATAVALID_OUT: out std_logic   -- drives the DATAVALID input of COMP_SM
 );
end Conversion;
architecture arch of Conversion is
signal datavalid_int, clr_int: std_logic;
begin
process (DATAVALID, clr_int) begin
  if (clr_int = '1') then
    datavalid_int <= '0';
  elsif (DATAVALID 'event and DATAVALID = '1') then
    datavalid_int <= '1';
  end if;
```

```
end process;

-- This process is to implement the second register.
-- Note that the global system reset is used.
process (SYSCLK, RESETn) begin
  if (RESETn = '0') then
    datavalid_out <= '0';
  elsif (SYSCLK 'event and SYSCLK = '1') then
    DATAVALID_OUT <= datavalid_int;
  end if;
end process
end arch;
```

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