Temperature Monitoring Techniques for Fusion

Introduction

Flash-based Fusion devices integrate analog and digital circuitry into a single chip. With a 12-bit SAR ADC and embedded Flash memory, Actel Fusion is very well equipped to perform voltage, current, and temperature monitoring functions.

This application note describes various methods that may be employed to measure temperature values using the Actel Fusion FPGA:

1. Direct measurement using an external silicon junction
2. Direct measurement using a resistive temperature detector (RTD)
3. Indirect measurement using an RTD and a Wheatstone Bridge

Temperature Measurement with Fusion Using a PN Junction

The effect of temperature on a PN junction is a well known physical phenomenon. The Fusion temperature monitor pad (AT) leverages this by passing two known current levels through an external diode connected bipolar transistor. The temperature monitor block measures the difference in voltage across the transistor as the current is stepped from 10 µA to 100 µA.

EQ 1 is used for finding the voltage drop generated by the PN junction.

$$V_{BE} = (KT_k/q) \times (\ln (I1/I2)$$

EQ 1

Given:

$I1/I2 = 10$

$K/q = 8.7248 \times 10^{-5}$

T_k = Temperature in Kelvin = (273.15 + T °C)

To calculate the actual voltage presented to the input of the ADC, this voltage must be multiplied by 12.5 because of the gain stage shown in Figure 1.

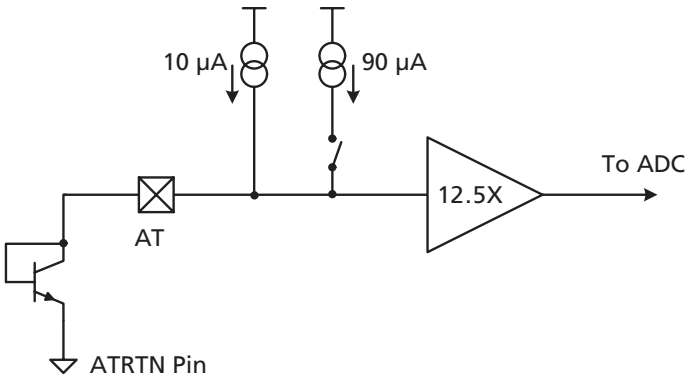

Figure 1 • **Temperature Monitor Connection to External PN Junction**

$$V_{adc} = [(KT_k/q) \times (\ln(I1/I2))] \times 12.5$$

EQ 2

Example: It is desired to construct a temperature monitor to measure the internal temperature of a computer enclosure. The desired temperature measurement range is from 10ºC to 120ºC. What are the corresponding min/max values for V_{adc} and what is the resulting resolution in degrees Celsius of the measurement?

Using EQ 2 and using 10 °C or 283 °Kelvin for T_k,

$$V_{adc} = [(8.7248 \times 10^{-5} \times 283°K) \times (\ln(10))] \times 12.5$$

$$V_{adc} = 0.7107 \text{ Volts.}$$

Again using EQ 2, and using 120 °C or 393 °Kelvin for T_k,

$$V_{adc} = [(8.7248 \times 10^{-5} \times 393°K) \times (\ln(10))] \times 12.5$$

$$V_{adc} = 0.9869 \text{ Volts.}$$

The PN junction is good for about ±2°C resolution but is limited to applications below 150ºC. For higher temperature applications, the designer needs other components, such as a resistive temperature detector (RTD), to allow temperature measurement.

Temperature Measurement with Fusion Using a Resistive Temperature Detector (RTD)

A resistive temperature detector, as the name implies, is a sensor used to measure temperature by correlating the resistance of the RTD element with temperature. The RTD element is made from a pure material whose resistance at various temperatures has been documented. The material has a predictable change in resistance as the temperature changes. RTDs will generally be capable of withstanding and measuring temperatures up to 800ºC. All of these factors make the RTD a more accurate and repeatable temperature sensor in comparison to a PN junction.

RTDs are relatively immune to electrical noise, making them good candidates for applications around motors, generators, and other high voltage noise sources.

Since most digital designers do not currently work with analog sensors of this type, some basic facts regarding RTD are covered.

Using RTD in a Voltage Divider or Half Bridge

Figure 2 on page 3 illustrates one method for connecting an RTD to a Fusion device: it is a simple voltage divider arrangement. For optimal results, this method makes use of the reference voltage output to drive the divider. Note that, an operational amplifier connected as a voltage follower is used to buffer the reference voltage and provide adequate current to drive the resistor network. While this method does not have the inherent noise immunity or the resolution that a bridge circuit can offer, it is easy to implement and it is a reliable method for getting reasonable temperature resolution without the complexity of using a full bridge. This method can use any voltage input of an Analog Quad for the temperature measurement. The Fusion external voltage reference or an external reference can be used to power the divider circuit.

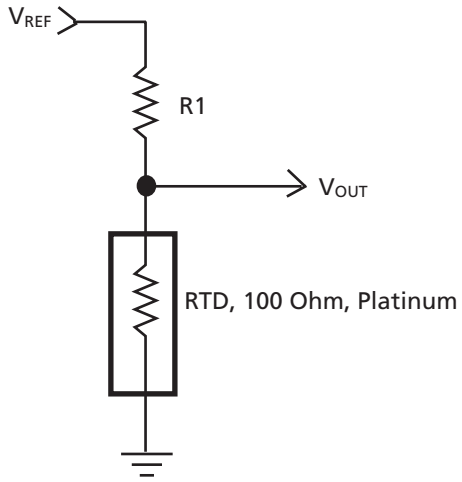

Figure 2 • **Voltage Divider Circuit (Half Bridge)**

Example: assuming that a measurement range of 0ºC to 300ºC is desired, a 100 Ohm Platinum RTD is chosen as a starting point. Table 1 shows a range of resistance values and the corresponding temperature values.

Table 1 • **RTD Resistance Versus Temperature**

Temperature ºC	Resistance in Ohms
0	100
50	119.4
100	138.5
150	57.32
200	175.84
250	194.08
300	212.3

The designer's task is to design a divider circuit capable of varying (212.3 – 100), or 112.3 Ohms, with a voltage swing of 3.3 V.

$$V_{out} = (R_{RTD} \div (R_1 + R_{RTD}))V_{ref}$$

EQ 3

The sum of R_1 plus the resistance of the RTD control is the amount of current required by the circuit. Since the designer has no control over the RTD, the R_1 must be carefully selected. As R_1 gets smaller, the dynamic range of the divider circuit will go down, the linearity will go up, and current requirements will increase. At some point the designer will have a decision to make regarding dynamic range versus excitation current.

The maximum voltage divider current will be required when the RTD is at its lowest temperature. To calculate this current, use EQ 4.

$$I_{ref} = V_{ref} \div (R_1 + R_{RTD})$$

EQ 4

Note: The designer must ensure that the V_{ref} can supply enough current to excite the voltage divider.

Linearity and Accuracy

The voltage divider output accuracy is highly dependent on the tolerances of the RTD, the resistors, and the excitation voltage tolerance. For best accuracy, use a good stable voltage reference and a 0.1% wire-wound resistor for R_1.

The dynamic range is dependent on R_1. This will become apparent later on. Keep in mind that the smaller the value of R_1, the more linear the divider, and the dynamic range of the divider will suffer as the linearity improves.

Important Things to Consider in Design

1. As the value of R_1 increases, the dynamic range decreases for any given RTD value.
2. The larger R_1 is, the smaller the excitation current required will be.
3. The voltage output representing 0°C will not be zero. It can be close to zero, but will require a very large value for R_1.
4. Determine available excitation current, before proceeding with selection of R_1.
5. The smaller R_1, the more linear the result, and the smaller the dynamic range.

Designing the Circuit

This example uses the external voltage reference provided by VCC (3.3 V). Assuming the VCC supply can provide an extra 20 mA for the bridge, the voltage divider is limited to a worst case of 18 mA. Based on these assumptions and an RTD_{Rmin} of 100 ohms, the maximum value for R_1 is calculated using EQ 4 on page 3.

$$R_1 = (V_{ref} \div I_{ref}) - R_{RTD}$$

Given:

I_{ref} =18 mA

V_{ref} = 3.3 V

R_{RTD} = 100 Ω.

R_1 = 183.3 Ω. - 100 Ω. = 83.3 Ω.

Using EQ 3 on page 3 to calculate the minimum and maximum values for V_{out}, based on the resistance values for the RTD at 0 and 300°C.

Given:

R_1 = 81 Ω

R_{RTD}= 100 @ 0 °C

R_{RTD} = 212 @ 300 °C

@ 0 °C

$$V_{out} = (R_{RTD} \div (R_1 + R_{RTD}))V_{ref}$$

V_{out} = (100 ÷ (81 + 100))3.3 V = 1.823V

@ 300 °C

$$V_{out} = (R_{RTD} \div (R_1 + R_{RTD}))V_{ref}$$

V_{out} = (212 ÷ (81 + 100))3.3 V = 2.3877 V

Examining the bridge output sensitivity with respect to resistance:

$\Delta\Omega / \Delta Temp = (212\ \Omega - 100\ \Omega)/300\ °C$

This yields:

$\Delta\Omega / \Delta Temp = 0.3373\ \Omega /\ °C$

Now calculate the change in voltage with respect to temperature, or the minimum resolution of the circuit. The resolution is minimum at the high end of the RTD's resistance range. In this case, the minimum

resolution occurs when the resistance of the RTD changes from 212 Ω to 212.3373 Ω. This represents a 1°C change in temperature.

The maximum resolution occurs when the RTD is at its lowest designed resistance value.

dV/dT = V_{out} @ 100.3373 Ω – V_{out} @ 100 Ω

= (100.3373 Ω ÷ (81 Ω + 100.3373 Ω))3.3 V – (100 Ω ÷(81 Ω+ 100 Ω))3.3 V

= 0.002747 Volts

The next calculation considers resolution at the RTD's highest temperature in its designed temperature range with the RTD resistance at 212 Ω:

dV/dT = V_{out} @ 212 Ω – V_{out} @ 211.6627 Ω

= (212 Ω ÷ (81 Ω + 212Ω))3.3 V – (211.6627 Ω ÷ (81 Ω+ 211.6627 Ω))3.3V

= 0.00105 Volt

This dV/dT value is use to calculate the effective resolution in degrees centigrade.

Temp Resolution @12 bits = ADC Quanta (Volts) ÷ dV/dT (Volts/ °C)

Given:

ADC Quanta (Volts)@ 12 bits = 0.004834 V

Temp Resolution @12 bits = 0.004834 V ÷ 0.00105 Volts / °C

= 4.60 °C

While less accurate than the PN junction, the RTD configured in a voltage divider provides a vastly wider temperature range with a relatively simple implementation. To improve the accuracy of the RTD, the designer needs to look at a full bridge implementation.

Using an RTD in a Wheatstone Bridge

This implementation utilizes the Fusion current monitor input as it is a differential input amplifier. There are several things must be kept in mind when using the Fusion current monitor in this manner.

1. The gain of the current amplifier is fixed at 10 and is not adjustable; therefore, the maximum input to this differential Amp is 0.1x of Vref or, in the case of the example presented in this application note, 0.33 V. Any larger voltage input than this will cause the amplifier to saturate.
2. The input to the differential Amp is unipolar. It can range from 0–0.33V and is differential in nature. Being unipolar, it cannot accept an input below ground.
3. It is not recommended to implement threshold flags for current monitor with this configuration because the sense resistor value is not a constant.
4. Since the flags are not going to be used, the external current sense resistor value required by Analog System Builder in SmartGen can be set to any value (R).

The typical interface circuit for an RTD is a Wheatstone Bridge. The output of the bridge is differential. It will yield 0 volts when the bridge is in balance and will yield a voltage any time there is a difference between the reference and measurement legs of the bridge. As shown in Figure 3 on page 6, the reference leg of our bridge is the "ground leg," while the measurement leg (RTD) is the positive leg. There are other bridge topologies such as Delta or Wye Bridge circuits, but these are not covered here.

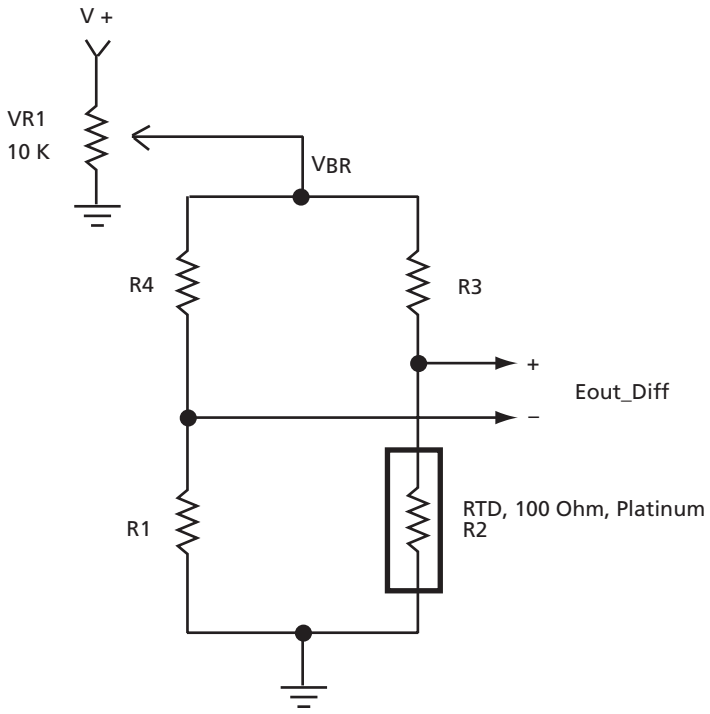

Figure 3 • **Basic Bridge Circuit**

As with the previous example, a measurement of 0°C to 300°C is desired and a 100 Ohm Platinum RTD is chosen as a starting point. The task is to design a bridge circuit capable of varying (212.3 – 100) or 112.03 Ohms with a differential voltage swing of less than or equal to 0.33 V.

EQ 5 is the basic equation for the Bridge output.

$$V_{out\_diff} = R2 \div (R3 + R2)\, V_{BR} - R1 \div (R1 + R4)\, V_{BR}$$

EQ 5

EQ 5 will be used to compute the unknown circuit values.

Bridge Circuit Basics

A few design related details regarding Wheatstone bridge circuits in general are covered below.

Balancing the Bridge

In order for the bridge to balance, the following must be considered.

Setting the above equation to 0 and solving,

$$0 = R2/(R3 + R2)\, V_{BR} - R1/(R1 + R4)\, VBR$$

$$R2 \times R4 = R1 \times R3$$

When the above equation is satisfied, the bridge will balance.

Sensitivity of the Bridge Circuit

To determine the conditions for which this output voltage (V_{out_diff}) changes the most for a given change in a resistance, start by calculating the rate of change of the output voltage as a function of R2 and R3. The derivative of output voltage ($dV_{out}/R2$) with respect to the RTD resistance is as follows:

$$dV_{out}/R_2 = V_2 R_3/[(R_3 + R_2)^2]$$

To get the maximum slope, set $R_2 = 0$. However, the sensor resistance cannot be controlled. R_3 can be chosen to get the maximum slope. To determine the maximum slope, differentiate the expression given above and set the result to zero. This will yield the following:

$$d(dV_{out}/R_s)/dR_c = V_s(R_c - R_s)/[(R_c + R_s)^3],$$

which shows that the maximum slope occurs when $R_3 = R_2$. This may or may not be practical in the specific application.

Linearity of the Bridge Circuit

The designer may want the output voltage of the bridge to change linearly with resistance change in the RTD. It has been found that the output voltage will change linearly with the sensor resistance if

$$R3 >> R2.$$

If the above condition is met, the output from the right leg of the bridge will be almost zero, and the designer will have lost some sensitivity for linearity. This is a trade-off that must be considered.

Bridge Power Requirements

To determine the maximum power requirements for the bridge circuit, the designer must determine the worst case equivalent series resistance of the bridge. In the case of the bridge circuit using an RTD, this will always occur at the lowest resistance of the bridge's sensor (RTD) range.

$$R_{eq} = (R_1 + R_4)(R_2 + R_3) \div (R1 + R_4) + (R_2 + R_3)$$

EQ 6

Once this resistance has been found, it is a simple matter to calculate the current for the bridge.

$$IBR = VBR \div R_{eq}$$

EQ 7

The Bridge Design

Given:

1. The RTD device is rated at 100 at 0°C and 212 at the design target max of 300°C.
2. The bridge must balance at 0°C. This means at 0°C, R4 = R3 and R1 = R2.
3. For maximum sensitivity, the designer must try to keep R3 = R2.
4. To achieve the best Linearity, R3 must be much greater than R2.

Using EQ 5 on page 6, the designer can begin to solve for the values for R_3 and R_4.

$$V_{out\_diff} = R2 \div (R3 + R2)\, VBR - R1 \div (R1 + R4)\, VBR$$

It should be noted that the bridge in this example will not have the best linearity because the V_{out_diff} is limited to 0.33 V and a 100 ohm RTD is used. R_1 will need to be 100 Ohms, and R_3 and R_4 will be less than R_1 and R_2. This will neither be optimal for sensitivity or linearity.

An Excel spreadsheet was used to calculate the appropriate values and analyze the resulting sensitivity/linearity from EQ 5 on page 6. Various values were tried for R_3 and R_4 until the appropriate V_{out_diff} was achieved (Table 2).

Table 2 • **Bridge Calculations**

Name	Value	Units	
RTD Value at 0°C	100	Ohms	
RTD_value at Target	212	Ohms	
R1	100	Ohms	Chosen equal to RTD value at 0°C
R3	27	Ohms	
R4	27	Ohms	
Vbr	3.3	Volts	
Calculated V_{diff}	0.328771	Volts	

Substitute in the upper value of the R_2 (RTD) to 212 Ω and R_1 = 100 Ω, V_{BR}= 3.3 volts to solve the equation by inspection to yield V_{out_diff} = 0.33 volts, or as close as it can get with standard 1% resistor values.

Using R3 = R4 = 27 Ω,

V_{out_diff} = 100 Ω ÷ (27 Ω+ 100 Ω)3.3 V – 212 Ω ÷ (212 Ω+ 27 Ω) 3.3 V

V_{out_diff} = 0.328 V

At 0°C, the RTD resistance is equal to 100 Ω. Using EQ 4 on page 3 yields the following:

$R_2 \times R_4 = R_3 \times R_1$

Or

100 × 27 = 100 × 27;

thus the bridge balances and the V_{out_diff} is equal to 0 V.

Bridge Linearity

Table 3 and Table 4 show the change in the bridge output as compared to the RTD resistance. The bridge output does not increase or decrease linearly with linear changes in RTD resistance. By examining the Delta Ohm/Volt column, find that the bridge output changes by approximately 5.4 mV per change in 1 ohm at the low end of the RTD resistance range (Table 3). At the high end of the range, the output changes by 1.5 mV per 1 Ohm change (Table 4 on page 9). This is not very linear due to the limitation that the designer cannot set R3 greater than R2.

Table 3 • **Bridge Output Versus RTD Resistance (100–121 Ohms)**

RTD Resistance in Ohms	Bridge Output	Delta Ohm/Volt
100	0	0.005481*
101	-0.005481053	0.005396
102	-0.010877129	0.005313
103	-0.016190188	0.005232
104	-0.021422131	0.005153
105	-0.026574803	0.005075
106	-0.031649991	0.004999
107	-0.03664943	0.004925
108	-0.041574803	0.004853
109	-0.046427744	0.004782
110	-0.05120984	0.004713
111	-0.055922629	0.004645
112	-0.060567609	0.004579
113	-0.065146232	0.004514
114	-0.06965991	0.00445
115	-0.074110014	0.004388
116	-0.07849788	0.004327
117	-0.082824803	0.004267
118	-0.087092045	0.004209
119	-0.091300831	0.004152
120	-0.095452354	0.004095
121	-0.099547776	0.00404

Note: *The bridge is balanced.

Table 4 • **Bridge Output Versus RTD Resistance (205–211 Ohms)**

Resistance in Ohms	Bridge Output	Delta Ohm/Volt
205	-0.317523079	0.001648
206	-0.31917137	0.001634
207	-0.320805572	0.00162
208	-0.322425867	0.001607
209	-0.32403243	0.001593
210	-0.325625436	0.00158
211	-0.327205055	0.001566

Dealing with Bridge Nonlinearity

The easiest way to deal with this nonlinearity is to create a lookup table to correct for the resulting bridge nonlinearity. This could be accomplished by using the Fusion Flash memory to hold a lookup table of corrections. This would be obtained by sweeping the temperature in known increments and recording the resulting value so that a calibration table could be made. Other methods could be used, but these are not discussed in this application note.

Evaluating the Sensitivity of the Bridge Circuit

While the RTD bridge is capable of measuring sub 1°C changes in temperature, the minimum sensitivity must be determined for later comparison with the ADC converter. As can be seen from Table 4, the minimum resolution of the bridge occurs when the RTD resistance is highest and the maximum resolution occurs when the RTD is at its lowest value. The designer needs to use the maximum sensitivity to determine the value to compare against the minimum ADC Quanta to make sure the ADC will work for the application.

Maximum Bridge Sensitivity = 1.566 mV/Ω,

Expressed in Decibels:

20 Log(0.33V/1.566 mV) = 48.8 dB

Minimum Bridge Sensitivity = 5.488 mV/Ω,

Expressed in Decibels:

20 Log(0.33V/5.488 mV) = 35.6 dB

Next, examine the bridge output sensitivity with respect to resistance. Consider the following:

ΔΩ,/ ΔTemp = (212 Ω – 100 Ω)/300°C

This yields

ΔΩ,/ ΔTemp = 0.3373 Ω/ C

Using 0.3373 Ω/ °C to determine the change in the bridge output voltage per one °C rise in temperature, the designer will determine the difference in bridge output voltage at the point where it will have its smallest change. That is at 211°C.

$V_{out\_diff} = R_2 / (R_3 + R_2)$ VBR – R1/(R1+ R4) VBR

@ 212 Ω V_{out_diff} = –0.32877 V

@ 211.6627 Ω V_{out_diff} = -0.32824 V

So,

dV/dT = V_{out_diff} @ 212 Ω – V_{out_diff} @ 211.6627 Ω

dV/dT = 0.32877 Volts / °C – 0.32824Volts/ °C

dV/dT = 0.00053 Volts / °C

Calculating the Bridge Supply Current

The equation for calculating the equivalent bridge resistance was given in EQ 7 on page 7. Using this, the supply current can be calculated for this application.

$$R_{eq} = (R_1 + R_4)\ (R_2 + R_3) \div (R_1 + R_4) + (R_2 + R_3)$$

Substituting in the real circuit values yields

$$R_{eq} = (100\ \Omega + 27\ \Omega)\ (100\ \Omega + 27\ \Omega) \div (100\ \Omega + 27\ \Omega) + (100\ \Omega + 27\ \Omega)$$

$$R_{eq} = 63.5\ \Omega.$$

Bridge current is found as follows:

$$I_{BR} = V_{BR} \div Req$$

$$I_{BR} = 3.3V \div 63.5\ \Omega$$

$$I_{BR} = 51.9\ mA$$

All of the above calculations do not take into account the tolerances of the resistors used in the design. These calculations are left up to the designer if absolute accuracy is needed. For most practical designs this is probably not necessary.

Examining the Bridge Sensitivity Versus Converter Resolution

The bridge circuit, at its worst, has a sensitivity of 48.8 dB. This means that the Fusion ADC with its 56 dB resolution in 12-bit mode or 50.69 dB in 10-bit mode is capable of performing the application. The choice between 10-bit or 12-bit mode depends on the exact temperature resolution the designer wishes to achieve.

Temperature Resolution of the Bridge-ADC Subsystem

Earlier in this document it was determined that the bridge circuit would provide the following ΔV with respect to a 1°C change in temperature.

This is the worst case and occurs at the largest resistance value of the RTD of the desired temperature measurement. In this case it is between 211 and 212 Ohms.

$$dV/dT = 0.00053\ Volts/\ °C$$

This value must be multiplied by a factor of 10 to account for the gain present in the Analog Quad current amplifier which is being used as a differential amplifier. When this gain factor is applied to the bridge $\Delta V/\ \Delta Temp$, the $\Delta V/\ \Delta Temp$ applied to the ADC becomes the following:

$$10 \times (0.00053V) \text{ or } 0.0053\ Volts/\ °C$$

If the designer divides the smallest resolvable voltage of the ADC converter by the bridge voltage output per °C (as presented at the ADC input), it will yield the temperature resolution of the system.

Given:

ADC Quanta (Volts)@ 12 bits = 0.004834 V,

ADC Quanta (Volts) @ 10 bits = 0.00963 V,

Temp Resolution @ 12 bits = ADC Quanta (Volts) / Bridge Resolution (Volts/ °C)

$$= 0.004834\ V \div 0.0053\ Volts/\ °C$$

$$= 0.9120\ °C$$

Temp Resolution @ 10 bits = ADC Quanta (Volts) / Bridge Resolution (Volts/ °C)

$$= 0.00963\ V \div 0.0053\ Volts/\ °C$$

$$= 1.816\ °C$$

To achieve better than 1°C resolution, the designer would choose the 12-bit mode.

Calculating the Bridge Supply Current

The equation for calculating the equivalent bridge resistance was given in EQ 7 on page 7. Using this, the supply current can be calculated for this application.

$$R_{eq} = (R_1 + R_4)\,(R_2 + R_3) \div (R_1 + R_4) + (R_2 + R_3)$$

Substituting in the real circuit values yields the following:

$$R_{eq} = (100\ \Omega + 27\ \Omega)\,(100\ \Omega + 27\ \Omega) \div (100\ \Omega + 27\ \Omega) + (100\ \Omega + 27\ \Omega)$$

$$R_{eq} = 63.5\ \Omega$$

Bridge current is found as follows:

$$I_{BR} = V_{BR} \div Req$$

$$I_{BR} = 3.3\ V \div 63.5\ \Omega$$

$$I_{BR} = 51.9\ mA$$

Using the Active Half Bridge Circuit

Figure 4 details a possible circuit to requiring one less op amp but still giving close to 0.5°C resolution. It makes use of the Fusion voltage reference, which must be buffered because of source current limitation. This reference can only source 10–20 µA.

The first amplifier stage provides buffering for the reference voltage and is configured to run at unity gain. The voltage swing off the RTD half bridge varies from 232–447 mV, corresponding to 0–300°C. The output of the divider goes into a gain stage of 5. This amplifier has its bandwidth limited via C1. The value of C1 is chosen to yield approximately 6 dB of gain roll-off at 100 Hz and 25 dB at 1000 Hz.This makes the circuit immune to high frequency noise.

The next amplifier stage is set up as a summing amp that sums the RTD signal with an offset voltage to restore the RTD signal to a zero referenced condition at 0°C. It can also compensate for offset error induced elsewhere in the system (Fusion device, etc.). This Amp has gain stage of 3 that expands the dynamic range so the full 3.3 Volt swing can be utilized.

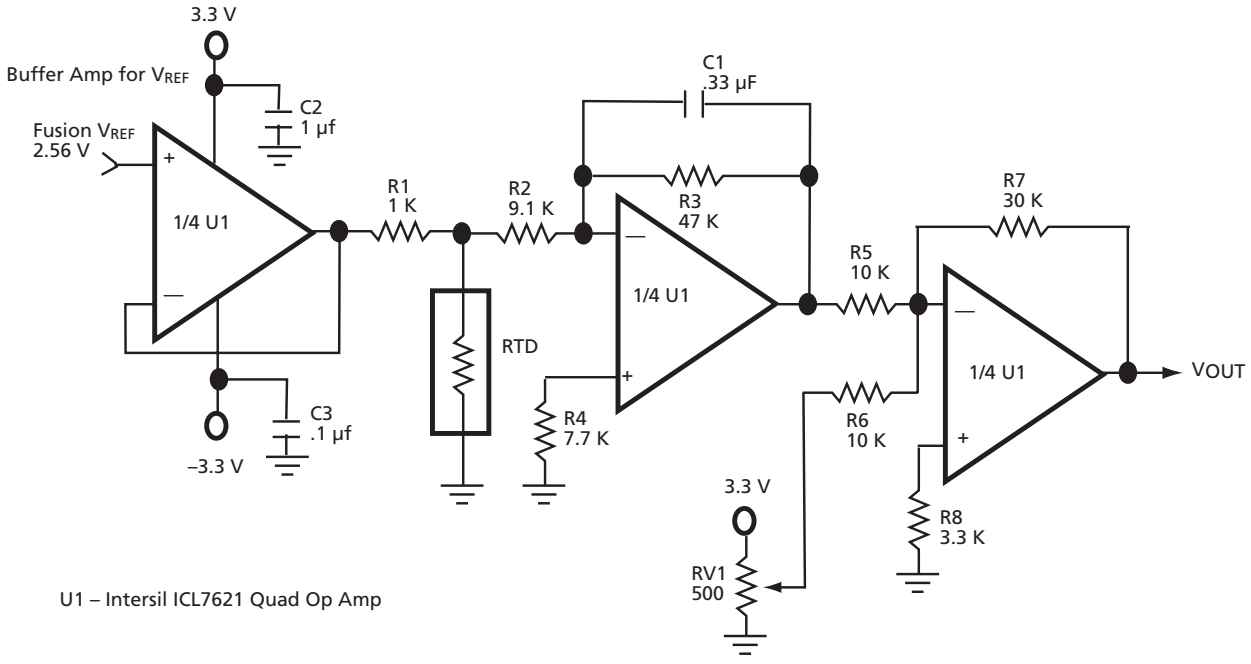

Figure 4 • **Divider with V_{ref} Buffering and Offset Adjustment**

Analysis of Circuit

The output of the half bridge is 0.232 V @ 0 °C and 0.447 V @ 300 °C from EQ 3 on page 3.

$V_{out} = (R_{RTD}/ (R_1 + R_{RTD}))V_{ref}$

The first amplifier stage gain can be calculated from

$Av = R_f + (1/ 2\pi \times F \times C)/ R_{in}$

The reactive component of this equation is what yields frequency roll-off of the amplifier.

The first gain stage amplifies this to

0.232 Volts × 5 = 1.16 V @ 0 °C

0.447 Volts × 5 = 2.235 V @ 300 °C

The second gain stage Av equals

$Av = – R7 (V_{in1} / ((R5 + R_s) + V_{offset}))/ ((R6 + R_{soff}) / (V_{in1} + V_{offset})) \cong 3$

R_s = Output source impedance of amplifier

R_{soff} = Source impedance of offset voltage divider

Which yields the following:

(–1.160 Volts + 1.16 V offset) × –3 = 0 V @ 0 °C

(–2.235 Volts + 1.16 V offset) × –3 = 3.237 V @ 300 °C

Putting it all together leads to EQ 8, which describes the voltage output of Figure 4 on page 11 with respect to RTD resistance.

$$V_{out} = \frac{(R_{RTD}/(R_1 + R_{RTD})) \times V_{ref} \times ((-R3)/(R2)) \times (-R7(V_{in1}/((R5 + R_s) + V_{offset})))}{(R6 + R_{soff})/(V_{in1} + V_{offset})}$$

EQ 8

Examining Sensitivity in Volts /Celsius

Using EQ 8 to find out V_{out} @ 211.6627 Ω,

V_{out} = 3.2280 V

Sensitivity is then dV with respect to a 1°C change in temperature.

dV/dT = V_{out} @ 212 Ω – V_{out} @ 211.6627 Ω

= 3.2368 Volts / °C – 3.2280 Volts / °C

= 0.00882 Volts / °C

Resolution in Celsius

= ADC Quanta (volts) ÷ dV/dT

= 0.004834 V ÷ 0.00882 Volts/ °C

= 0.548 °C

Using the RTD Bridge with an External Instrumentation Amplifier

Figure 5 on page 14 shows a circuit to improve the performance of the RTD Bridge circuit. It makes use of the Fusion voltage reference which must be buffered because of source current limitations. This reference can only source 10–20 µA.

This is one of the best RTD interfaces that can be used for this type of application. It allows for the best linearity and good common mode noise rejection. It also has zero adjustment for the bridge. The output V_{out} can be connected to the Voltage input channel and will vary from 0 Volts at 0°C to 3.25 Volts at 300°C.

Basic Circuit Topography

Vref Buffer

The circuit uses a Voltage follower setup to provide unity gain. This provides the buffered 2.56 V reference to the bridge circuit. R5 and R6 could be manipulated to increase the gain to provide a larger reference voltage if desired. This is shown in EQ 9.

$$Av = 1 + R6/R5$$

EQ 9

Bridge Circuit

The bridge resistors (R4 + ½ P1) and (R3 + ½ P1) are set to 470. This makes R4 >> R2 and R3 >> RTD, thus improving linearity. P1 is used to balance the bridge manually at 0°C to 0 Volts. From EQ 1 on page 1 we find that the output of the bridge is 0 volts at 0°C and 0.3466 Volts at 300°C. Since we want the output of the entire circuit to be 0–3.3 V, a gain stage follows the bridge. The required gain is calculated in EQ 10.

$$Av = V_{out} \div V_{in} = 3.3\ V \div 0.3466\ V = 9.52$$

EQ 10

Instrumentation Amplifier

The amplifier is type chosen is an instrumentation Amp. It is differential and has good common mode noise rejection and is tailor-made for these types of applications. The one in this design is built from a Intersil ICL7621. This is a Quad low power, low noise amplifier. A full datasheet can be found at the following link: http://www.intersil.com/data/fn/fn3403.pdf.

To calculate the gain of the instrumentation amplifier, use EQ 11.

$$Av = 1+ 2R/Rg$$

EQ 11

Solving in terms of Rg,

Given:

$R = 1\ K\Omega$

$Av = 9.52$

$Rg = 2R \div Av - 1 = 2(1\ K\Omega) \div (9.52 - 1) = 234.7\ \Omega$

EQ 12 is used to calculate the voltage output of Figure 5 on page 14 with respect to RTD resistance.

$$V_{out} = (1+ (2R \div Rg)) \times [(R2 \div (R3+R2)) - (R1 \div (R1+R4))]V_{BR}$$

EQ 12

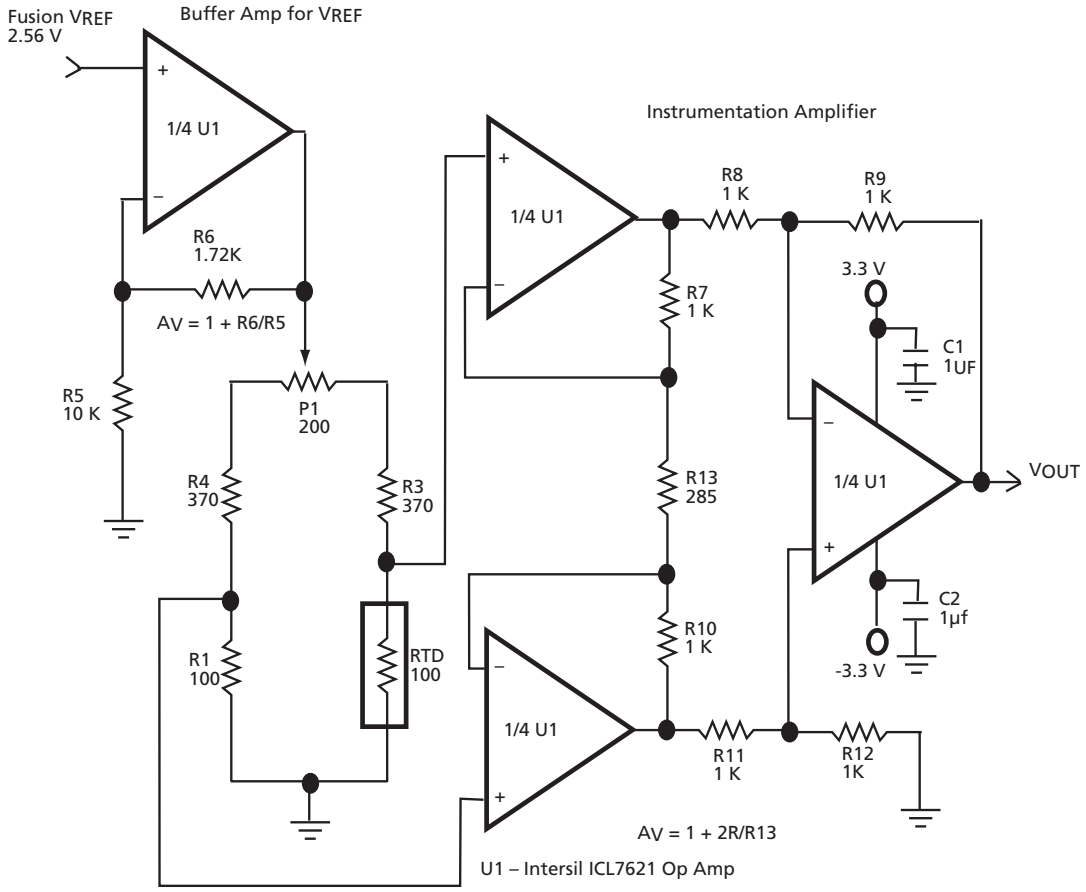

Figure 5 • **Full Bridge with Instrumentation Amplifier**

Examining Sensitivity in Volts / Celsius

Remembering the resistance increases 0.3373 Ω per degree Celsius, the Voltage out of Figure 5 must be calculated for an RTD resistance of 212 Ω and 211.6627 Ω. This is 300 °C and 299 °C respectively.

dV/dT = $V_{out\_}$@212 Ω – $V_{out_@}$211.6627Ω

= 3.30015 Volts/ °C – 3.29184 Volts/ °C

= .00831 Volts/ °C

Resolution in Celsius

= ADC Quanta (Volts) ÷ dV/dT

= 0.004834 V ÷ 0.00831 Volts/°C

= 0.5817 °C

Conclusions

The Actel Fusion device has great flexibility in handling all the temperature measurement needs. The built-in temperature monitor allows for ± 2°C resolution using an inexpensive PN junction such as a 2N2222 transistor or 1N914 signal diode. For more measurement range and resolution, use an RTD device with Fusion voltage or current inputs, and for the most exacting applications, use the RTD bridge with an instrumentation amplifier for ± 0.5°C resolution. If for some reason the designer uses all the current inputs for something other than the RTD circuits, the voltage input can be employed for RTD use with the half bridge configuration.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (51900127-1/4.07)	Page
51900127-0/1.06	Figure 1 on page 1 was updated.	1

www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley, Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

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