

Flash*Freeze Control Using JTAG

Introduction

The Actel IGLOO® and ProASIC®3L families of FPGA devices are based on Actel nonvolatile flash technology and single-chip ProASIC3 FPGA architecture. These devices are part of a 1.2 V to 1.5 V operating voltage, offering the industry's lowest power consumption, smallest footprint, competitive prices, and many advanced features. The Flash*Freeze technology used in IGLOO and ProASIC3L devices enables entering and exiting Low Power mode that consumes as little as 2 μ W of power while retaining all SRAM and register data. Flash*Freeze technology simplifies power management through input/output (I/O) and clock management, with rapid recovery to full operational mode. Refer to the *IGLOO FPGA Fabric User's Guide* and the *ProASIC3L FPGA Fabric User's Guide* for additional information on the device features and use of the Flash*Freeze pin.

In applications where the device is in Flash*Freeze mode for most of the operation or in cases such as remote deployment with the Flash*Freeze pin asserted, there is a need to control the Flash*Freeze entry and exit from within the device to save power, simplify software, and avoid continuous toggling of the Flash*Freeze pin.

In addition, IGLOO and ProASIC3L devices cannot be programmed while in Flash*Freeze mode and the logic that enables authentication for encrypted programming is turned off by default to save power. Therefore, a solution is needed to bring the device out of Flash*Freeze mode and to internally turn on the authentication circuit in applications where physical access to the Flash*Freeze pin is not available. This logic, which is programmed into the device along with the user application, acts as a Master for the Flash*Freeze mode. Two distinct use models have been developed to address this type of application. You can choose either one of these solutions, depending on the individual application requirements:

- Flash*Freeze control using JTAG: This solution provides on-demand wake-up of the device for programming and also for authentication.
- Flash*Freeze control using an internal oscillator

This application note describes the Flash*Freeze control with JTAG for all IGLOO and ProASIC3L devices and addresses the following requirements:

- Entry to and exit from Flash*Freeze mode using JTAG instructions without toggling the Flash*Freeze pin
- Programming when the device is in Flash*Freeze mode, while addressing the need of remote programming
- On-demand authentication by turning on the authentication circuit required for encrypted and secure programming

Files for this application note can be downloaded from the Actel website:

www.actel.com/download/rsc/?f=FlashFreeze_Ctrl_using_JTAG_DF.

Note: All files are Verilog 2001 compliant.

The internal oscillator approach is described in *Flash*Freeze Control Using the Internal Oscillator*.

Flash*Freeze Control with JTAG

This use model takes advantage of the active JTAG pins during Flash*Freeze mode. The functionality is accomplished using a macro which consists of the following elements:

- UJTAG
- Custom finite state machine (FSM)
- User low static ICC macro ULSICC_AUTH

UJTAG provides the 8-bit parallel data corresponding to the serial data coming from the test data input (TDI) pin. This data is decoded by the FSM to determine the state into which the design should move. The ULSICC_AUTH macro, which is a variant of the ultra-low static ICC macro, is used to control Flash*Freeze mode and the authentication circuit. [Figure 1](#) shows the block diagram for this macro.

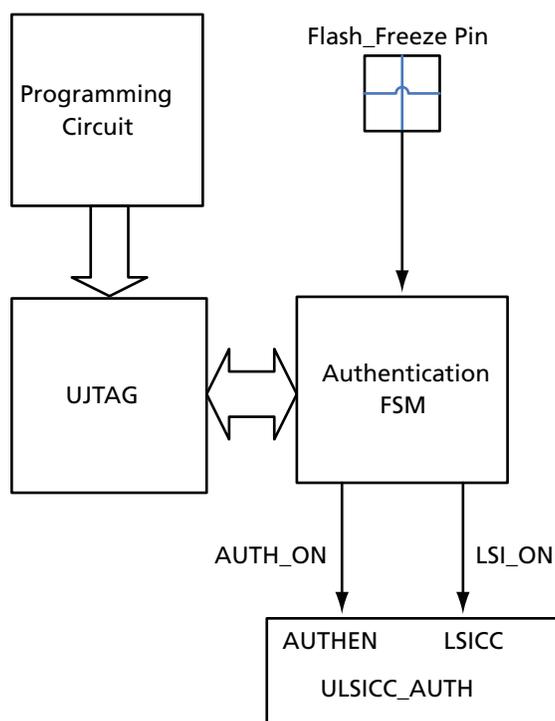


Figure 1 • ULSICC_AUTH Macro Block Diagram

Design States

A design programmed in an IGLOO or ProASIC3L device can be in any one of these states:

- Active: Normal operational mode of the design
- Flash*Freeze: Asserts the LSICC input of ULSICC_AUTH macro to enter a low power state. The device enters Flash*Freeze mode only when the external Flash*Freeze pin is also asserted.
- Authenticate: This is not a design state but rather a device state. The AUTHEN input of ULSICC_AUTH is asserted to turn on the authentication circuit. By default, AUTHEN is turned off, saving approximately 1 mA in device current.

JTAG Instructions

FSM decodes the JTAG instructions as described in Table 1. New user-defined instructions were specifically defined for this macro.

Table 1 • Supported JTAG Instructions

Instruction	Opcode	Description	Comment
U_FF	0x7E	Takes the device into Flash*Freeze mode. The Flash*Freeze pin must be asserted.	New instruction
U_ACTIVE	0x7F	Takes the device into Active mode.	New instruction
U_HW	0x7D	Puts the device under control of the Flash*Freeze pin.	New instruction
AES_INIT	0xDD	Enables the authentication circuit (authenticate state).	Existing instruction
VERIFY_DMK	0x0A	Keeps the authentication circuit on (authenticate state).	Existing instruction
DESCRAMBLE	0xDF	Keeps the authentication circuit on (authenticate state).	Existing instruction
BYPASS	0xFF	Keeps the authentication circuit on (authenticate state).	Existing instruction

FSM Description

FSM has four distinct states (Figure 2 on page 4). Since JTAG pins are active during Flash*Freeze mode, FSM uses TCK for clocking, provided by a FlashPro3/STAPL player or any other programming circuitry.

Note: During Flash*Freeze, external clocks are not seen inside the core.

FSM accomplishes the required functionality by controlling the LSICC and AUTH_EN inputs of the ULSICC_AUTH macro. Depending on the state of the Flash*Freeze pin and incoming JTAG instruction, FSM places the device into one of these states:

- **HWControl:** The U_HW instruction brings the FSM into this state. This is also the state at reset.
- **Active:** The device is active, not in Flash*Freeze mode. The U_ACTIVE instruction brings the FSM into this state. FSM needs to be in an active state before programming or the JTAG boundary scan test can be initiated.
- **Flash*Freeze:** Software control of Flash*Freeze. The U_FF instruction brings the FSM into this state.
- **Authenticate:** The authenticate circuit is ON. The AES_INIT instruction brings FSM into this state and VERIFY_DMK/DESCRAMBLE/BYPASS instructions keep FSM in this state. Authentication circuit is on in this state.

Upon reset, the device defaults with Flash*Freeze control to the external Flash*Freeze pin.

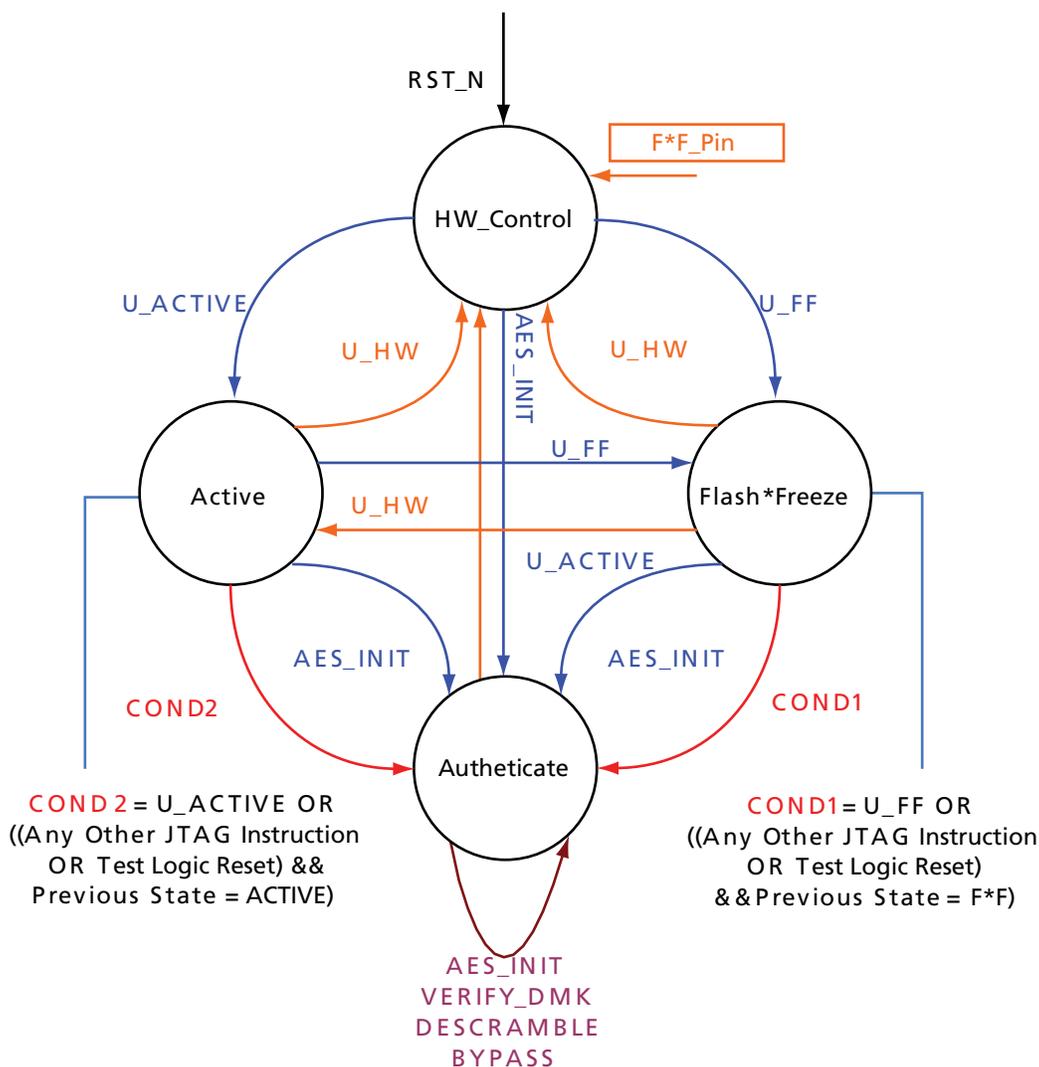


Figure 2 • States of the FSM

Theory of Operation

In a typical IGLOO or ProASIC3L application, the Flash*Freeze pin is asserted (active Low) on the board. The device can be in Flash*Freeze mode with the LSICC pin asserted (active High). The FSM, which is part of the design programmed into the FPGA, listens to and reacts to the JTAG instructions coming in.

Prior to programming the device, the device first needs to be brought out of Flash*Freeze mode and into Active mode by the JTAG instruction U_ACTIVE (0x7F).

Sample STAPL Code

The TAKE_TO_ACTIVE and TAKE_TO_FF STAPL procedures take the Actel device into the active state and Flash*Freeze state respectively. The AES_INIT instruction required for the authenticate state entry is part of the existing STAPL files and there is no need for any additional procedures:

```
PROCEDURE TAKE_TO_ACTIVE USES GV;
PRINT "Get into Active State";
    IRSCAN 8, $7F;
    WAIT IDLE, 3 CYCLES;
    WAIT 1000 USEC;
ENDPROC;
PROCEDURE TAKE_TO_FF USES GV;
PRINT "Get into F*F State";
    IRSCAN 8, $7E;
    WAIT IDLE, 3 CYCLES;
    WAIT 1000 USEC;
ENDPROC;
```

Two action blocks are defined for these procedures:

```
ACTION IN_ACT = TAKE_TO_ACTIVE;
ACTION IN_FF = TAKE_TO_FF;
```

To bring the device to Active mode before programming, the PROGRAM action must be modified to include the TAKE_TO_ACTIVE procedure as the first procedure of the action. After programming, IN_FF takes the device back into Flash*Freeze mode. The new action PROGRAM_IN_FF should be used when the device is in Flash*Freeze mode:

```
ACTION PROGRAM_IN_FF =
    TAKE_TO_ACTIVE,
    W_INITIALIZE,
    DO_ERASE,
    DO_PROGRAM,
    DO_VERIFY_BOL,
    DO_PROGRAM_RLOCK,
    DO_PROGRAM_SECURITY RECOMMENDED,
    DO_EXIT;
```

Since the STAPL file has been edited, the CRC check will fail. To avoid this, the CRC value of the STAPL file must be changed to zero. This is the last line of the STAPL file:

```
CRC 0;
```

Limitation

ARM® Cortex™-M1 designs with debug from a FlashPro3 interface use the UJTAG macro. IGLOO and ProASIC3L devices have only one instance of UJTAG. Since this macro requires another instance of UJTAG, this macro cannot be used with designs that have a Cortex-M1 FlashPro3 interface.

Utilization Details

This design was verified in Actel's AGL600-256 FBGA IGLOO device, but can easily be instantiated in other IGLOO and ProASIC3L devices that contain the minimum required resources. The utilization details for the AGL600-256 FBGA are described in [Table 2](#).

Table 2 •

Resource	Utilization	Total	Percentage
Core	79	13,824	0.57%
I/Os	3	177	1.69%
Global (chip + quadrant)	0	18	0.00%
PLL	0	1	0.00%
RAM/FIFO	0	24	0.00%
Low static ICC	1	1	100.00%
User JTAG	1	1	100.00%

Conclusion

Flash*Freeze control with JTAG and minor STAPL file modifications gives you control of Flash*Freeze mode and the authentication circuit, allowing ISP and secure programming from within Flash*Freeze mode. Software control of Flash*Freeze mode provides flexibility and control that is otherwise not possible.

Related Documents

IGLOO FPGA Fabric User's Guide

www.actel.com/documents/IGLOO_UG.pdf

ProASIC3L FPGA Fabric User's Guide

www.actel.com/documents/PA3L_UG.pdf

*Flash*Freeze Control Using the Internal Oscillator*

www.actel.com/documents/FlashFreeze_Ctrl_using_IOSOC_AN.pdf

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