Ceramic Chip Carrier Land Grid (CC256) Package Handling

Introduction

Die-level solutions allow for the integration of differing technologies or products from multiple companies, all on the same board or multi-chip module. Die that can be tritemp tested or screened, also known as known good die (KGD), provides the highest yields at the module and board-assembly level. This application note provides a background on why an FPGA programmable at the die level is needed, where it can be used, and finally the solution Actel offers for programming at the die level, the 256 pin Ceramic Chip Carrier Land Grid(CC256) package.

CC256 Package Description

The CCLG is a multi-layer ceramic package with attributes including:

1. Dark ceramic, same material as Actel's Ceramic Quad Flatpack (CQFP or CQ) CQ208, 256, 352 packages

2. 256 bond fingers on top for routing signals when it is assembled either in a multi-chip module or a system board

3. 256 land pads on the bottom with a 1.0 mm pitch, which are used for testing and programming the devices

4. Body size is 17 mm square for CC256

5. Ceramic thickness is 1.397 mm

6. Total package thickness is 1.847 mm

7. Wire bond interconnect used to connect silicon to package

8. Die cavity is on the top side of the package and hermetically sealed with AuSn eutectic material the (Lid is connected to GND)

Background

Antifuse technology offers the highest performance and highest reliability. The connection is electrically and thermally initiated. However, once made or fused, it becomes a mechanical connection, and is highly resistant to electrical noise and virtually immune to single-event effects (SEE). SEEs are effects due to ionic particles contained in cosmic galactic rays (GCR) in space. GCRs are comprised of these charged particles or ions that can strike a semiconductor device and alter the state of charge stored devices. It is the superior performance and the ability to withstand SEEs that makes antifuse technology the programmable logic device of choice for the space community.

The programming of antifuse devices present some unique challenges for the designer as semiconductor processes scale in feature size. These are tiny devices comprised of layers of amorphous silicon and dielectric materials sandwiched between two metal electrodes. With the right amount of applied voltage, stressing polarity, and temperature, a solid electro-mechanical connection is created. Many technical papers have been written to describe the modeling and reliability behavior of this technology. See the "Related Documents" section on page 5 for a background on metal-to-metal antifuse technology. Figure 1 on page 2 is a cross section of a metal-to-metal antifuse for a triple-level metal CMOS process. (The triple-layer metal was chosen for its simplicity of illustration).
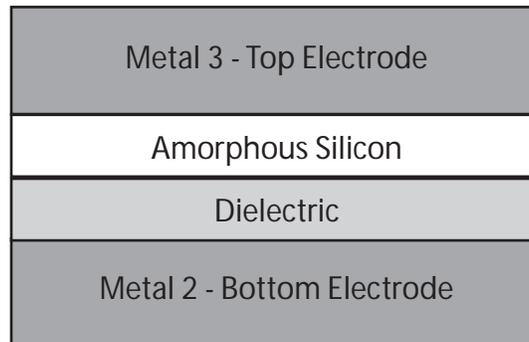
Figure 1 • **Cross-sectional View of a Metal-to-Metal Antifuse**

The metal-to-metal antifuse has the following advantages:

- Low temperature requirements for CMOS processing
- Smaller size (for high density)
- Low leakage
- Low programmed resistance and capacitance (high performance),
- Low programmed capacitance
- High off state (unprogrammed) and on-state (programmed) reliability

In order to achieve a reliable connection, accurate programming currents are required to obtain the correct metal-to-metal antifuse resistance distribution. These currents are controlled during the forming process of the conducting link. Stray or uncontrolled programming currents and voltages can stress these devices whereby the results could lead to unreliable connections or damaged fuses. Electrical overstress is a major cause of fuse damage in the programming, manufacturing and handling of antifuse FPGAs. Unstressed, the accuracy and repeatability of antifuse connections are well documented in the literature listed in the "Related Documents" section on page 5. It is electrical overstress that mostly leads to unreliable connectivity due to damaged fuses.

Actel and its customers have successfully programmed generations of packaged antifuse devices including metal-to-metal. With suppliers of high reliability devices to the military/aerospace community diminishing, system manufacturers have had to develop clever ways of selecting and screening lower reliability product, that alone would not stand up to the rigors of GCRs or ions in space. Mitigation with some type of error correction or detection scheme, triple module redundancy are common techniques employed to protect the system and improve reliability. Antifuse programmable FPGAs can provide a low risk, low cost logic solution that can be used to implement applications; error correction and detection or some other mitigation scheme can minimize errors due to noise, either electrical or GCR initiated, in a system. In some applications where triple modular redundancy is required for mitigation, Actel FPGAs are used to reliably perform the voting and arbitration schemes. In commercial applications, where high performance board space is at a premium, the footprint is important. Many commercial applications require the merger of devices from incompatible process technologies, thus rendering integration at the integrated circuit level not possible. Integration then must be accomplished at the board level, using either multi-chip modules, hybrids, multi-chip packaging or some other exotic advanced packaging solution.

Antifuse technology requires controlled voltages and currents for reliable programming. However, integrating devices at the multi-chip packaging level, especially in high-reliability applications, requires a known good die (KGD). The resulting challenge is how to program the antifuse devices at the die level yet deliver these controlled signals to the FPGA. Sorting or applying any electrical signals to a die is fraught with the peril of long wires, photon-induced currents due to light, stray capacitance and inductance rendering control signal accuracy unattainable.

Packaged devices have the ability to deliver voltages and currents right to the device pins via low impedance socketing. Actel has solved the dilemma of programming at the die size integration level with a new advanced packaging solution called the Ceramic Chip Carrier Land Grid (CCLG) as an alternative solution for KGD. This package was developed with the space community in mind, to deliver die size

packaging with a radiation-tolerant FPGA. Actel is introducing the CC256 package with the RT54SX32S, Actel's designed-for-space, 0.25μm CMOS, radiation-tolerant (radtolerant or RT), 16,000 gate (ASIC equivalent gates).

The CC256 package is a small footprint (17mm), chip-scale package. It has 256 bond fingers on top for routing signals when it is assembled either in a multi-chip module or a system board. At the same time, there are 256 land pads on the bottom, which are used for testing and programming the devices. See Figure 2 and Figure 3 for details.
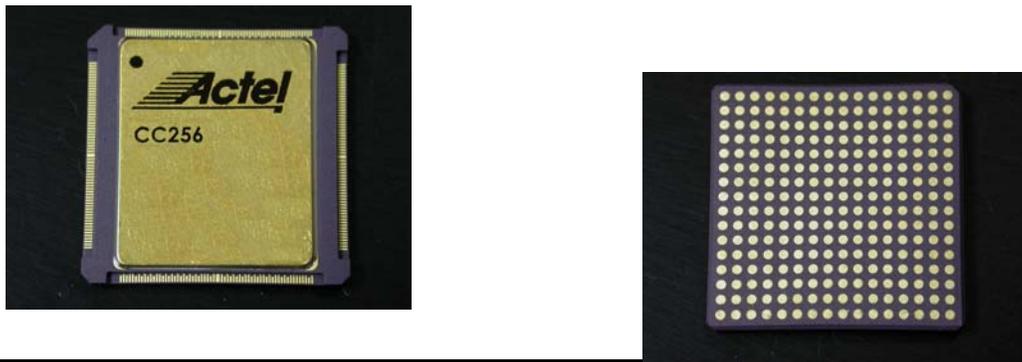
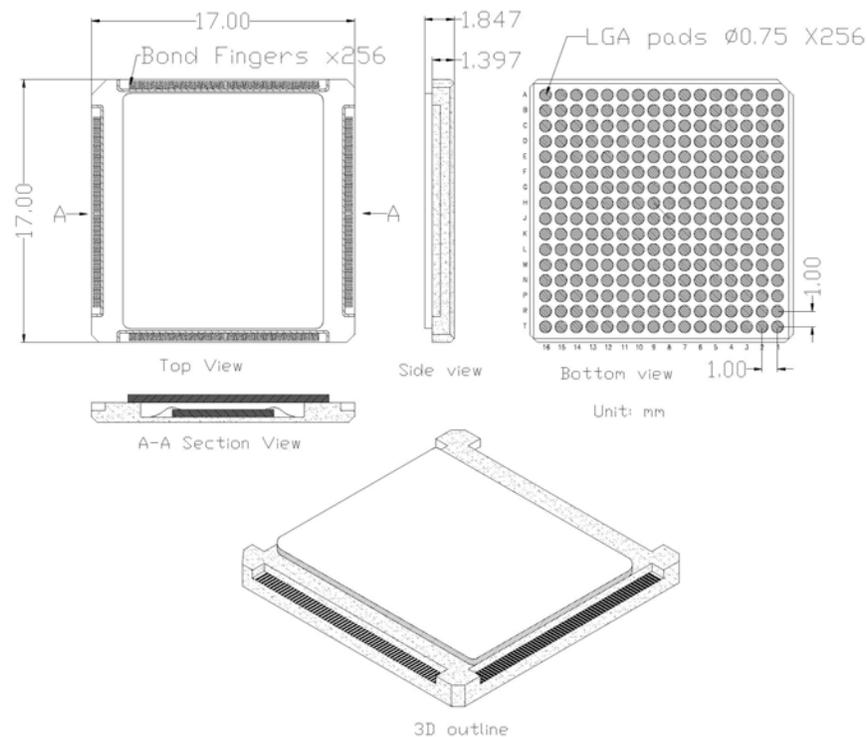

Figure 2 • **CC256 Package Top and Bottom View**

Figure 3 • **CC256 Outline Drawing**

Manufacturing Handling

It is very important for you to handle the CCLG packages in the proper manner. Preventing corrosion and or damage to the exposed external bonding pads will ensure interconnect reliability. Extreme care should be exercised when handling the CCLG devices during programming, test, and assembly of the final module.

1. Very carefully attach a vacuum pick-up tool on the central area of the lid to pick-up and place the CC256 devices from the shipping container box to the socket or from socket to shipping container box (Figure 4).
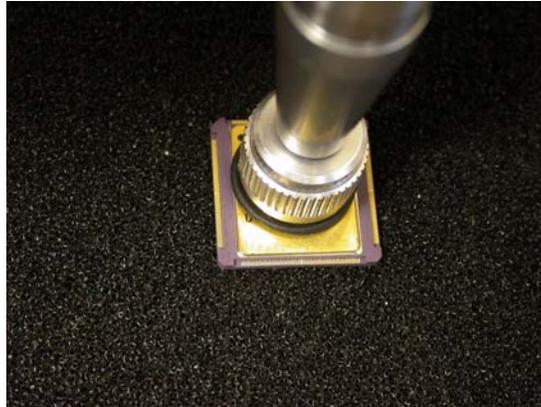

Figure 4 • **Pick and Place the CC256**

2. Never touch the external bonding finger area (four sides). Contamination on the external bonding fingers can lead to wire-bond failure.

Attaching the CC256 to the Multi-Chip Module or System Board

Since the bottom of the package consists of 256 LGA pads that are electrically connected to the silicon die, the material used to attach the CC256 must be thermally conductive yet electrically nonconductive.
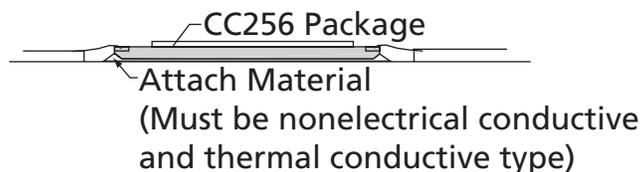

Figure 5 • **CC256 Attach Material Drawing**

Layout Signal Trace on Board for Routing Signal out from the Chip Carrier

The bonding fingers on the top of the CC256 are located on the edges of the four sides. The pitch on the bonding fingers is quite small (approximately 4mils-0.1mm). Some special function signals V_{CC} and GND bonding fingers must be bonded out to the system board. Please review the *RTSX-S Datasheet* and the detailed package drawing before committing to final board layout. Also, it is wise to review the wire bond process and capability with a board assembly vendor to ensure that wire bonding will meet your requirements.

Programming Devices in the CCLG Package

The CCLG package is programmed at the device-level the same as all other Actel antifuse products. See the *Silicon Sculptor User's Guide*. (http://www.actel.com/techdocs/manuals/default.asp#programmers)

Conclusion

The CC256 package is a KGD alternative to solve the metal-to-metal programming dilemma at the die level. This technology is critical in today's space and other high-reliability applications that will allow programmable logic to be vertically integrated with incompatible process technologies or products from multiple vendors in a smaller footprint. Due to the exposed bonding fingers, care must be exercised to avoid corrosion or damage that can lead to unreliable interconnects.

This application note provides some general guidelines to assist end users in the purpose and implementation of the CC256 package in their high reliability, multi-chip module applications. Please contact either your local Actel sales representative or tech support at tech@actel.com or the Actel Hotline at (800) 262-1060 should you need any further assistance.

Related Documents

C. Shih, R. Lambertson, F. Hawley, F. Issaq, J. McCollum, E. Hamdy, H. Sakurai, H. Yuasa, H. Honda, T. Yamaoka, T. Wada, C. Hu, Characterization and Modeling of a Highly Reliable Metal-to-Metal Antifuse for High Performance and High-Density Field-Programmable Gate Arrays, IEEE IRPS Proceedings, 25-33, (1997).

http://www.actel.com