

32-Channel Waveform Generator Implemented Using Actel's Axcelerator FPGA

Introduction

Waveform generators are widely used in high-speed applications. A few examples include communication design and test, pulse generation, high-speed, low-jitter data and clock source, and mixed-signal design and test. This application note describes how to implement a 32-channel waveform generator with 1 ns resolution in Actel's Axcelerator FPGAs.

Based on user-defined 10-bit inputs to each channel, this waveform generator can generate 32 channels of output waveforms independently. With Axcelerator's high-performance phase locked loop (PLL) core, the designer can obtain a 1.0 GHz system clock, which guarantees 1 ns resolution waveform generation. For example, Channel 0 in [Figure 1](#) is generating 4 ns, 5 ns, and 6 ns pulses, respectively.

The advanced feature demonstrated in this design is to run the system at 1.0 GHz, or generate output data with 1.0 ns resolution. Other SRAM-based FPGAs can only clock at 400 MHz (both edges) using their DDR output register modes to achieve 1.25 ns resolution. A high-performance, low-jitter, Axcelerator PLL is used to generate the 1.0 GHz system clock from a 50 MHz input reference clock. The system clock is distributed on low-skew, global networks, allowing manual placement in Designer ChipPlanner for particular logic blocks to minimize the routing delay.

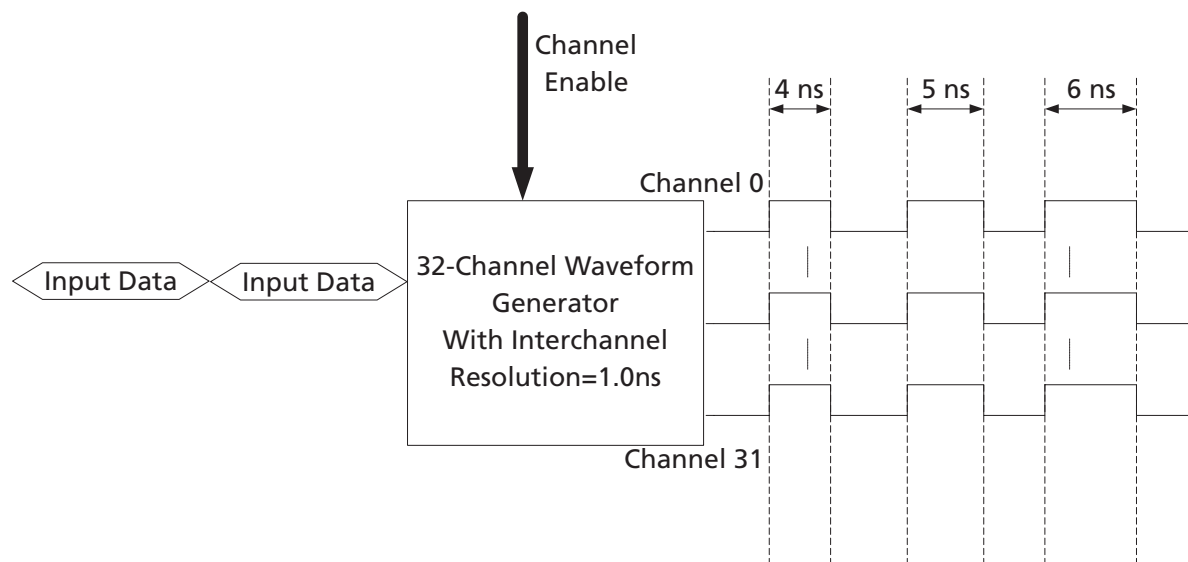


Figure 1 • Top-Level Diagram of a Waveform Generator

Design Description

Figure 2 shows the waveform generator basic block diagram of one channel. The Input Data is registered in a 10-bit Data Input Register and then propagated to a 10-bit Parallel-In-Serial-Out (PISO) Shift Register. The Load Instruction Bits Generator generates the Parallel Load Instruction and sends it to the 10-bit PISO Shift Register every 10 clock cycles. Once the 10-bit PISO Shift Register receives the Load Instruction, it loads the 10-bit Registered Input Data in parallel format and shifts them out in serial format, which becomes the output waveform.

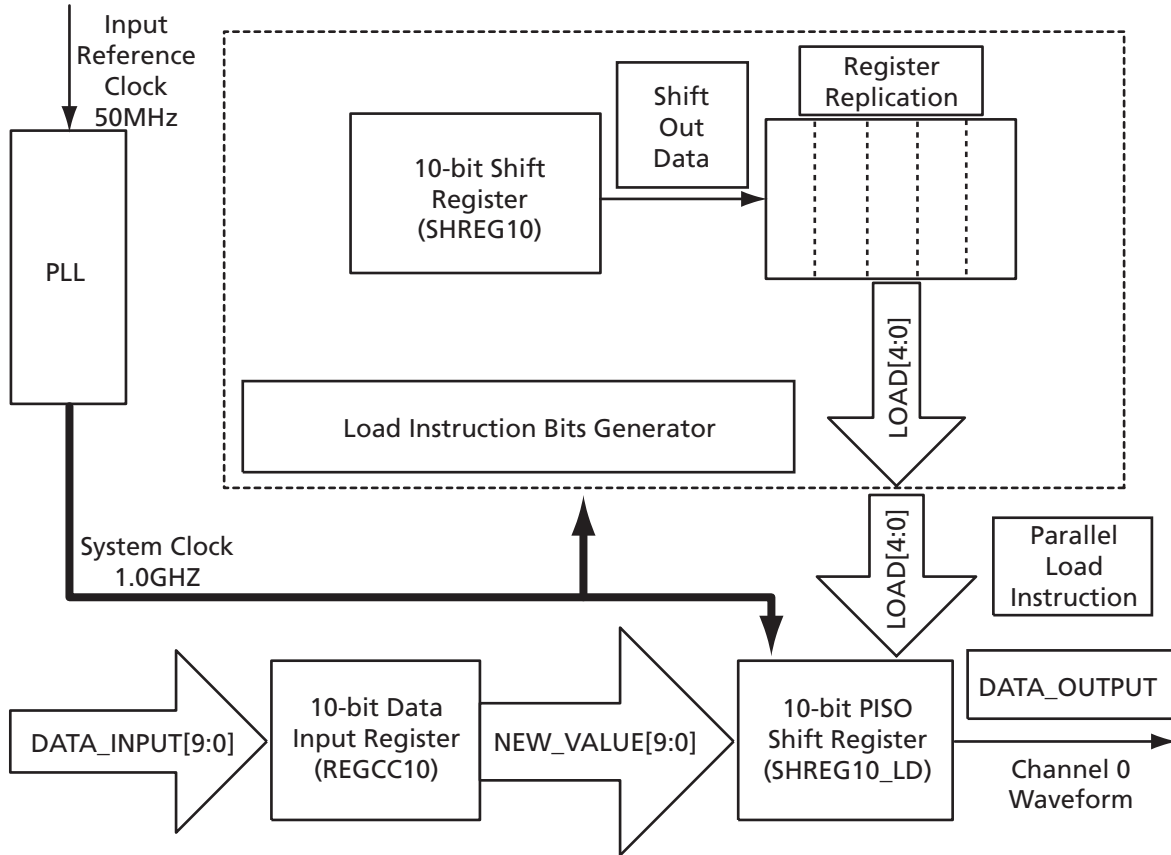


Figure 2 • Block Diagram of the Waveform Generator Channel 0

Design Implementation

Since this design has extremely aggressive timing requirements—1.0 GHz system clock—a schematic representation with embedded ACTgen cores was chosen over a behavioral VHDL approach to achieve a high degree of control. The implementation of different functional blocks is illustrated below. Table 1 shows the resources needed in this design implementation.

Table 1 • Design Resources

Design Environment	Libero™ Integrated Design Environment (IDE) v5.2 and newer versions
Target Device	AX250 FG484 (Utilization: R-cell 1120/1408 C-cell 1280/2816)
Programmer	Silicon Sculptor II

System Clock Generator—PLL

The 1.0 GHz system clock is generated from the Axcelerator PLL. Figure 3 shows the configuration of the PLL.

The screenshot shows the configuration for a PLL. It is divided into three main sections:

- REF Clock:**
 - Frequency (MHz): 50.0000
 - Delay (ns): Static (0.00), Dynamic
 - Input: Hardwired I/O / Core Logic, External I/O
- Feedback:**
 - Internal, External
- Cascading:**
 - Yes, No

Below these are two clock output sections:

- CLK1:** CLK1, Frequency (MHz): 1000.0000. Clock Out: Hardwired, Routed, Routed Net.
- CLK2:** CLK2, Frequency (MHz): 33.0000. Clock Out: Hardwired, Routed, Routed Net.

Figure 3 • System Clock Generator—PLL Configuration

10-Bit Data Input Register

The 10-bit Data Input Register (instance name: REGCC10) deployed in this design is an ACTgen core, where the configuration can be found in Figure 4.

The **Sequential Type** is set to **Combinatorial**. This uses one CC macro to implement a register instead of an R-cell in order to cut down the utilization of the R-cells.¹ The rest of the design has consumed around 80% of available R-cells.

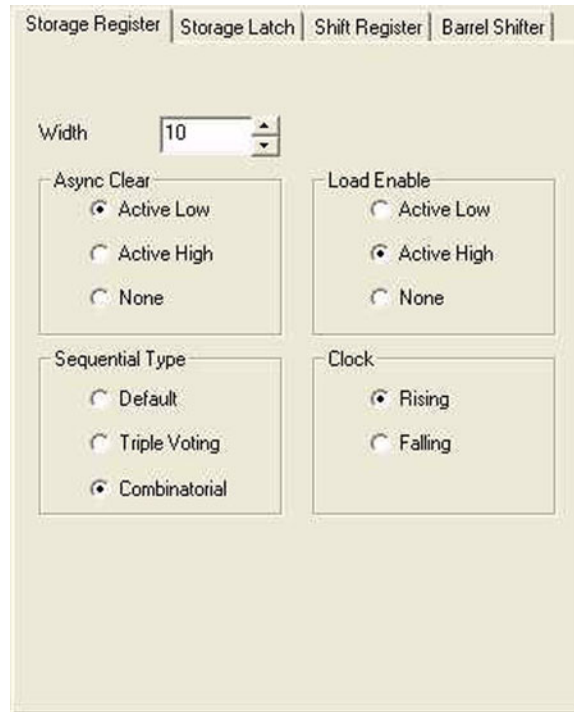


Figure 4 • 10-bit Data Input Register ACTgen Configuration

1. The CC macro is a sequential logic composed of two C-cells. Usually, these two C-cells are adjacent in the physical location of the chip.

Load Instruction Bits Generator

The main components of the Load Instruction Bits Generator are two 10-bit shift registers (instance name: SHREG10), as illustrated in Figure 5.

The 10-bit shift register generates a one-clock cycle High pulse every 10 clock cycles. Two shift register blocks were replicated to average the load on each one for timing concerns. The pulses from shift registers are registered and combined into LOAD instruction bits. Figure 6 shows the waveform of the Load Instruction Bits Generator functionality.

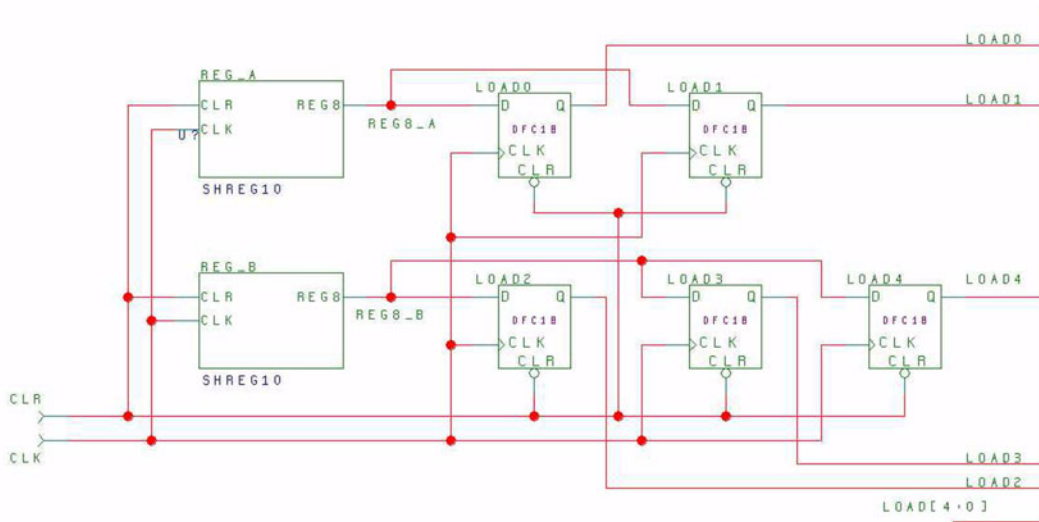


Figure 5 • Load Instruction Bits Generator

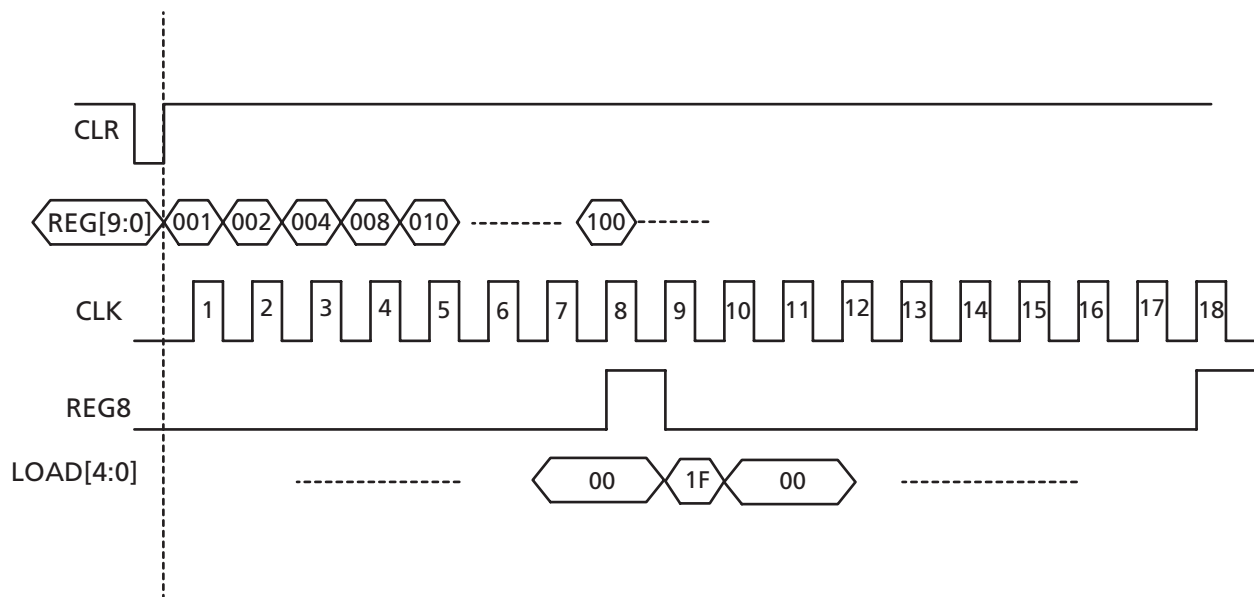


Figure 6 • Load Instruction Bits Generator Functionality Waveform

10-Bit PISO Shift Register

The 10-bit PISO Shift Register is the critical part running at 1.0 GHz system clock and also needs to support a parallel load capability. Normally, this would require a logic level in between each register that introduces additional delay. A 2:1 MUXed R-cell, DFMB, is used to implement the same logic but removes the additional logic and minimizes the register-to-register delay. Figure 7 shows the implementation details.

When LOAD[4:0] = "11111," NEW_VALUE[9:0] parallel loading is performed and when LOAD[4:0] = "00000," the loaded data of NEW_VALUE[9:0] is shifting. REG9 is the real output waveform. Figure 8 shows details of the functionality waveform.

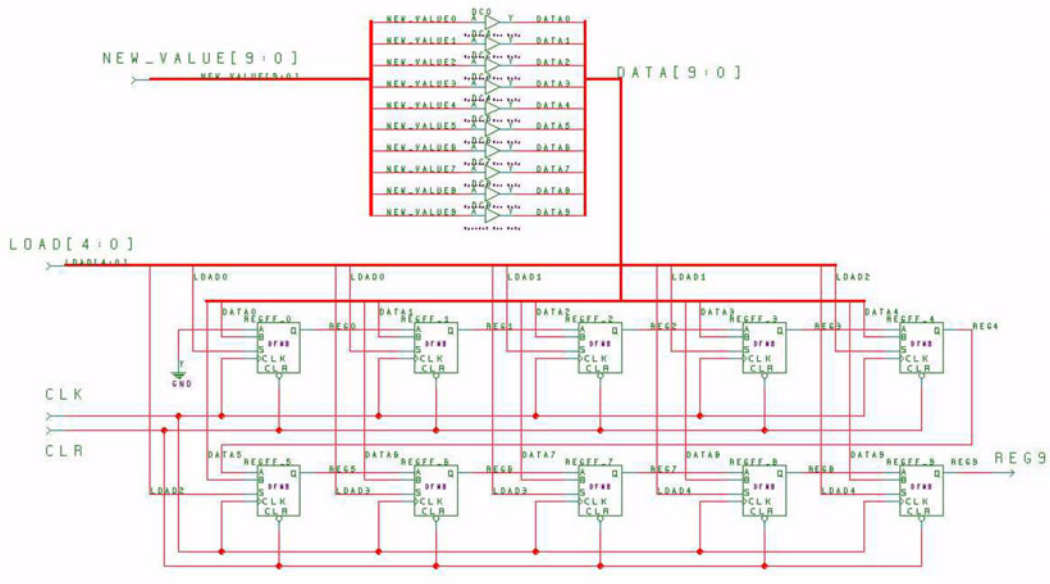


Figure 7 • 10-bit PISO Shift Register Implementation

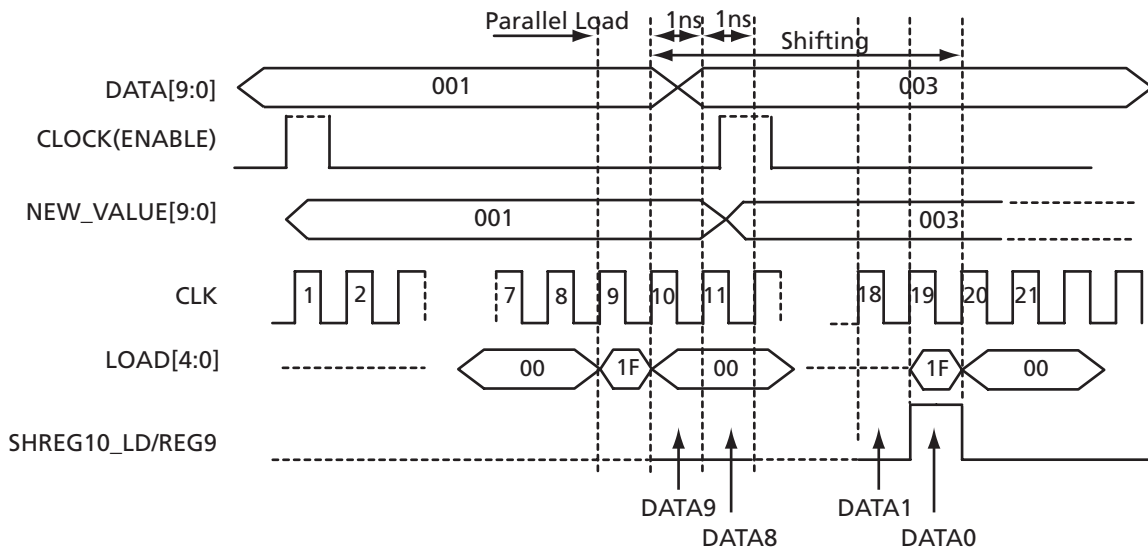


Figure 8 • 10-bit PISO Shift Register Functionality Waveform

Each channel of the Waveform Generator can run independently after the channel is enabled. Based on a different input data pattern, the output signal can be changed in a 1 ns increment. The RESET signal is deasserted after the PLL is locked. All valid input data begins assertion after RESET deassertion to ensure they are all captured properly. The channel ENABLE signal works as a clock signal for the Data Input Register block, which has a period of 10 system clock cycles. DATA_INPUT_B is reloaded every 10 cycles, following the pattern "000," "001," "003"... "3FE," "3FF," while DATA_INPUT_A follows pattern "3FF," "3FE," "3FC," ... "001," "000." Figure 9 illustrates the functional simulation results.

Shifting "3FF" on Ch0~Ch15;
Shifting "000" on Ch16~Ch31

Shifting "3F0" on Ch0~Ch15;
Shifting "00F" on Ch16~Ch31

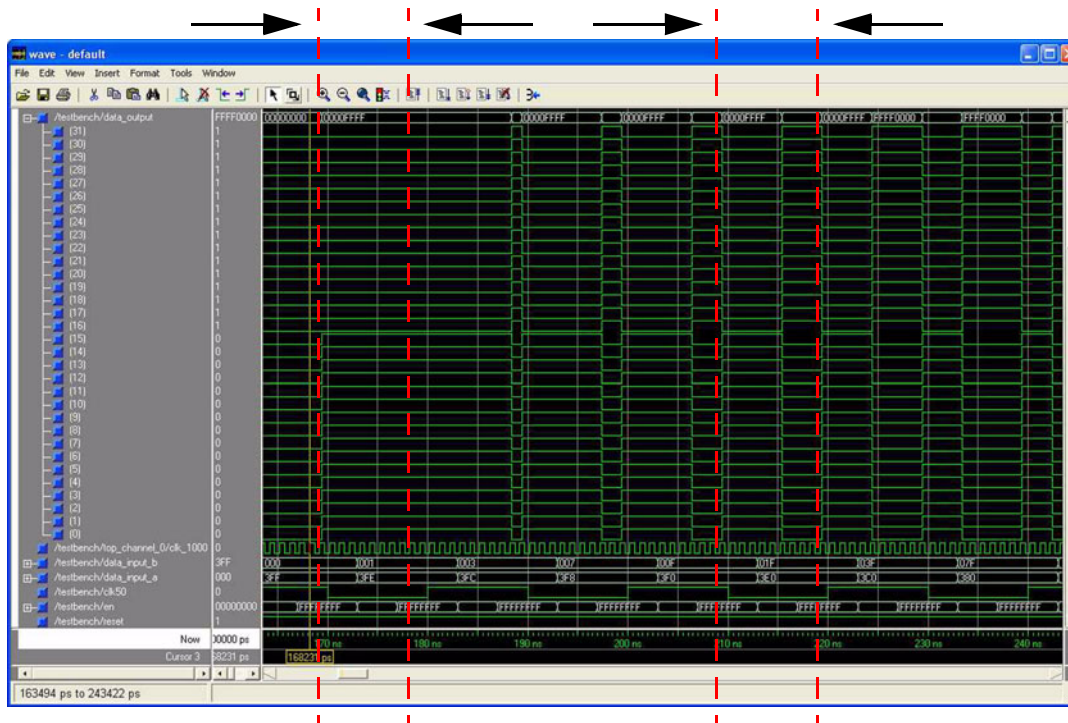


Figure 9 • Functional Simulation Result

Design Features

Some specific Axcelerator design features are used in this design. The 1.0 GHz system clock is generated from the high-performance Axcelerator PLL with low jitter and fast acquisition (lock) time. Output of the PLL, the system clock, is distributed on low-skew global networks.

ChipPlanner allows the designer to manually place logic cells for functional blocks, such as the 10-bit PISO Shift Register. This minimized the routing delay to meet the 1.0 GHz system performance requirement. For information on using ChipPlanner, refer to the Designer online help.

The 2:1 MUXed registers (DFMB) are used in the 10-bit PISO Shift Register block to implement the shift register, with parallel load capability. Figure 10 on page 8 illustrates the DFMB macro and Table 2 on page 8 presents the truth table. The B input of DFMB is mapped to the DCIN input of a R-cell. Figure 11 on page 8 illustrates the Axcelerator R-cell architecture.

The DCIN input is driven by the DCOUT of an adjacent C-cell via the DirectConnect routing resource. For more details, refer to the *Axcelerator Family FPGAs* datasheet.

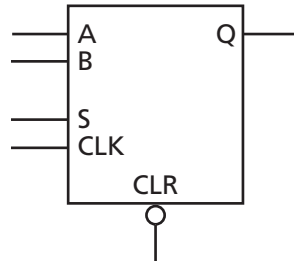


Figure 10 • DFMB Macro

Table 2 • DFMB Truth Table

CLR	S	CLK	Q_{n+1}
0	X	X	0
1	0	↑	A
1	1	↑	B

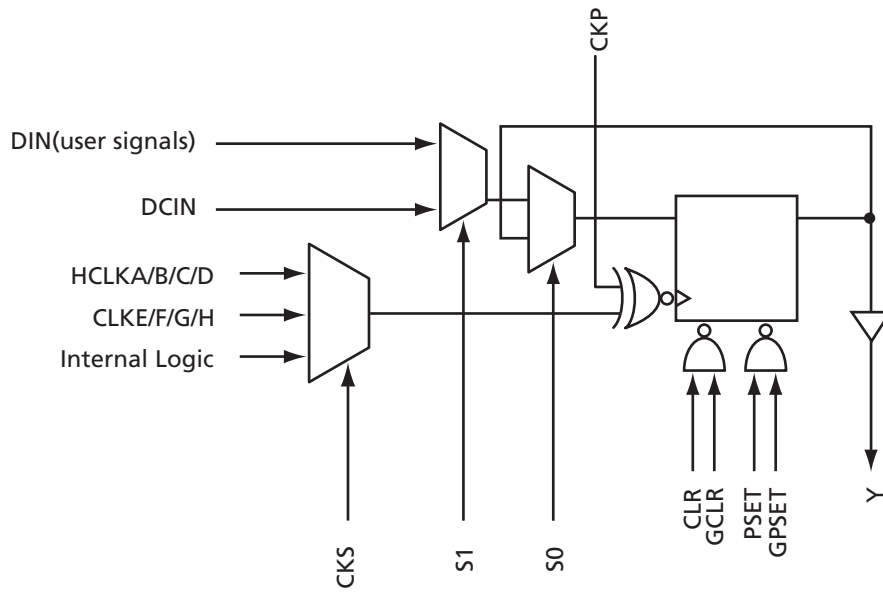


Figure 11 • R-Cell

In this design, a BUFD is used and hand-placed at the adjacent C-cell to the DFMB in order to bring the parallel load data into the B input of the DFMB via the DirectConnect. The corresponding view in ChipPlanner is illustrated in Figure 12.

This design can be implemented in Axcelerator –3 speed grade commercial devices even under worst-case conditions. To increase the timing margin, the designer can try to use a higher voltage than the minimum requirement of worst-case condition (worst = 1.425V, typical = 1.500V, best = 1.575V). All analysis of this design was done at 1.575V, which is the best-case voltage. However, other factors affecting timing analysis still remain on worst-case, such as temperature and process.

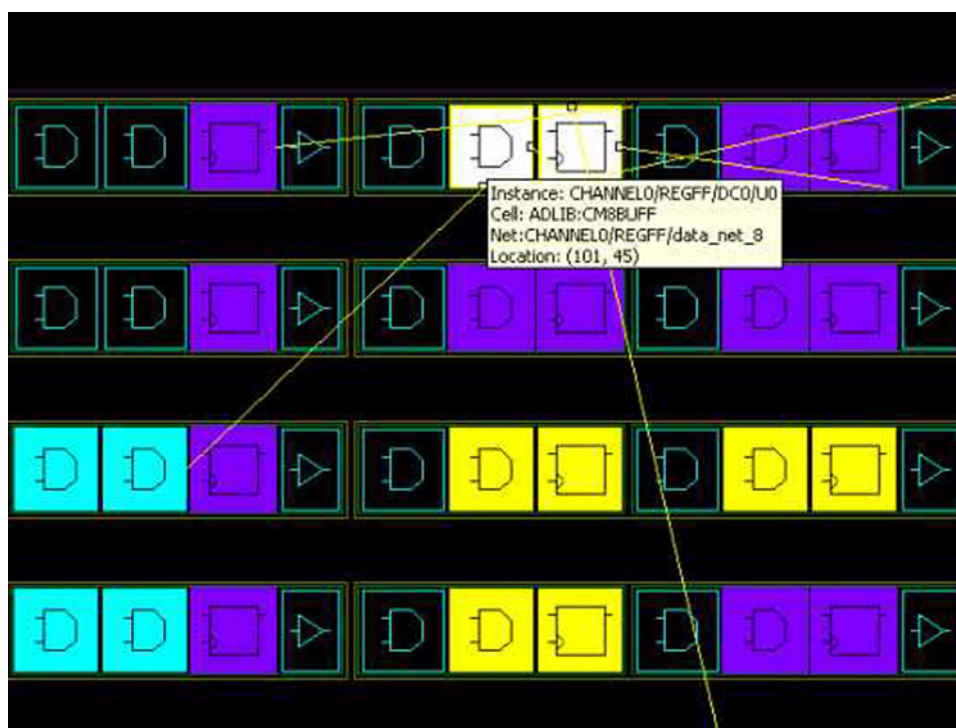


Figure 12 • ChipPlanner View of DirectConnect

Conclusion

The design used in this application note demonstrated that Axcelerator's high-performance PLL can run in a stable manner at 1.0 GHz and outperform other SRAM-based FPGA products. The nonvolatile feature makes it possible for the Waveform Generator to provide high-resolution waveforms to test equipment right after power-up. The 32 channels can run independently to generate user-defined waveforms. They can also be used together and chosen separately at a different time to create various waveforms for a given target device. The designer can change the PLL configuration to adjust the system clock frequency if the system performance and waveform resolution requirements are different.

Related Documents

Datasheets

Axcelerator Family FPGAs

http://www.actel.com/documents/AX_DS.pdf

User's Guides

Antifuse Macro Library Guide

http://www.actel.com/documents/libguide_UG.pdf

Libero IDE User 's Guide

http://www.actel.com/documents/libero_UG.pdf

Designer User 's Guide

http://www.actel.com/documents/designer_UG.pdf

ChipPlanner in MultiView Navigator User 's Guide

http://www.actel.com/documents/mvn_ug.pdf

ACTgen Cores Reference Guide

http://www.actel.com/documents/gen_refguide_UG.pdf

Appendix

Figure 13 shows the hierarchy of this design.

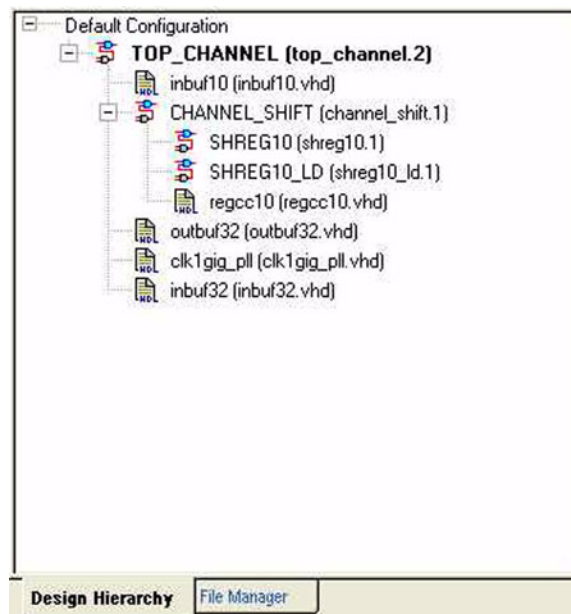


Figure 13 • Design Hierarchy

Among all these blocks, "inbuf10," "inbuf32," "outbuf32," "clk1gig_pll," and "regcc10" are ACTgen cores; the rest are schematics. The whole design in the Libero IDE project directory with the top-level folder named "wfg32" is located in the wfg32.zip file.

Figure 14 illustrates the design directory hierarchy.

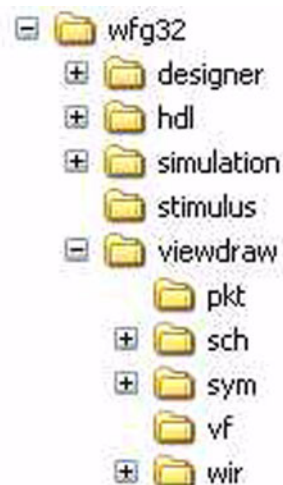


Figure 14 • Design Directory Hierarchy

An .ADB file with compilation and layout done is located inside the \designer folder. The user can open the .ADB file in Designer v5.2 or newer to check out the compile and layout information, do timing analysis in Timer, review manual placement results in ChipPlanner, or generate various reports. The \designer folder also has the _ba.vhd and _ba.sdf files, which are used for post-layout simulation.

The \hdl folder contains all .GEN files and corresponding .VHD files for all ACTgen macros in this design. The user can reload these .GEN files into ACTgen Core Generator to check the configurations of these macros.

The \stimulus folder includes all the testbenches for different levels of this design. The user can set different level as root in Libero IDE and run simulation for it after associating corresponding testbench.

The \viewdraw folder has all schematic files and symbol files for this design.

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