IEEE Standard 1149.1 (JTAG) in the Axcelerator Family

Introduction

Testing modern loaded circuit boards has become extremely expensive and very difficult to perform. The rapid development of surface-mount technology and the use of multi-layer boards has increased board complexity. Finer pin spacing and double-sided boards have also contributed to the increasing cost and difficulty of testing. Traditional testing uses methods such as in-circuit testing by bed-of-nails and functional testing. Although functional testing can cope with complex and dense boards, it is costly because different designs require different sets of test programs.

The test architecture was developed by the Joint Test Action Group and later adopted by IEEE as the IEEE Standard Test Access Port and Boundary-Scan Architecture (also referred to as IEEE Standard 1149.1 or informally known as JTAG). The standard provides a cost-effective method of board testing through use of the boundary-scan technique. Boundary scan provides the means to test each component's required performance, interconnections, and interaction. In addition to describing boundary scan, the standard also describes the design-for-test feature.

Overview

The Actel Axcelerator® family devices are compliant with IEEE Standard 1149.1.[1] Figure 1 shows the major parts that make up the JTAG test logic circuit. The circuit provides the required components (Test Access Port controller and registers) to support all the mandatory boundary-scan instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) as well as six optional public instructions (INTEST, USERCODE, IDCODE, Diagnostic, HIGHZ, and CLAMP). The diagnostic instruction is very similar to the JPROBE instruction on Actel's legacy parts.

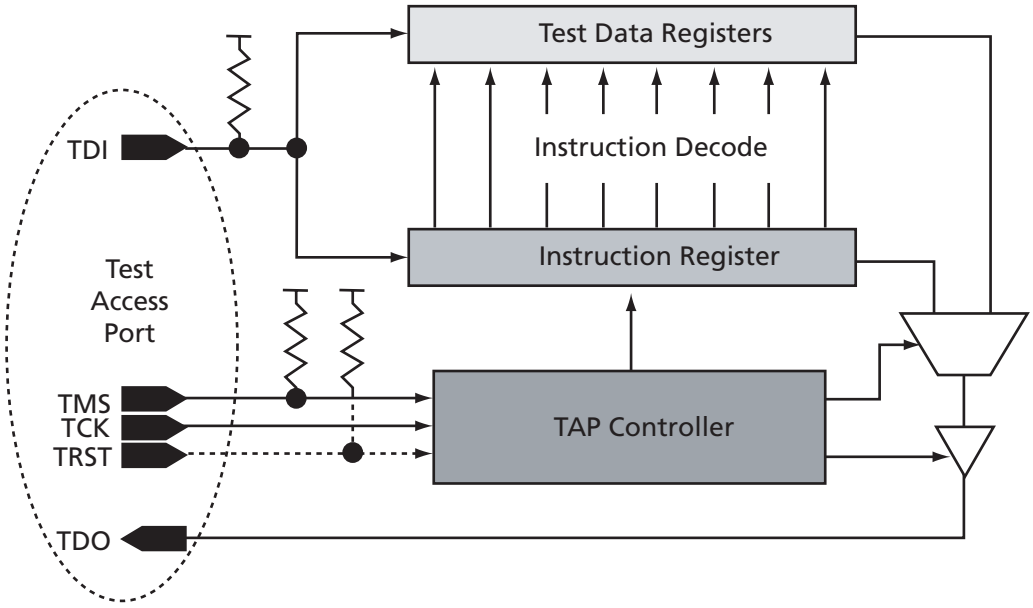

Figure 1 • **JTAG Block Diagram**

1. *There are two minor exceptions. See the "Instructions" section on page 6 and the "Axcelerator ID Code" section on page 7.*

JTAG Mode Selection

Enter JTAG test logic mode in Actel Designer software by selecting **Tools** > **Device Selection**. Click **Next** and the Variations dialog box appears, as shown in Figure 2. Click the **Reserve JTAG** check box to reserve pins for JTAG (dedicated mode). Dedicated mode is recommended if JTAG is to be used extensively. If the box is not checked, flexible mode is selected by default.

The JTAG dedicated mode can also be selected when using TCL scripting by adding the command:

```
set_device -jtag "yes"
```

If the unshaded box, **Reserve JTAG Test Reset**, appears (SX-A or eX devices), the user also has the option of reserving a pin for the JTAG TRST signal (see the "Test Access Port (TAP)" section). The JTAG TRST pin can be reserved when using TCL scripting with the command:

```
set_device -trst "yes"
```

These can also be done with a single line:

```
set_device -jtag "yes" -trst "yes"
```[2]

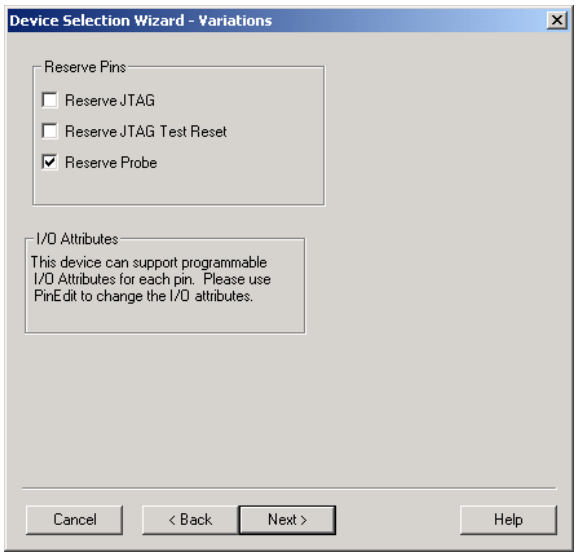

Figure 2 • **SX-A Device Selection Dialog Box**

Test Access Port (TAP)

Each test logic function is accessed through the Test Access Port. The five pins associated with the TAP are listed in Table 1 on page 3 with their corresponding descriptions. Four pins – TMS, TCK, TDI, and TDO – are always required for JTAG operation. The fifth pin, TRST, is optional. These pins are dedicated pins – used only with the test logic. If flexible mode is selected, three of the pins – TCK, TDI, and TDO – are free to be used as regular I/O pin (Figure 3 on page 4). Note that TRST (if present) and TDI are equipped with internal pull-up resistors. This means that these pins do not need to be terminated in either flexible or dedicated mode to ensure proper JTAG operation. In dedicated mode, the TMS pin is equipped with a pull-up resistor to place the TAP controller in the reset state (after a minimum of 5 TCK pulses) when no input is present. In flexible mode, there is NO pull-up resistor; an external 10 kΩ pull-up resistor is required. The test logic was designed to be in the reset state on power-up.

2. *This has been tested in a simple eX64-TQ64 design and the only variables affected are the RESTRICTJTAGPINS and RESTRICTTRSTPIN, respectively.*

Table 1 • **Test Access Port Descriptions**

Port	Description
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock (TCK). An internal pull-up resistor is present in dedicated mode but not in flexible mode. See the "Test Access Port (TAP)" section on page 2 for more information.
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock. The maximum clock frequency for TCK is 20 MHz.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock. This pin is equipped with an internal pull-up resistor.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.
TRST (Test Reset)	Active-low input which asynchronously resets the test logic. This pin is equipped with an internal pull-up resistor.

TRST Pin

The Axcelerator device is equipped with a dedicated TRST pin. The TRST overrides the behavior of TMS and TCK. In other words, asserting TRST will reset the TAP controller regardless of the states of TMS and TCK. Also, if the TAP controller is held in reset, asserting TMS and TCK will have no effect. The TAP controller will remain in the reset state. The TRST pin is equipped with an internal 10 kΩ pull-up resistor.

TAP Controller

The 16 states of the tap controller state machine are shown in Figure 4 on page 4. The 1s and 0s shown adjacent to the state transitions represent the TMS values that must be present at the time of a rising edge at TCK for a state transition to occur. In the states that include the letters -IR, the instruction register operates; in the states that contain the letters -DR, the test data register operates (bypass, boundary-scan, and XY-registers). The TAP controller receives two control inputs, TMS and TCK, and generates control and clock signals for the rest of the test logic architecture, as illustrated in Figure 5 on page 5.

On power-up (or on the assertion of TRST), the TAP controller enters the Test-Logic Reset state. To reset the controller from any other state, TMS must be held high for at least five TCK cycles. After reset, the TAP controller's state changes at the rising edge of TCK based on the value of TMS.

Note: The value shown adjacent to the state transitions in Figure 4 on page 4 represents the signal present at TMS at the time of the rising edge of TCK.

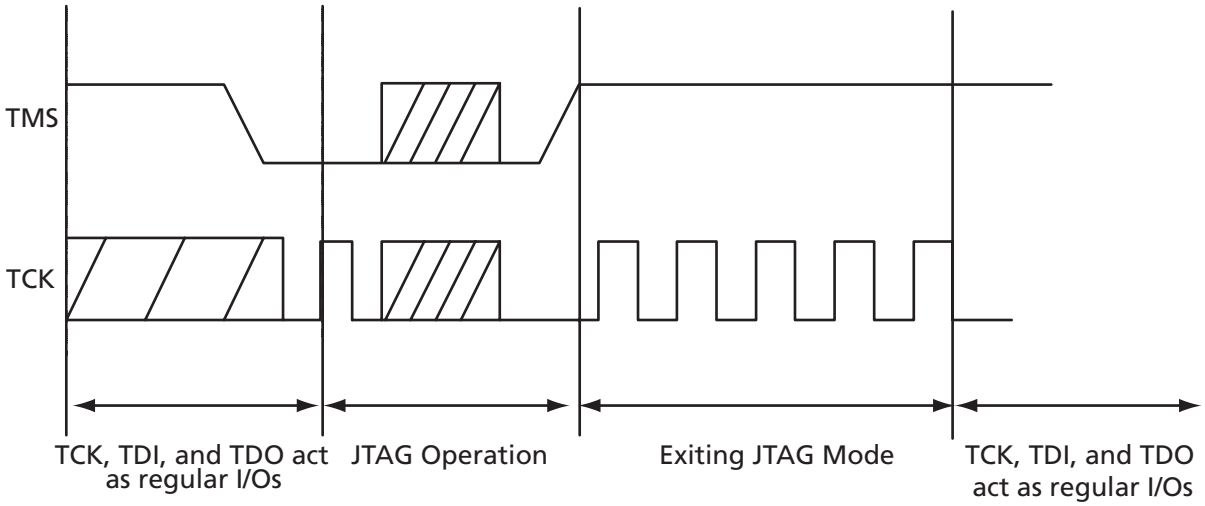

Figure 3 • **Entering and Leaving JTAG Flexible Mode**

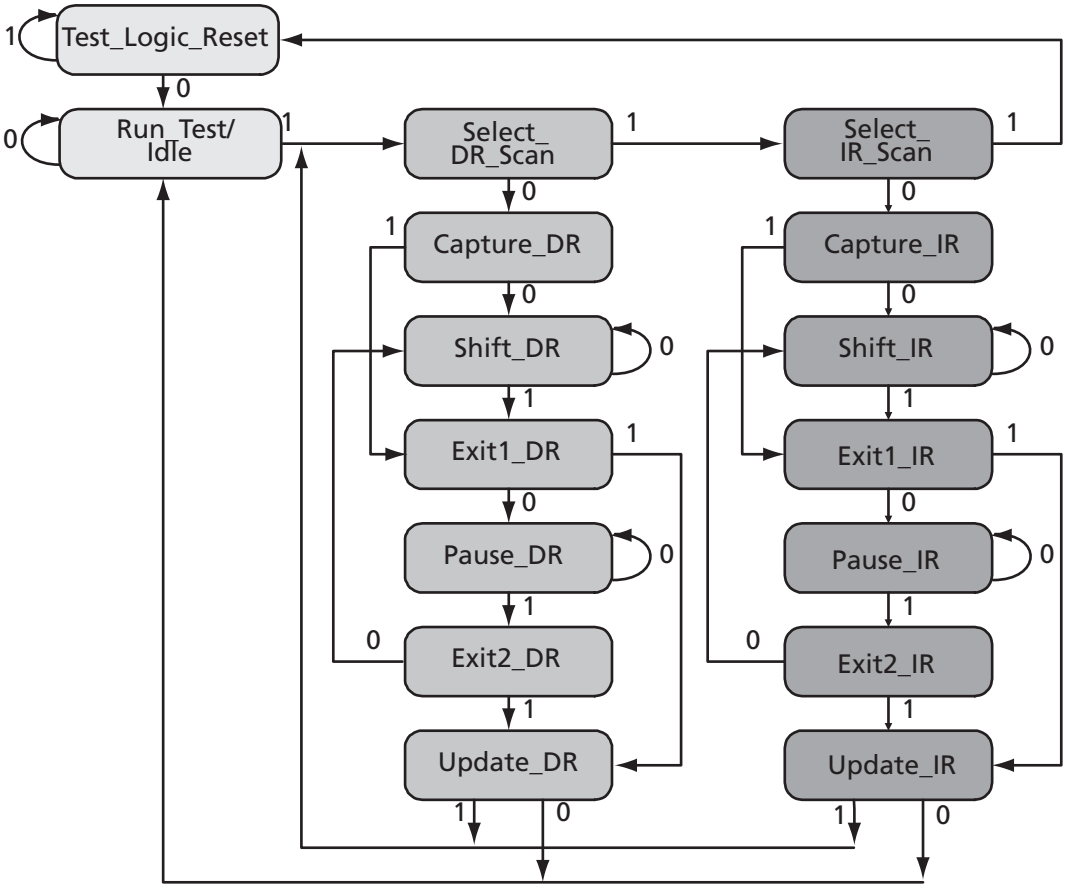

Figure 4 • **TAP Controller State Diagram**

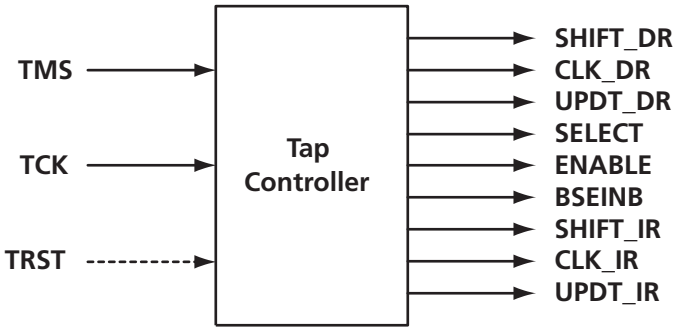

Figure 5 • **TAP Controller Block Diagram**

Instruction Register

The instruction register (IR) consists of five IR cells. Each cell has a shift-register stage and a latch stage (Figure 6). On the Capture_IR state, the shift register is loaded with bits 11101, which are used for fault isolation of the board-level serial test data path. The TDI-IR-TDO path is established on the Shift_IR state. Data in the shift register is shifted toward TDO, and data in the latch remains the same. The data in the shift registers is latched out and becomes the current instruction on the falling edge of the TCK in the Update_IR state. When the TAP controller enters the Test-Logic Reset state, bits 00100 are latched in the IR, which corresponds to the IDCODE instruction, and the data in the shift register cell retain their previous values. Table 2 on page 6 shows the summary of the operation of the instruction register.

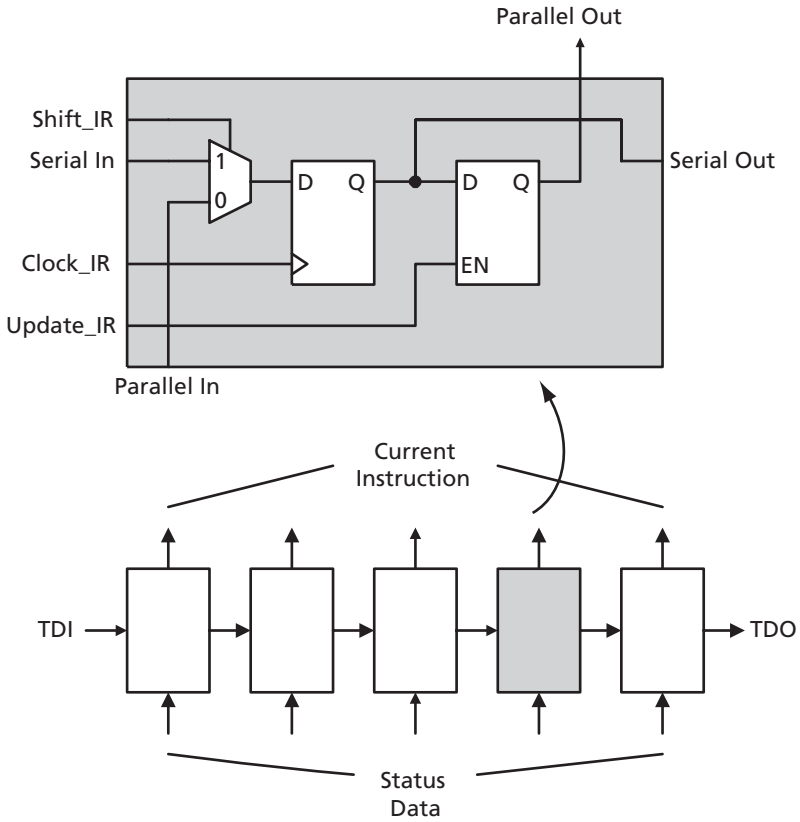

Figure 6 • **Instruction Register Block Diagram**

Table 2 • **Instruction Register Operation**

Controller State	Shift-Register Stage	Latch Stage
Test_Logic_Reset	Undefined	IDCODE Instruction (IR4 – IR0 = 00100)
Capture_IR	11101 is loaded	Retain Previous State
Shift_IR	Shift Data Toward TDO	Retain Previous State
Exit1_IR	Retain Previous State	Retain Previous State
Exit2_IR		
Pause_IR		
Update_IR	Retain Previous State	Latch Data from Shift Register
All Other States	Undefined	Retain Previous State

Instructions

Table 3 lists the supported instructions with their corresponding IR codes and descriptions. Because some unused opcodes are employed during Actel testing, all unused opcodes should be considered reserved.

Note that the INTEST instruction does not fully comply with rule 7.8.1(b) of IEEE Standard 1149.1-1990. No single-step capability for the three clock inputs HCLK, CLKA, and CLKB is provided because these are high-performance clock pins and only "observable" boundary-scan cells are included in the scan chain. The same comment applies to the quadrant clocks (QCLKA/B/C/D) on the A54SX72A and the RT54SX72S.

Table 3 • **Supported Public Instructions**

Instruction	IR Code (IR4 – IR0)	Instruction Type	Description
EXTEST	00000	Mandatory	Allows testing of off-chip circuitry and board-level interconnections
SAMPLE/PRELOAD	00001	Mandatory	Allows a snapshot of the normal operation of the component to be taken and examined
INTEST	00010	Optional	Allows testing of on-chip system logic while component is assembled on the board
USERCODE	00011	Optional	32-bit user-programmable identification code
IDCODE	00100	Optional	32-bit hard-wired Actel ID, part number, and version number
HIGHZ	01110	Optional	Tristates all I/Os to allow external signals to drive pins.
CLAMP	01111	Optional	Allows state of signals driven from component pins to be determined from the Boundary-Scan Register.
Diagnostic	10000	Optional	Allows microprobing of internal logic module's output logic state
BYPASS	11111	Mandatory	Provides minimum-length (1-bit) serial path between TDI and TDO pins of component when no test operation of that component is required

Axcelerator ID Code

The JTAG standard specifies that a JTAG compliant device must have the ID Code register or the Bypass register connected between TDI and TDO immediately after a power-on reset, this allows a JTAG tester to obtain the device ID code and any other information contained in the identification registers of the device. The Axcelerator device connects the ID Code register after the power-on reset. This scheme allows a JTAG tester to shift out the ID code of the device (or devices in a daisy-chain) and verify that the correct devices are soldered onto the board.

The JTAG standard also specifies that an ID Code must be 32 bits, though the Axcelerator device has an expanded 33-bit ID code to improve post programming verification of the charge pump. With testers that support user customization, such as Teradyne's J750, this 33-bit ID code is not an issue. For these testers, the user simply configures the tester to shift out 33 bits instead of 32 bits on the Axcelerator device. However, some testers have limited or restricted options for user customization and the Axcelerator 33-bit ID Code may generate an error.

Some testers perform a blind interrogation of the daisy-chain (a daisy-chain can contain one single device) to verify the devices in the chain. When a blind interrogation is performed, these testers default to a standard setting and assume all the devices in the chain contain 32-bit ID codes; when reading out the Axcelerator 33-bit ID code some tools will incorrectly recognize this as an invalid IDCODE.

Figure 7 is an example of a chain in which all devices have 32-bit ID codes. When blind interrogation is performed, the software simply reads 32 bits at a time to obtain the correct ID code. Figure 8 on page 8 is an example of what happens when the 33-bit ID code is introduced to the chain. The 33-bit ID code may cause some tools to misread the ID codes of the devices after the 33-bit ID code device.

In the event the tester in use will not allow the user to implement the previous solution, it is recommended to omit or bypass the Axcelerator ID Code check in the test flow. Once the ID Code check is bypassed, the user can perform complete functional JTAG testing on the chain. For some testers, such as JTAG technologies, simply removing the ID Code register from the BSDL file is sufficient. Removing the ID Code register from the BSDL file will enable the JTAG technology tester to automatically put the Axcelerator device into bypass mode. Once the Axcelerator device is in bypass mode, it will contribute only a single bit to the ID code of the entire chain (Figure 9 on page 8). This will allow the user to verify the ID codes of all other devices in the chain.

The Axcelerator device supports all the necessary JTAG instructions and tests. The 33-bit ID code will not prevent users from using any of the JTAG instructions and tests. Some JTAG testers may require some user customization to accommodate the Axcelerator 33-bit ID code. To handles issues related to the 33-bit ID code, Actel recommends contacting the manufacturer of the tester to obtain the most up to date solution.

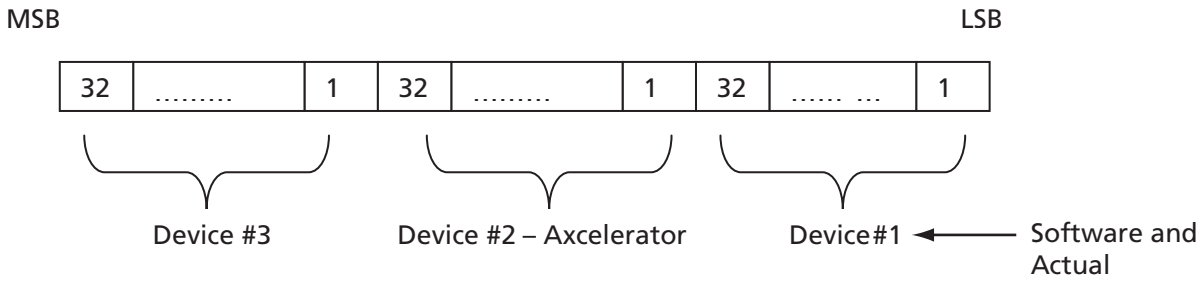

Figure 7 • **Chain Containing 32-Bit ID Code Devices Only**

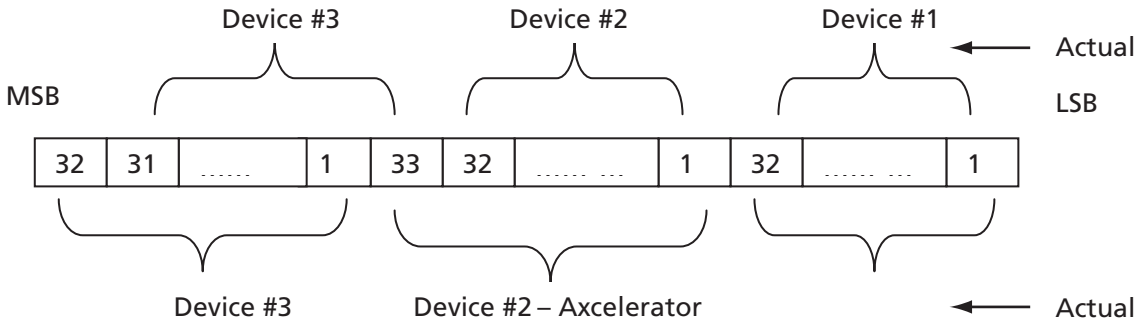

Figure 8 • **Chain Containing 33-Bit ID Code Device**

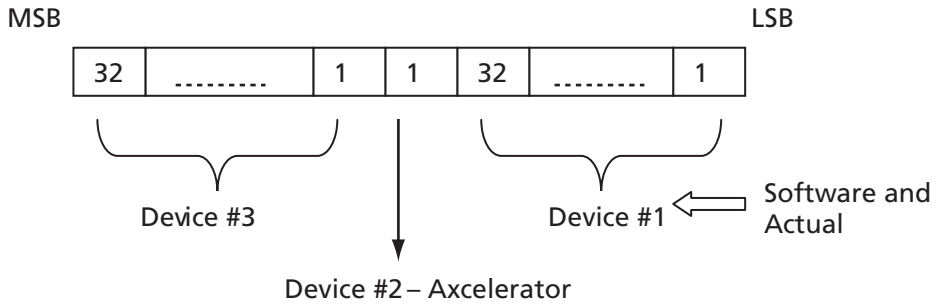

Figure 9 • **Axcelerator Device in Bypass Mode**

Bypass Register

The Bypass register is a single-bit register that provides a minimum data path between the TDI and TDO pins (Figure 10). The bypass register is selected when the BYPASS, HIGHZ, or CLAMP instruction is the current instruction in the instruction register. On the Capture_DR controller state, 0 is loaded into the bypass register. Test data can then be shifted from the TDI pin to the TDO pin on the Shift_DR state. Data movement throughout the bypass register is terminated when it moves into the Update_DR controller state. Table 4 shows a summary of the operation of the bypass register.

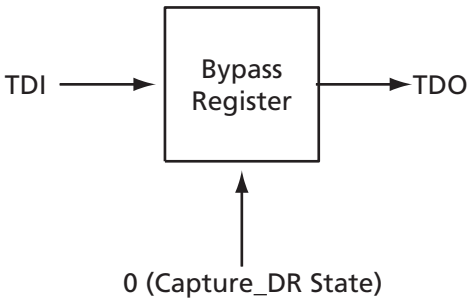

Figure 10 • **Bypass Register Diagram**

Table 4 • **Bypass Register Operation**

Controller State	Bypass Register
Test-Logic-Reset	Retain previous state
Capture_IR	'0' is loaded
Shift_IR	Shift data toward TDO
Exit1_IR	Retain previous state
Exit2_IR	
Pause_IR	
Update_IR	Retain previous state
All Other States	Undefined

Boundary-Scan Register

The boundary-scan register is used to observe and control the state of each system pin. Note that clock pins can only be observed, not controlled. Each boundary-scan cell consists of serial input (SI) and serial output (SO) that are connected to each cell, as shown in Figure 6 on page 5. In addition, each boundary-scan cell (BSC) consists of a parallel input (PI) and a latched parallel output (PO) that connect to the system logic and system output. Three cells are used for each I/O – an input cell (BS2), an output cell (BS1), and an output-enable cell (BS0).

The operation of the boundary-scan register during specific boundary-scan instructions is described in Table 5 on page 10 and Table 6 on page 10. If the EXTEST instruction is not being used in conjunction with the SAMPLE/PRELOAD instruction, the external test starts by shifting the desired test data into the boundary-scan register in the Shift_DR controller state. By moving into the Update_DR controller state, data shifting is terminated. The falling edge of the TCK, the data from the shift-register stage is transferred onto the parallel output of the latch stage. The external test results are loaded into the shift-register stage from the system input in the next Capture_DR controller state. These results are examined by shifting the data toward TDO on the next Shift_DR controller state. During the SAMPLE/PRELOAD instruction, the Shift_DR state is used to shift out the data captured from the system input and output pins for examination during the Capture_DR state. At the same time, the Shift_DR state shifts in test data to be used by the next boundary-scan instruction (other than SAMPLE/PRELOAD). The EXTEST instruction is usually initiated following the SAMPLE/PRELOAD instruction. The data pre-loaded during the SAMPLE/PRELOAD instruction phase becomes available at the parallel output of the boundary-scan cells when the EXTEST becomes the current instruction on the rising edge of TCK in the Update-IR state. Similarly, the CLAMP instruction is usually initiated following the SAMPLE/PRELOAD instruction. The latched data in the boundary-scan cell becomes available to the system output pins when CLAMP becomes the current instruction and when the bypass register is selected as the data path from TDI to TDO.

During the SAMPLE/PRELOAD instruction, the parallel input and output of the boundary-scan cells are transparent (PI equals PO).

Table 5 • **Operation Summary of EXTEST Instruction**

Controller State	Boundary-Scan Shift-Register Stage	Boundary-Scan Latch Stage	Parallel Output (PO)
Test_Logic_Reset	Undefined	Undefined	Parallel In = Parallel Out
Capture_DR	Data at PI Is Loaded	Retain previous state	Latched Data
Shift_DR	Shift Data Toward TDO	Retain previous state	Latched Data
Exit1_DR, Exit2_DR, Pause_DR	Retain Previous State	Retain previous state	Latched Data
Update_DR	Retain Previous State	Latches Data from Shift Register	Latched Data = Parallel Out
All Other States	Retain Previous State	Retain previous state	Latched Data

Table 6 • **Operation Summary of SAMPLE/PRELOAD Instruction**

Controller State	Boundary-Scan Shift-Register Stage	Boundary-Scan Latch Stage	Parallel Output (PO)
Test_Logic_Reset	Undefined	Undefined	Parallel In = Parallel Out
Capture_DR	Retain Previous State	Data at PI is loaded	Parallel In = Parallel Out
Shift_DR	Shift Data Toward TDO	Retain previous state	Parallel In = Parallel Out
Exit1_DR, Exit2_DR, Pause_DR	Retain Previous State	Retain previous state	Parallel In = Parallel Out
Update_DR	Retain Previous State	Latches data from Shift Register	Parallel In = Parallel Out
All Other States	Retain Previous State	Retain previous state	Parallel In = Parallel Out

Note: *During the SAMPLE/PRELOAD instruction, the parallel input and output of the boundary-scan cells are transparent (PI equals PO).*

Diagnostic Instruction

The diagnostic instruction (IR code 10000) allows microprobing of internal module outputs. This is done via an XY-register. The scan chain structure is illustrated in Figure 11 on page 11. The XY-register consists of a shift register whose length depends on the specific part. The registers that are darkened are not parts of the XY-register. The presence of the XY-register and the diagnostic instruction permits the use of the internal probe circuitry to observe and analyze any signal inside an Actel chip via JTAG.

The desired probe address is shifted into the XY-register by first selecting the diagnostic instruction and then moving to the Shift_DR controller state. Shifting is discontinued by entering the Update_DR controller state. The probe results are loaded into the XY-register on the rising edge of TCK in the next Capture_DR controller state. The probe results can be examined by moving back to the Shift_DR controller state and shifting the result toward TDO. Table 7 on page 11 shows the summary of the diagnostic instruction's operation. The probe results may also be observed in real time at the probe pins (PRA and PRB), provided that these pins have been reserved for probe use.

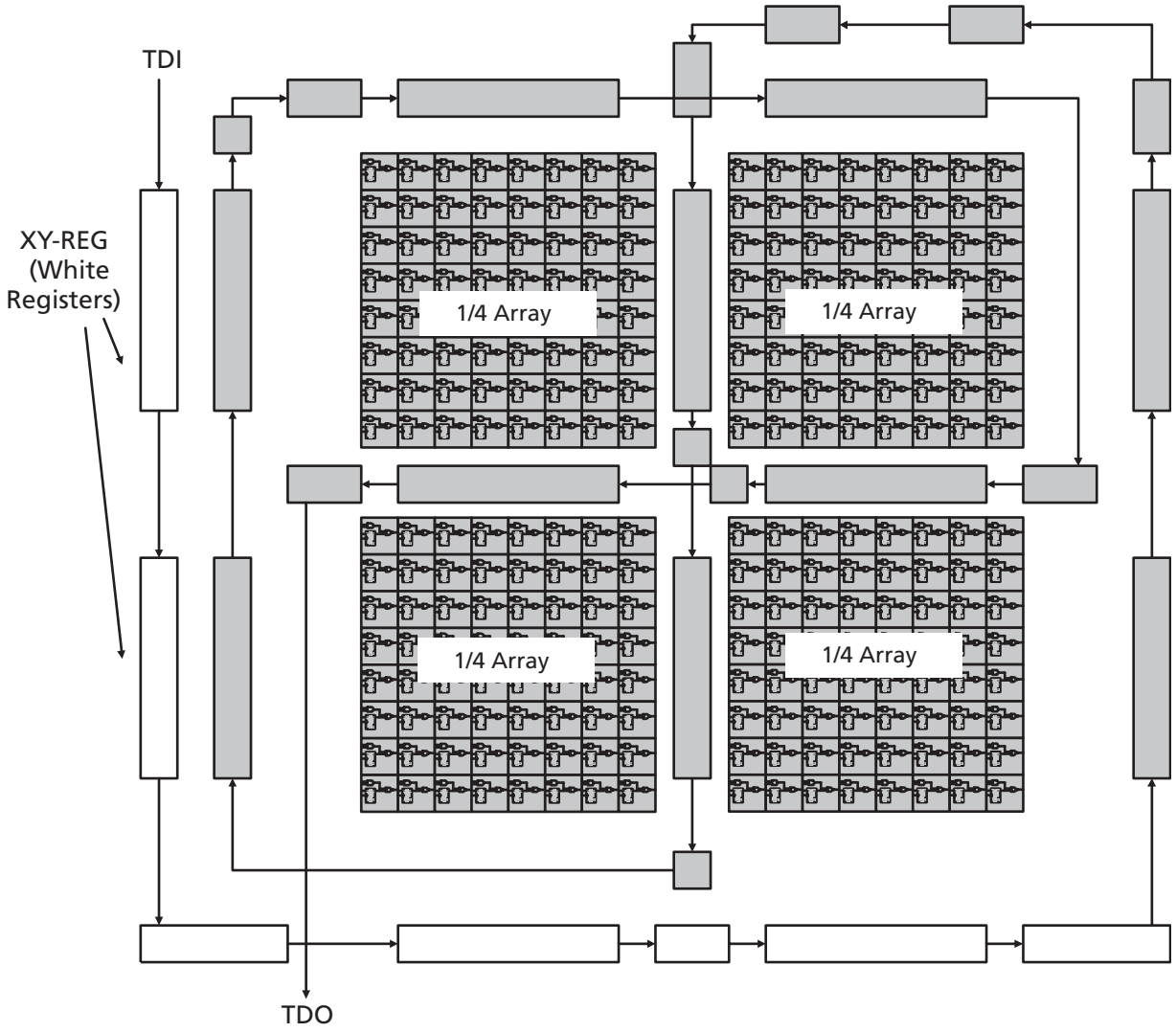

Figure 11 • **Functional Schematic of the XY-Register**

Table 7 • **Operation Summary of Diagnostic Instruction**

Controller State	XY-REG Register	XY-REG Latch Stage
Test_Logic_Reset	Logic '0'	Logic '0'
Capture_DR	Probe Result Loaded when Valid Probe Register Address	Retain Previous State
Shift_DR	Shift In New Address and Shift Out Probe Result Toward TDO	Retain Previous State
Exit1_DR, Exit2_DR,Pause_DR	Retain Previous State	Retain Previous State
Update_DR	Retain Previous State	Latch Data from Shift Register
All Other States	Undefined	Undefined

Boundary-Scan Description Language (BSDL) File

Conforming to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components that can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order. Note that if a general-purpose I/O in a customer design is configured as either an output (OUTPUT) or a tristate buffer (TRIBUF), the input for that pad and hence the JTAG input boundary-scan cell (the lower cell in Figure 11 on page 11) is disabled. This cell does not exist in the BSDL file generated by Designer Software.

References

1. Colin M. Maunder & Rodham E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. IEEE Computer Society Press, Los Alamitos.
2. "IEEE Std 1149.1-1993, IEEE Standard Test Access Port, and Boundary-Scan Architecture." IEEE, Inc., New York.
3. Kenneth P. Parker. *The Boundary-Scan Handbook*. Kluwer Academic Publishers, Norwell.

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