Axcelerator Family Footprint Compatibility

The Axcelerator family offers devices in a variety of densities and FBGA packages to fit your application needs. Should your design requirements change over the course of the design cycle, the Axcelerator family allows you to migrate to a device of different density and/or FBGA package with ease.

Table 1 lists the FPGA packages available in the Axclerator family. Those in the same color support package migration.

Table 1 • **Axcelerator Offerings in FBGA Packages**

	AX125	AX250	AX500	AX1000	AX2000
FG256	✓	✓			
FG324	✓				
FG484		✓	✓	✓	
FG676			✓	✓	
FG896				✓	✓
FG1152					✓

Two issues a designer must take into account when migrating a design in the FBGA package are as follows:

1. V_{CCDA} pin locations
2. I/O bank assignments

V_{CCDA} Pin Locations

The V_{CCDA} pin supplies power to the differential I/Os and the control circuits. In the Axcelerator family, the larger devices require more V_{CCDA} pins than the smaller devices. V_{CCDA} pins that appear in the larger device's pin description may become No Connect (NC) pins in the smaller devices of the same package.

When a designer wants the flexibility to migrate a given design to a larger device, the board layout must include the V_{CCDA} connections needed for the largest device that will be used. Actel recommends is to laying out the board using the pinouts of the biggest device in a given package**.** For example, when using the FG484 package, simply connect all the V_{CCDA} pins using the AX1000-FG484 pinout table.

As the NC pins are not bonded to the die in the smaller package, connecting the NC pins to the V_{CCDA} will not have any effect on the operation of the device. The designer can use the Axcelerator ball maps to determine which NC pins are affected (available at www.actel.com/documents/AX_Ball_Maps.zip).

I/O Bank Assignments

The Axcelerator family features a flexible I/O structure, supporting a range of mixed voltages with its bank-selectable I/Os. Across the various device package combinations, certain I/Os in the same pin location may belong to different I/O banks. If the I/O is used with a single-ended standard, there is no migration issue. Care should be taken to ensure that these pins are not used as voltage-referenced I/Os because V_{REF} pins from a different I/O bank will control them after design migration. Similarly, these pins should not be used as V_{REF} pins. Once again, the designer should use the Axcelerator ball maps to determine which pins are affected (available at www.actel.com/documents/AX_Ball_Maps.zip).

Conclusion

The Axcelerator family of devices support design migration, allowing designers the flexibility of moving to a larger device or a different package. However, care must be taken regarding V_{CCDA} pins and I/O bank assignments.

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