Preloading of ProASIC®/ProASIC^PLUS® RAM Models for Simulation Using Actel Libero® IDE Software

Introduction

This application note describes how to preload RAM models in VHDL and Verilog simulations using Actel Libero Integrated Design Environment (IDE) software.

Libero IDE v7.0 Release

There are four scenarios for the initialization of RAM cells in VHDL and Verilog simulations:

1. Actual silicon behavior

   This initialization is unknown. The RAM cells could be powered-up to either '1' or '0'.
2. Simulation without the meminit.dat file

   The contents of the RAM cells remain unknown until the first write to memory.
3. Simulation using the default meminit.dat file

   Memory arrays are initialized to a default value of '0' according to the default meminit.dat file.
4. Simulation employing a user-defined initialization file

   Memory arrays are initialized to user-specified values according to the user-defined initialization file.

In the Libero IDE v7.0 release, Actel has implemented the last scenario. The SmartGen tool generates multiple memory initialization files (ram_int_<RAM block number>.mem) for all the RAM blocks that a particular RAM configuration uses. The files are created with all zeros. You need to modify these files with the desired initialization values ('1' or '0').

Memory Initialization File

For both VHDL and Verilog simulations, ensure that the SmartGen generated memory initialization files in the current simulation directory. The memory initialization files can be copied to the simulation directory from the SmartGen project directory.

To initialize memory cells to user specified values, open each memory initialization file and enter the value as desired and save it. Note: SmartGen creates all the memory initialization files as memory arrays are initialized to a default value of '0'.

Design Example

This design example illustrates the initialization of RAM cells for VHDL and Verilog simulations. The design cascades two basic RAM blocks (size 256x9) generated using SmartGen core generator to create a 10x10 memory configuration with parity bits.

Memory Initialization Files for Design Example

As illustrated in Figure 1, this design has two basic RAM blocks: the M0 RAM block has eight data bits and one parity bit referenced, while the M1 RAM block has two data bits and one parity bit referenced.

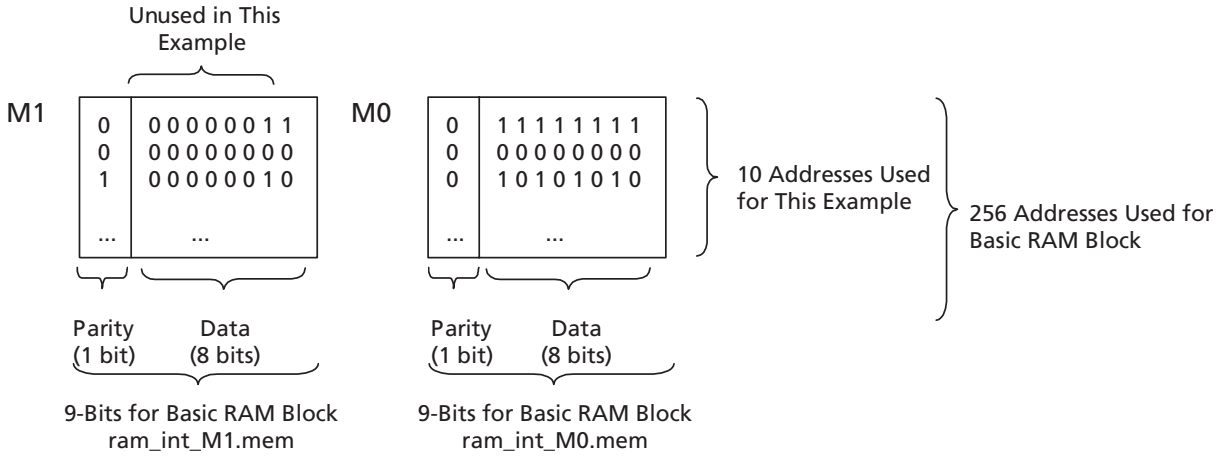

Figure 1 • **Design Example**

From the structural netlist, it can be seen how the RAM data and parity bits are mapped to each basic RAM block. It can also be determined how to set up the initialization file for each RAM block. Note that a separate initialization file is required for each basic RAM block.

M0 is initialized with the user-defined ram_int_M0.mem initialization file, and M1 is initialized with the user-defined ram_int_M1.mem initialization file.

Note: The parity bit, if it exists, corresponds to the most significant bit at each RAM address.

In this example:

- Instance M0: Parity bit 0 is mapped to DI8, bit 0 is mapped to DI0, and bit 1 is mapped to DI1.
- Instance M1: Parity bit1 is mapped to DI8, bit 8 is mapped to DI0, and bit 9 is mapped to DI1.

For example:

To initialize address 0 of a 10x10 memory block to '1111111111', parity bit 0 is '0' and parity bit 1 is '0' (check even parity configuration).

To initialize address 3 of a 10x10 memory block to '1010101010', parity bit 0 is '0' and parity bit 1 is '1' (check even parity configuration).

The following example shows the memory initialization files for the M0 and M1 instances:

M0

```
011111111
000000000
010101010
000000000
000000000
```

M1

```
000000011
000000000
100000010
000000000
000000000
```

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