AC256
Application Note
Power-Up Behavior of ProASICPLUS Devices

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1.1 Introduction

ProASIC^{PLUS}® family FPGAs, built on flash technology, are nonvolatile and live at power-up. They offer a single-chip solution for ASIC-like applications and a reduction of the total system cost of designs. In contrast with SRAM-based FPGA devices, re-programmable ProASIC^{PLUS} FPGAs retain the programmed bit-stream in the absence of power, and thus a device configuration is not required after power-up. Unlike many SRAM FPGAs, ProASIC^{PLUS} devices have no limitation on the power supply ramp rate. This document provides guidelines for ProASIC^{PLUS} power-up and describes the details of different power-up sequence conditions.

1.2 References

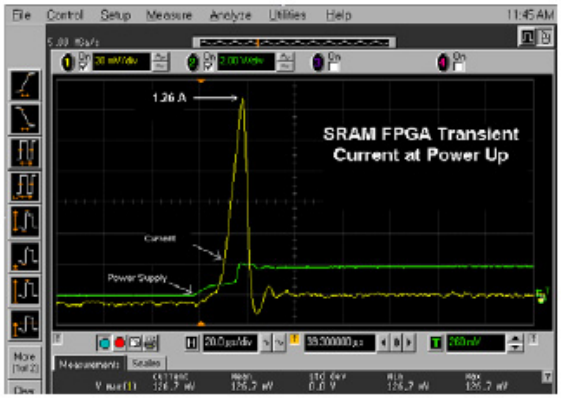
The following document is referred in this application note:
ProASICPLUS Flash Family FPGAs Datasheet

1.3 Transient Current

Depending on the power-up ramp time and the delta between V_{DD} and V_{DDP}, there may be a very small transient current seen on the V_{DD} supply voltage when V_{DD} reaches ~700 mV. Due to the technology inherent in the ProASIC^{PLUS} devices, this transient current is much smaller than the surge current experienced in SRAM-based FPGAs for a given power-up ramp rate. The transient current in the flash-based ProASIC^{PLUS} device is due to the capacitive load seen by the power supply. The nature of this transient current is different from the transient current in SRAM-based devices. In an SRAM-based FPGA, the transient current at power-up is a result of the unconfigured logic array. Since the SRAM-based FPGAs are volatile, they lose their configuration in the absence of power. Therefore, at each power-up the unconfigured SRAM cells need to be reinitialized. As a result, until they are reset, they draw a significant current at power-up, which appears as a transient current. Figure 1, page 2 shows the transient current of a typical SRAM FPGA and ProASIC^{PLUS} FPGA during power-up at similar ramp rates.

The value of the transient current peak in the ProASIC^{PLUS} device depends on the capacitive load (including the decoupling capacitors on the board) seen by the power supply during power-up. Since the board decoupling capacitors need to be charged at the supply power-up, a very fast ramp rate in the presence of large capacitors may result in higher transient current peaks. The current peak would not damage the device or cause reliability issues. The peak of the transient current depends on the power-up ramp rate. The larger the ramp rate (faster power-up) is, the higher the transient current peak becomes. Table 1, page 2 lists the typical transient current peak values measured on nine APA750-BG456 devices from three different lots. Note that these results were obtained under typical temperature conditions. The value of the transient current peak in the ProASIC^{PLUS} device also depends on the delay between V_{DD} and V_{DDP}. Table 2, page 2 provides the guidelines on V_{DD} and V_{DDP} delays to minimize transient power on current.

Figure 1 • **Transient Current Spike of a Typical SRAM Vs ProASIC^{PLUS} FPGAs during Power-Up**



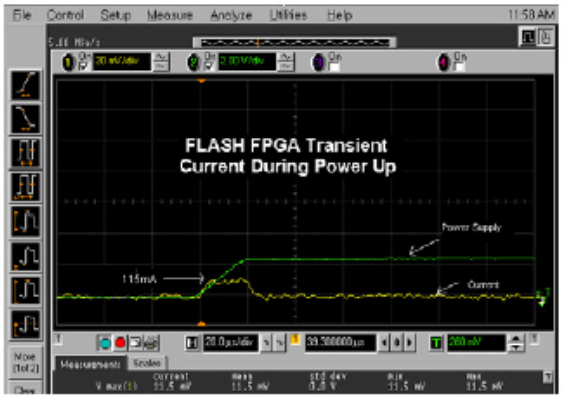


Table 1 • **Typical ProASIC^{PLUS} Transient Current (mA)**

	Power-Up Ramp Time	
Power-Up Sequence	**500 µs**	**>1 ms**
Simultaneous power-up	60-90 mA	60-90 mA
V_{DDP} before V_{DD}	50-90 mA	50-90 mA
V_{DDP} = 3.3 V, V_{DD} = 2.5 V	–	–

Note: The ramp time is 10% to 90% rise time for both power supplies.

Table 2 • **Guidelines To Minimize Transient Current (mA) When V_{DD} before V_{DDP}**

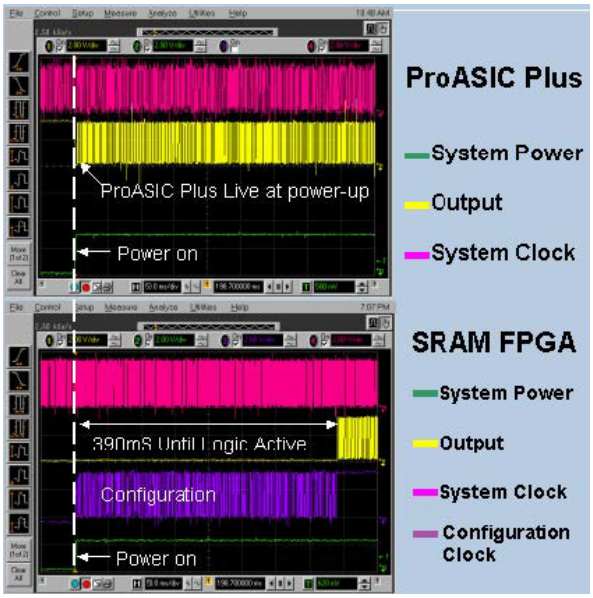
Power On Ramp Rate (V_{DD}/V_{DDP})	**Delay Between V_{DD} and V_{DDP}**	**Delta Between V_{DD} and V_{DDP}**	**Transient Current**
5 µs/V	2 us	400 mV	60-90 mA
10 µs/V	3 us	300 mV	60-90 mA
100 µs/V	50 us	500 mV	60-90 mA
500 µs/V	250 us	500 mV	60-90 mA
1 ms/V	500 us	500 mV	60-90 mA

1.4 Power-Up Behavior

During power-up, V_{DD} and V_{DDP} reach their functional level at around 700 mV and 1 V, respectively. Since the core is functional once V_{DD} reaches 700 mV, the power-up time is defined by the time it takes V_{DD} to reach 700 mV, not by any time after V_{DD} reaches this trip point, making ProASIC^{PLUS} FPGAs live at power-up. Therefore, ProASIC^{PLUS} FPGAs are live at power-up. Figure 2, page 3 shows the functionality of a ProASIC^{PLUS} and a typical SRAM FPGA at power-up.

One of the important board level characteristics of the device during power-up is the I/O state and behavior, while the power supplies are ramping up toward their normal values.

Figure 2 • **Functionality of the ProASIC^{PLUS} and a Typical SRAM FPGA at Power-Up**



1.4.1 Output Behavior

Due to the architecture of the device, the configuration of an I/O (Flash switch) is controlled by V_{DD}, while the external driver circuit level is powered by V_{DDP}. The power-up to functional time of an output is determined by both V_{DD} and V_{DDP}.The following table describes of the output behavior during different states of power-up with different sequences.

Table 3 • **Output Behavior with Different Power-Up Sequences**

Power-Up Sequence	Output Behaviors
V_{DD} first – V_{DDP} second	Before power-up of V_{DDP} and due to the internal architecture of the device, V_{DDP} is pulled up to a diode drop below V_{DD}. The output drive stage (powered by V_{DDP}) is powered, but it is not fully on. As a result the output drives an intermediate voltage level until the V_{DDP} power supply is powered on and the output is fully functional.
V_{DDP} first – V_{DD} second	When V_{DDP} is powered up first, the output will drive to an unknown state (1 or 0) until V_{DD} reaches its functional level and the correct logic is propagated to the output.

1.4.2 Input Behavior

The configuration of the I/O cells is powered by V_{DD} while their output/input buffer stages are powered by V_{DDP}. Therefore, the input's behavior during power-up depends on the power-up sequence. The following table explains the input behavior during power-up.

Table 4 • **Input Behavior With Different Power-Up Sequences**

Power-Up Sequence	Output Behaviors
V_{DD} first – V_{DDP} second	When V_{DD} powers up first, I/Os designed as inputs are configured as inputs throughout the entire power-up. However, no logic passes into the core until V_{DDP} is powered-up. Note that in this case, V_{DDP} is pulled up to a diode drop below V_{DD} before it is powered-up.
V_{DDP} first – V_{DD} second	Since the V_{DD} supply is not powered up, the configuration of the I/Os is undefined and the drive stage of the I/O is powered by V_{DDP}. Therefore, the I/O may drive an unknown logic state until the V_{DD} line is powered up. Once the core voltage is at its functional level, the I/O is configured as an input and functions as expected. In this case the input may behave as an unknown output while V_{DD} is not powered-up; it may cause conflicts if a device driving the ProASIC^{PLUS} input is driving the pin. Microsemi recommends powering-up V_{DD} before V_{DDP}. In the Power-Up Solutions, page 6, some techniques are offered for a safe power-up of the device. Unless care is taken, exposure to this mode may cause damage to the ProASIC^{PLUS} input or the driving device output.

1.5 JTAG Configuration for Proper Power-Up

During power-up of ProASIC^{PLUS} FPGAs, the power-on device circuitry detects an increase in the power supply voltages and sends a reset signal to the JTAG circuitry. This forces JTAG into the TEST-LOGIC-RESET state. It is important that the power supplies ramp up cleanly, free from glitches, steps, and residual voltage in order for this reset signal to be generated properly. As specified in the *ProASICPLUS Flash Family FPGAs datasheet* (refer to the Pin Description section), Microsemi recommends adding a nominal 20 kΩ pull-up resistor to the TCK pin. This helps to prevent false edges on the TCK pin due to noise during power-up; this may cause an inadvertent state change of the JTAG state machine. If JTAG is not in TEST-LOGIC-RESET state at power-up, the I/Os may be initialized to an unknown state.

Microsemi recommends the following options, Option 1 and Option 2 or Option 3 for systems that may have FPGA power supplies with residual voltage, glitches, or voltage steps during power-up. The use of any one of these recommendations will ensure the JTAG TAP controller of the device always powers up in the TESTLOGIC-RESET state.

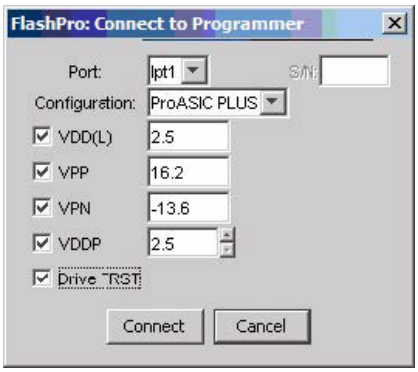
1.5.1 Option 1

Connect the TRST pin to ground. This will asynchronously hold the JTAG TAP controller in a TEST-LOGICRESET state. Use this option only if you are not planning to employ JTAG circuitry in the future. With TRST held at ground, in-system programming (ISP) of the device is disabled. By using a jumper setting on the board, you can release TRST from ground, enabling ISP as needed.

1.5.2 Option 2

If you plan to use the JTAG circuitry, perform remote ISP of the device, or where the use of a jumper is not possible, Microsemi recommends connecting the TRST pin to ground through a 1 kΩ resistor. This will hold the JTAG TAP controller in TEST-LOGIC-RESET state without disabling the JTAG or programming capability. If you are programming the device with FlashPro or FlashPro Lite, select **Drive TRST** when connecting the programmer to drive the TRST pin to logic '1' (Figure 3, page 5). When using a microprocessor for ISP, you may also opt to drive the TRST pin from a microprocessor or microcontroller port to enable ISP when the controller drives the TRST pin to logic '1.

Figure 3 • **Drive TRST to '1' from FlashPro or FlashPro Lite**



1.5.3 Option 3

After the initial power-up of the device, hold the TMS '1' while applying at least five clock cycles on the TCK pin. This will force the JTAG TAP controller into a TEST-LOGIC-RESET state. For additional information related to JTAG reset circuitry and commands, refer to the Boundary-Scan Test IEEE Std. 1149.1 (JTAG) specification.

1.6 Applying Signals to Inputs Prior to Full Power-Up

In some applications, signals are applied to the device inputs before or during device power-up. In general, the ProASIC^{PLUS} devices do not support or guarantee “cold-sparing” applications. However, Microsemi has performed tests to examine the behavior of the inputs in these cases. The results show that if the V_{DDP} voltage plane is NOT grounded before power-up, signals can be applied to a limited number of inputs with no damage or long-term reliability issues.

If V_{DDP} is not powered and not grounded (floating), depending on the status of V_{DD}, the following may occur if the inputs are driven by a 3.3 V signal:

- If V_{DD} is powered to 2.5 V, the input draws approximately 10 mA and V_{DDP} is pulled up to 2.1 V. This causes no damage to the device. The amount of current may vary from design to design.
- If V_{DD} is not powered, the input draws approximately 50 mA. At this state, V_{DDP} and V_{DD} are pulled up to 2.5 V and 0.9 V, respectively. Even though the input voltage pulls up the power supplies and partially powers up the device, this does not cause any damage, since the I/O is configured as the input. Care must be taken concerning the number of inputs driven before power-up.

If the V_{DDP} is powered up and V_{DD} is not yet powered, the input may drive to an unknown state since the configuration of the I/O is not yet defined. Unless care is taken, contention of the printed circuit board (PCB) may occur. Exposure to this mode may cause damage to the ProASIC^{PLUS} input or the driving device output. Furthermore, when V_{DDP} is grounded, it is not safe to apply any signals to the inputs of the FPGA before or during power-up.

1.7 Power-Down Behavior

The behavior of ProASIC^{PLUS} devices during power-down is very similar to the power-up behavior. Just as in power-up, the I/O configuration is dependent on the core voltage (V_{DD}). ProASIC^{PLUS} chips may be powered down with both voltage dropping together or with V_{DD} first or V_{DDP} first. However, if V_{DD} power is removed before V_{DDP} the data inputs and outputs may drive an unknown logic state (as described in Table 3, page 3).

1.8 Power-Up Solutions

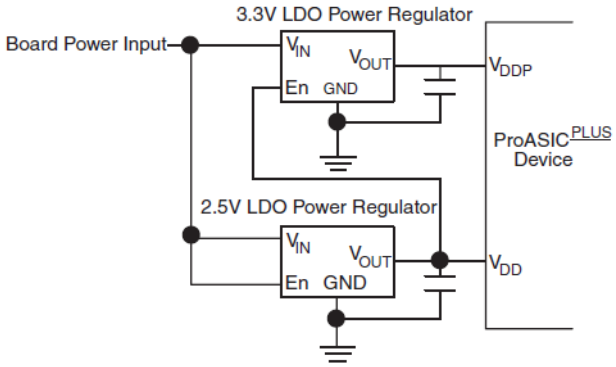
As discussed in the Power-Up Behavior, page 2, Microsemi recommends powering up the core voltage supply (V_{DD}) before the I/O power supply (V_{DDP}). In this section, some suggestions are made as guidelines to enable you to design a cost-effective, safe, and efficient power-up system for your board. There are several other solutions, such as power sequencers and dual-output switching regulators, but their implementation is not unique to the target device, so discussion of these solutions is outside of the scope of this application note. However, power sequencers can provide very accurate results and should be considered in applications that allow for their use.

Low Drop Out (LDO) power regulators often contain an enable functionality, which allows you to perform power-up sequencing very easily. As an example, if the designer needs to power-up the core voltage (2.5 V) before (3.3 V) supply, this can be done easily using LDO regulators and without the need for additional components. The LDO regulators offer additional advantages, such as LDO voltage during power-up or normal operation if a fast transient current response is required. Figure 4, page 6 shows two five-pin LDO regulators (with active high enable input) connected together in such a way that the 3.3 V I/O supply powers-up after the 2.5 V core voltage.

The 3.3 V regulator is enabled once the 2.5 V regulator output is powered-up. Therefore, the V_{DDP} voltage comes up after V_{DD}.

For designs that demand it, DC-DC converters can be used as power management systems to control the power-up sequence and ramp rate. The DC-DC converters offer designers a variety of options to control and manage the system power in different conditions.

Figure 4 • **Using LDO Power Regulators for Power Sequencing**



1.9 Conclusion

The ProASIC^{PLUS} devices are nonvolatile and live at power-up. These devices do not require any specific ramp rate to power-up, and they draw low transient current during power-up. The different power-up sequences will not potentially damage the device; however, the I/Os of the FPGA behave differently in different power-up sequences. As a result, Microsemi recommends designers to power-up V_{DDP} (I/O power supply) simultaneously or after the V_{DD} (core voltage supply). Microsemi offers a variety of solutions for different design budgets to help you manage the power-up procedure.

2 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

2.1 Revision 4.0

Revision 4.0 of the document has non-technical updates.

2.2 Revision 3.0

The Power-Up Solutions, page 6 is updated in the revision 3.0 of the document.

2.3 Revision 2.0

A new section, JTAG Configuration for Proper Power-Up, page 4 is added in revision 2.0 of the document.

2.4 Revision 1.0

The following list of changes are implemented in the revision 1.0 of the document:

- The Transient Current, page 1 is updated.
- The Table 1, page 2 is updated.
- The Table 2, page 2 is newly added.

2.5 Revision 0

A new section, Power-Down Behavior, page 5 is added in the revision 0 of the document.