Implementing Global Reset for ProASIC^PLUS® In-System Programming Applications

Background

Actel ProASIC^PLUS devices provide designers with in-system programming (ISP) capability. During ISP, the FPGA can be programmed while mounted on the board and powered on. While the FPGA is being programmed in-system, the device I/Os are held at tristate mode along with an internal weak pull-up on each I/O. When programming is completed, the device enters normal operation mode and I/Os switch to their operating state as defined by users in the programmed design (e.g., input, output, etc.). After the I/Os are activated at the end of programming, the inputs will take some time (per user's design), as illustrated in Figure 1, to propagate the right logic into corresponding outputs. Therefore, there will be a time interval (equivalent to the propagation delay) after the activation of the I/Os in which the output may drive to an unknown logic (1 or 0). The same behavior may occur on bidirectional I/Os, which can lead to unwanted bus contentions if there is more than one driver on the bus. Hence, for some applications, it is crucial for I/Os to be in a known state at the end of programming, when the FPGA returns to normal operation.

This document provides a solution that, if implemented in the user's design, leaves the FPGA I/Os in a known state at the end of ISP before returning to normal operation mode.

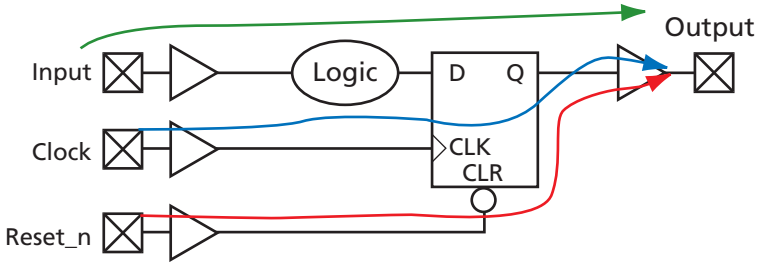

Figure 1 • **Simple Synchronous Input to Output Path**

Implementation

When using FlashPro or FlashPro Lite for in-system programming of ProASIC^PLUS FPGAs, there is a short period of time at the end of the programming cycle when the FPGA core is in normal operation mode but I/Os have not been yet released into normal operation mode. During this time, the programmer still drives the TCK with clock pulses. Since the FPGA core is functional, these additional TCK pulses can be used to implement a reset/initialization circuitry in the design.

When using an external microprocessor to perform ISP, the JTAG pins are usually directly mapped into the processor's memory space. It is trivial to add few clock cycles or any other instructions at the end of programming cycle. The purpose of these additional clock cycles is to mimic the extra TCK cycles that exist in FlashPro / FlashPro Lite programming.

The additional clock cycles at TCK input can be transferred into the core using the UJTAG macro in ProASIC^PLUS devices. The UJTAG macro is an Actel macro that can be instantiated in the user's design to access the core from the JTAG pins when the FPGA core is in normal operation mode. For more information on UJTAG and its usage, refer to the *How to Use UJTAG* application note.

Assuming that the final state of TCK at the programming cycle is logic high, Figure 2 illustrates a simple implementation of a global reset at the end of ISP before I/Os become functional.

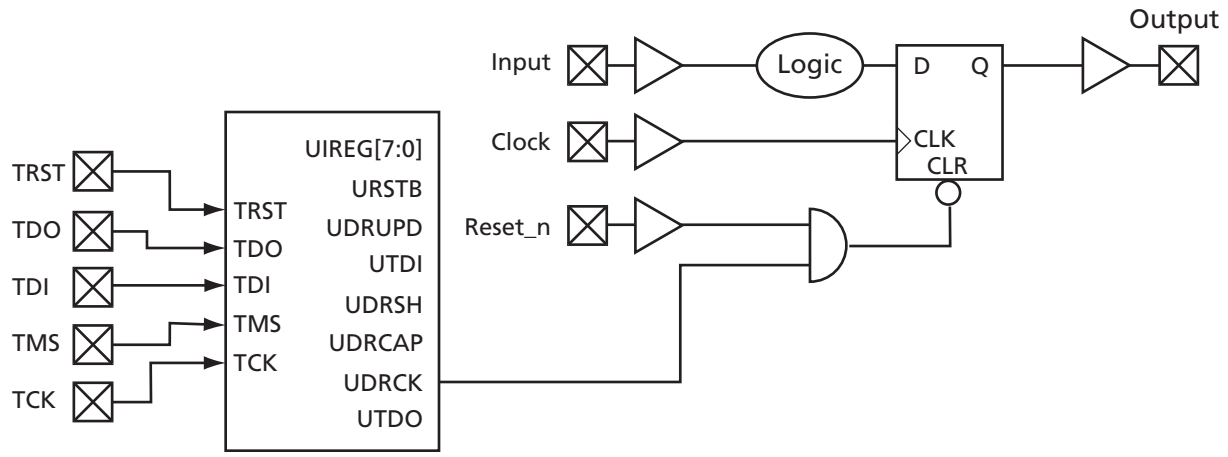

Figure 2 • **Simple Implementation of ISP Reset**

In Figure 2, the additional pulses of TCK while the core is functional will reset the design register, which in turn will place logic '0' at the input of the output buffer. Therefore, at the end of the programming cycle when the I/Os become functional, the output will begin by driving '0'.

Similarly, the initial value of the output can be set to 1, or in case of a bidirectional I/O, it can be initially set to be input, output driving 1, or output driving 0.

Conclusion

In many applications, ProASIC^PLUS FPGAs are programmed using various ISP methodologies. In some of these applications, it is important for the FPGA I/Os to be in a known logic state once the FPGA exits the programming mode and enters normal operation. This document described a simple implementation in which UTAG macro is used to create internal reset/preset signals after the end of programming and before the start of normal operation.

Related Documents

Application Notes

How to Use UJTAG

http://www.actel.com/documents/Flash_UJTAG_AN.pdf

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