Interfacing ProASIC^PLUS® FPGAs with 5V Input Signals

Introduction

The ProASIC^PLUS device family was designed to operate with a maximum input voltage of 3.3V. To meet the requirement for up to 5.5V input voltage, an external component must be added to each I/O pad to limit the input voltage to a maximum of 3.3V. In addition, the voltage on the I/O must be equal to or less than the V_{DDP} supply to the device. These voltage limitations are required to ensure device reliability. Discrete components reduce the input current and affect slew rates on the input signals provided. This application note describes two circuits that provide sufficient attenuation to prevent damage to the input structures of the ProASIC^PLUS device.

Background

Actel recommends two types of attenuation networks (Voltage Divider or Zener Diode), depending on the customer's requirements for speed and cost.

The design shown in Figure 1 was used for the evaluation.

One recommended circuit is a voltage divider network on the input of the device (Figure 2). This example circuit steps down a 1 MHz clock input from 5.5V to 3.3V. The resultant waveform is shown in Figure 3 on page 2.

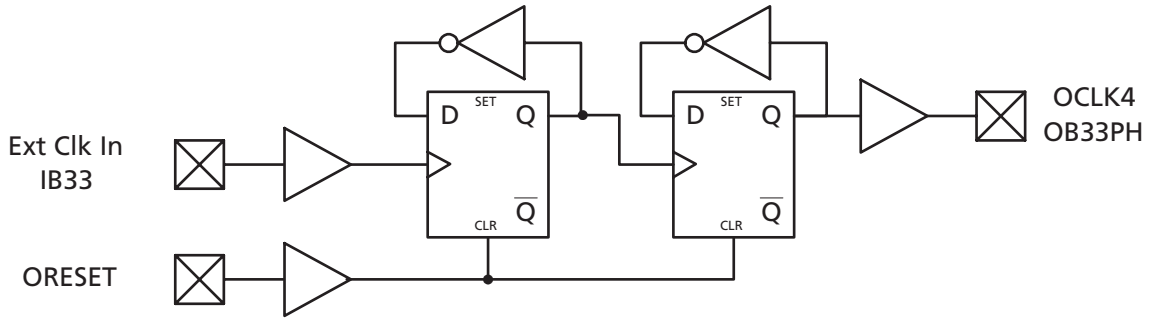

Figure 1 • **Schematic of Design Used to Evaluate Various High Voltage Input Schemes**

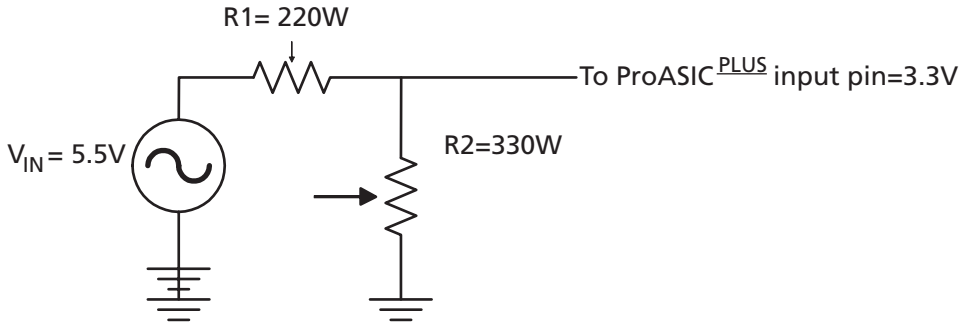

Figure 2 • **Schematic of Resistor Divide Network**

A second recommended circuit is a 3.3V Zener diode with a series resistor of 240Ω on the input of the device, as shown in Figure 4. The resultant waveform in Figure 5 uses a 1 MHz stimulus.

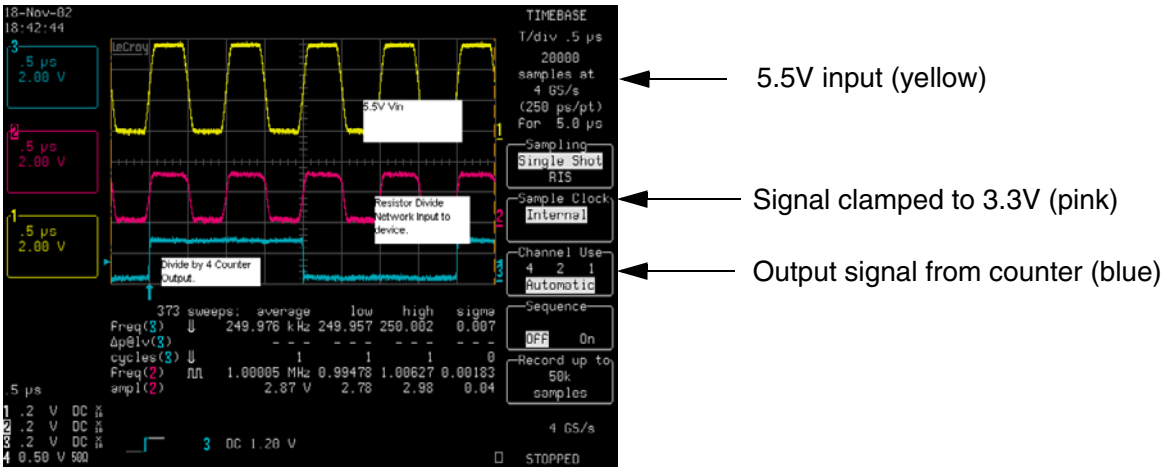

Figure 3 • **Resultant Waveforms of Resistor Divide Network**

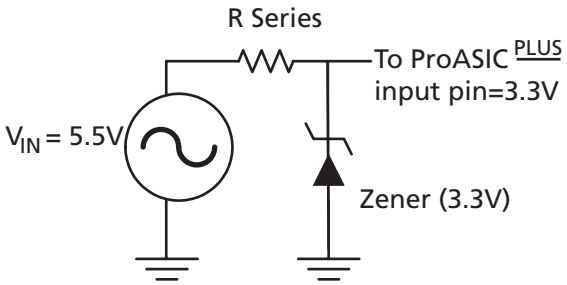

Figure 4 • **Zener Diode Circuit**

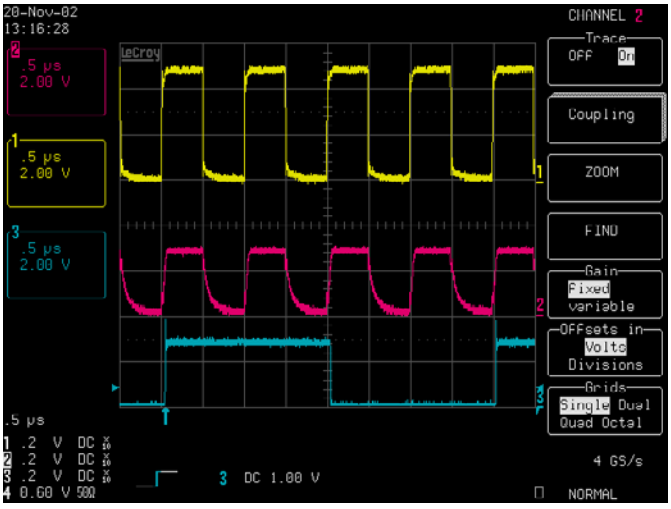

Figure 5 • **Resultant Waveforms of Zener Diode Circuit with 250Ω Series Resistor**

Resistor circuit variations are not recommended due to the reflections and attenuations induced on the input of the signal that drive the ProASIC^PLUS device. Figure 6 on page 3 shows a 50Ω resistor being used with the circuit shown in Figure 4 on page 2. The waveform shows no attenuation on the input or change in the slew rate. However, there is reflection being induced directly onto the 5.5V input source.

If the design does not require a fast slew rate, a larger value resistor may be used. Figure 7 on page 3 depicts the input to the device with a 500Ω series resistor being used with the circuit shown in Figure 4 on page 2. The waveform shows one volt of attenuation on the input and a significantly slower slew rate, especially on the failing edge.

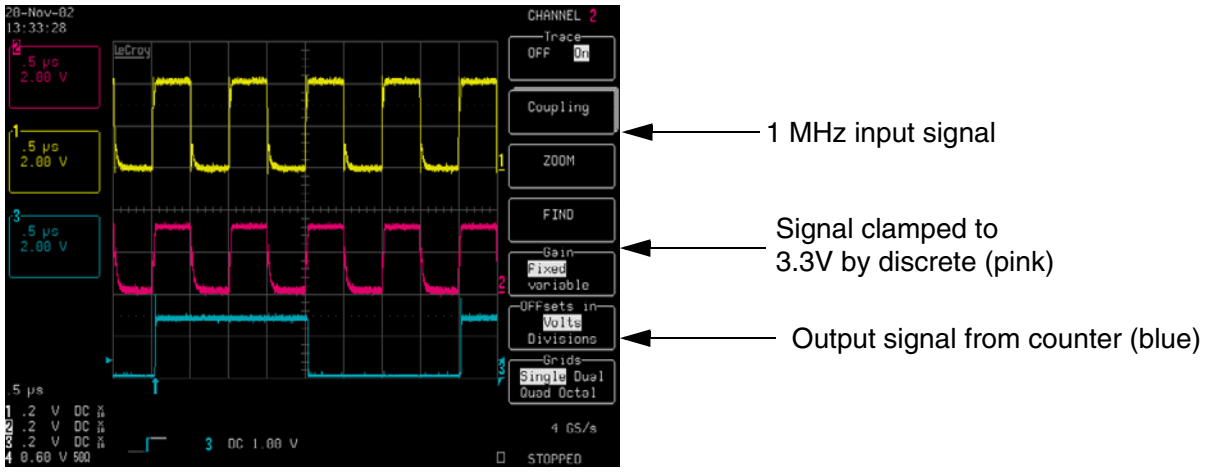

Figure 6 • **Resultant Waveforms of Zener Diode Circuit with 50Ω Series Resistor**

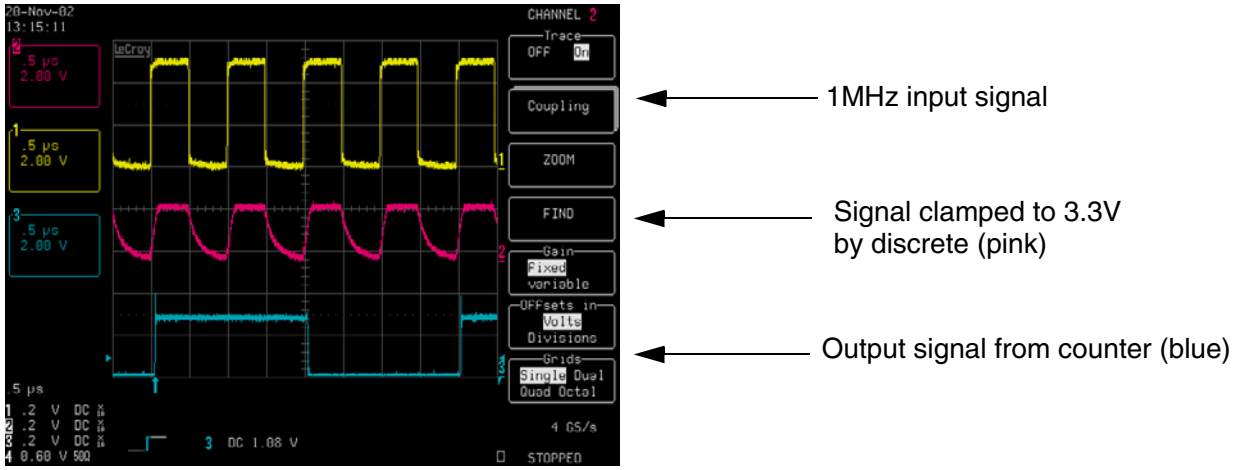

Figure 7 • **Resultant Waveforms of Zener Diode Circuit with 500Ω Series Resistor**

Recommendations

When choosing resistance values, customers should keep in mind that higher resistance equals lower currents. Higher resistance (and lower currents) severely affect the rise and fall time of the signal. This effect is more apparent as the signal increases in frequency. The Zener diode circuit does not have this constraint with smaller values of series resistance; however, reflection to the input source device may be an issue. For the Zener diode circuit, Actel recommends that customers use at least a 240Ω resistor in series with the Zener diode circuit because of reflections back to the I/O source to maintain device reliability.

Conclusion

Device reliability may be maintained with 5.5V signals as long as the voltage is limited to the *ProASIC^{PLUS} Flash Family FPGAs* datasheet specifications at the device input. In addition, under no circumstances should V_{IO} exceed the V_{DDP} of the device. For this reason, the two schemes described in this application note cannot be replaced with a diode-resistor scheme, which would raise V_{IO} to up to 4.3V. Experiments have shown that as long as the two proposed schemes are used and the input does not exceed 3.6V, the ProASIC^{PLUS} device reliability and functionality will be maintained.

Actel's reliability qualification on the ProASIC^{PLUS} devices was done with a maximum input voltage of 3.6V to the device for 1000 hours duration at 125°C. The foundry for the ProASIC^{PLUS} devices does not ensure gate oxide reliability on the 0.22µm technology used for this device if the input voltage to the device exceeds 3.6V.

Related Documents

Datasheets

ProASIC^{PLUS} Flash Family FPGAs

http://www.actel.com/documents/ProASICPlus_DS.pdf

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (51900023-0/3.04*)	Page
51900023-1/3.04*	The "Conclusion" was updated.	page 4

Note: **This is the part number located on the last page of the document.*

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