Microsemi eX, SX-A, and RTSX-SU I/Os

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Introduction

The eX, SX-A, and RTSX-SU devices have a variety of advanced I/O features, such as Peripheral Component Interconnect (PCI) compliance, programmable input threshold voltage, configurable output slew rate, and selectable output state during power-up. Furthermore, these devices are the first to support both hot-swapping and cold-sparing. This application note provides the guidelines for designing with selectable I/O standards in eX, SX-A and RTSX-SU devices.

I/O Standards Support

Table 1 lists all the supported I/O standards and advanced I/O features for the eX, SX-A, and RTSX-SU device families. The usage of these standards and features is discussed in detail in the "Configuring I/Os with Microsemi Software" section on page 4.

Table 1 • **Summary of Supported I/O Features**

I/O Standard	Device			Output Slew-Rate Control	Power-Up State Control	Hot-Swap	Loading (pf)
	SX-A	eX	RTSX-SU				
2.5 V LVCMOS	X	X		X	X	Yes	35
3.3 V LVTTL	X	X	X	X	X	Yes	35
5 V TTL	X	X	X	X	X	Yes	35
3.3 V PCI	X		X	High*	X	No	10
5 V PCI	X		X	High*	X	Yes	50
5 V CMOS			X	X	X	Yes	35

*Note: *PCI mode sets the output slew rate High by default.*

I/O Power-Up Behavior

Before Power-Up

All I/Os are tristated and therefore no current flows into the device even if a voltage (within allowable specifications) is applied to the I/Os.

During Power-Up

The I/Os of these devices are also tristated during power-up (including partial power-up). The SX-A has a recommended power supply sequence — applying VCCA at the same time or before VCCI. Refer to the I/O Power-Up Behavior section on page 1 of the *Microsemi SX-A and RTSX-SU Devices in Hot-Swap and Cold-Sparing Applications* application note for details. After the I/Os become active, they behave according to your design. Table 2 on page 2 summarizes the times when the I/Os become active during power up for devices at room temperature with various ramp-rates.

The data assumes a linear voltage ramp up to 2.5 V.

Table 2 • **Power-up Time at which I/Os Become Active**

Ramp Rate	0.25 V/µs	0.025 V/µs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Time Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11.0	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5.0	12.1	47.2
RTSX32SU	10	100	0.40	0.70	2.8	5.2	13.0	47.0
RTSX72SU	10	100	0.42	0.68	2.6	4.8	11.0	40.0

Note: Although the eX devices are not included in the above table, A54SX08A data can be used for the eX256 device. Smaller eX devices have not been characterized.

I/O Architectural Features

I/O Configuration

Each user I/O can be configured as an input, an output, a tristate output, or a bidirectional pin. Mixed I/O standards can be set for individual pins, though this is only allowed with standards that use the same supply voltage.

Figure 1 on page 3 shows a simplified diagram of the I/O circuitry. The output enable (OE) signal enables the output buffer to pass the signal from the core logic to the pad. The output buffer contains ESD protection circuitry, which is an N-channel transistor. This transistor shunts all ESD surges (up to the limit of the device ESD specification) to GND. Each I/O also contains programmable slew rate control, programmable power-up state control (pull-up/down resistor), hot insertion, 5 V tolerance, and clamp-diode control circuitry. AF0, AF1, AF2…AF4 are programmable fuse selectors. For example, if you select an I/O power-up state (refer to the "Power-Up State" section on page 5), then the AF2 and AF3 fuses are programmed appropriately to enable weak pull-up in the output pad.

Similarly, AF0 and AF1 are programmed to enable different input trip points (PCI, LVTTL, etc.) that are selected in the I/O attribute section.

Note: When the input trip point is set for 3.3 V PCI (for example, AF0, AF1 are programmed), this also activates a PCI clamp-diode to VCCI.

The SX-A and RTSX-SU inputs should be driven by high-speed push-pull devices with a low-resistance pull-up device. If the input voltage is greater than VCCI and a fast push-pull device is NOT used, the high-resistance pull-up of the driver and the I/O internal circuitry may create a voltage divider. This voltage divider could pull the input voltage below the specification for some devices connected to the driver. Logic '1' may not be correctly presented in this case. For example, if an open-drain driver is used with a pull-up resistor to 5 V to provide a logic '1' input, and VCCI is set to 3.3 V, the input signal may be pulled down by the device's input buffer. Refer to the "Design Practices" section on page 10 for more information.

PCI Compliance (SX-A and RTSX-SU Only)

The SX-A and RTSX-SU devices are 3.3/5 V PCI-compliant. As required for compliance with version 2.1 and later of the PCI specification, the input buffers of these devices have clamping-diodes to ground (Figure 2 on page 4). In addition, to comply with the 3.3 V PCI specification, the 3.3 V PCI I/O includes a clamping-diode to VCCI. (This clamping-diode to VCCI is optional for the PCI 5 V specification and is not included with the 5 V PCI I/O). The clamp-diodes to VCCI in the 3.3 V PCI buffers, while fully compliant with the 'regular' 3.3 V PCI specification, are NOT compliant with the hot-swap provisions of the CompactPCI specifications (www.picmg.org/v2internal/compactpci.htm)

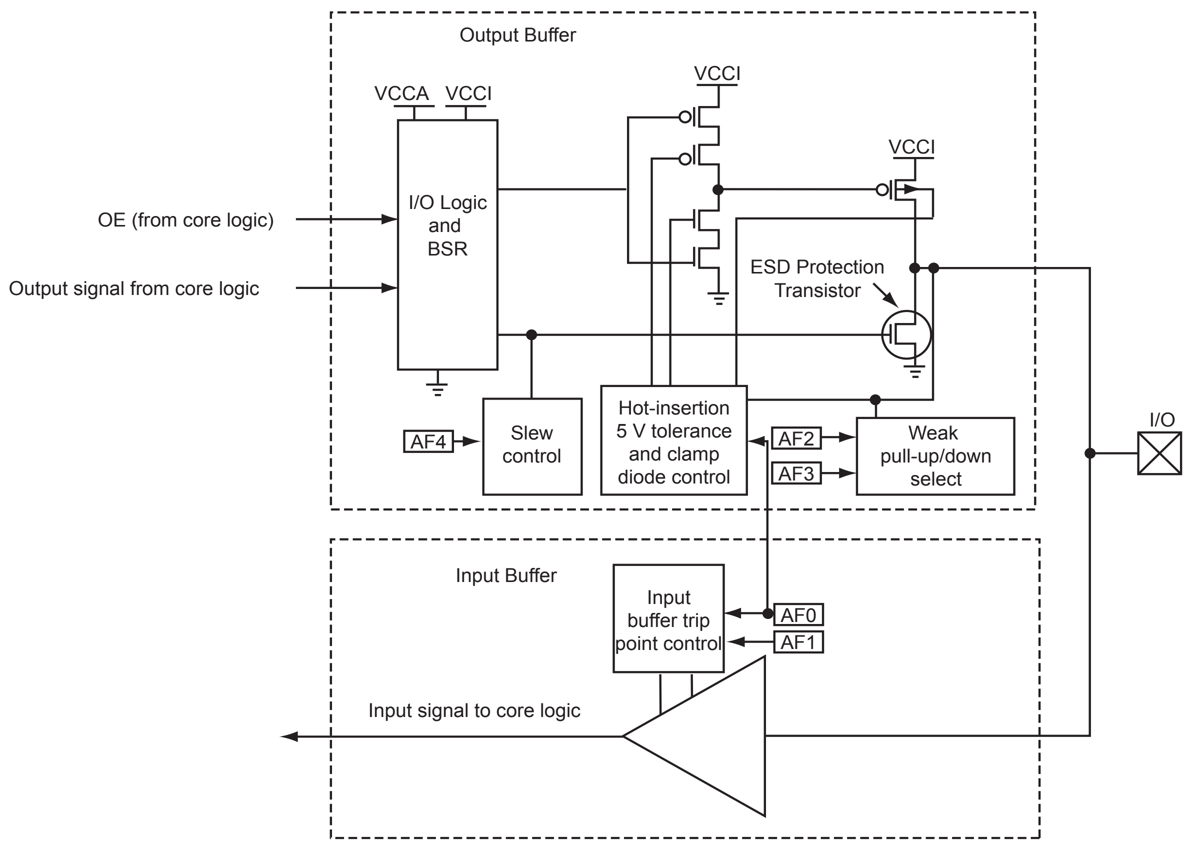

Figure 1 • **Simplified I/O Circuitry**

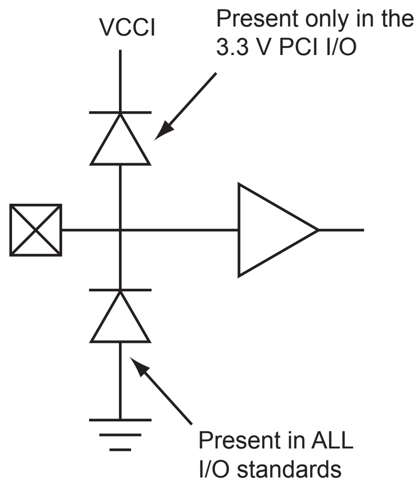

Figure 2 **• 3.3 V PCI I/O**

Configuring I/Os with Microsemi Software

The Designer software's I/O Attribute Editor tool allows you to select different I/O attributes as required by the design. The features available in I/O Attribute Editor are described below.

Port Name

Displays the port name listed in the netlist.

Macrocell

Displays the name of the macro used. Please refer to the *Antifuse Macro Library Guide* for specific details.

Pin Number

Displays the number (or alphanumeric location) of the assigned package pin. If you import a pin file during compilation in the Designer software, the pin assignments will be as given in the pin file. You can also compile the netlist without the pin file and later manually assign pin numbers. If you leave the pin numbers unassigned, then the Designer tool assigns them during place-and-route.

Fixed

Selecting this ensures that the specified pin location will be used during place-and-route. If a pin file is imported during the compilation, this is selected for the pins that are assigned in the file.

I/O Standard

Choosing a standard allows the software to set the I/O threshold, slew rate, hot-swap compliance, and output loading. Possible I/O standards include LVTTL/TTL, PCI, CMOS, and CUSTOM.

CUSTOM

By setting the I/O standard to CUSTOM, you can select additional combinations of I/O attributes. For example, if the I/O standard is set to PCI, the I/O threshold is automatically set to PCI and cannot be set to any other I/O threshold. However, if CUSTOM is selected, the I/O threshold can be set to LVTTL, even though all the other I/O attributes are those of PCI. You can even change the default output loading (pf) value's CUSTOM settings.

I/O Threshold

This selects the input buffer threshold (trip point) according to the chosen I/O standard. Possible I/O thresholds include 5 V PCI/TTL/CMOS, 3.3 V PCI/LVTTL, and 2.5 LVCMOS/LVTTL. Table 3 shows nominal input threshold values for the different I/O standards. The minimum and maximum guaranteed trip points are defined in each device's datasheet.

***Table 3* • Nominal Input Threshold Voltage for Different I/O Standards**

VCCI (Volts)	Input Threshold (Volts)				
	TTL	CMOS	LVTTL	LVCMOS	PCI
5	1.4	2.5	–	–	1.4
3.3	–	–	1.4	1.4	1.32
2.5	–	–	–	1.4	–

Slew

Output slew rate can be set to high or low, but slew control affects only the falling edges. Rising edges are not affected. The PCI I/O standard, which uses only high slew, does not have any slew control. However, if you select the CUSTOM I/O standard, you can choose the PCI I/O threshold and then choose high or low slew. Low-slew rates in 5 V PCI and TTL are identical.

Power-Up State

The state of the I/Os during power-up can be configured as High, Low, or None.

All eX and SX-A devices are equipped with optional pull-up or pull-down resistors of about 50Kohm that are enabled during power-up. These resistors are disabled just before VCCA reaches 2.5 V, and then the I/Os behave according to the design. This configurable I/O state does not eliminate the risk of an I/O driving a temporary unknown state near the end of the power-up sequence when VCCI is powered up before VCCA.

The default value for Power-Up State in the software is 'None'. The only exception to this is an I/O that exists in the netlist as a port, is not connected to the core, and is configured as an Output Buffer. In that case, the default setting is 'Low'.

Hot Swap

This indicates whether or not the pin is hot-swap capable (On or Off). This is linked to the I/O threshold because the same fuse controls both the functions. If hot swap shows 'On', it means that the pull-up clamp-diode is 'Off' (not present). In that condition, inputs are 5 V-tolerant (handle input voltages up to 5.5 V), and the device can be used in cold-sparing applications. Note that with a DC input of 5 V, the device can draw up to 300 uA per pin. Ensure that you disable the clamp-diodes on unused I/Os. Use the Generate Programming Files dialog box as shown in Figure 3.

Hot Swap 'Off' means that the pull-up clamp-diode is 'ON' (present), and this is only applicable if the 3.3 V PCI I/O standard is selected. Inputs are not 5 V-tolerant and only support VCCI + 0.5 V. The device cannot be used for cold-sparing since the pull-up clamp-diode is forward-biased, if a 5 V input is applied.

Loading

Loading determines which Timer is used as the loading on the output pin in question. The default loadings for different I/O standards are as follows:

- 35 pf for TTL, LVTTL, and CMOS
- 50 pf for 5 V PCI
- 10 pf for 3.3 V PCI

Note: These values are for Timer use only. Designers can customize the I/O loading for timing analysis. They do not affect the I/O configuration. Refer to Figure 4 on page 6 for more information.

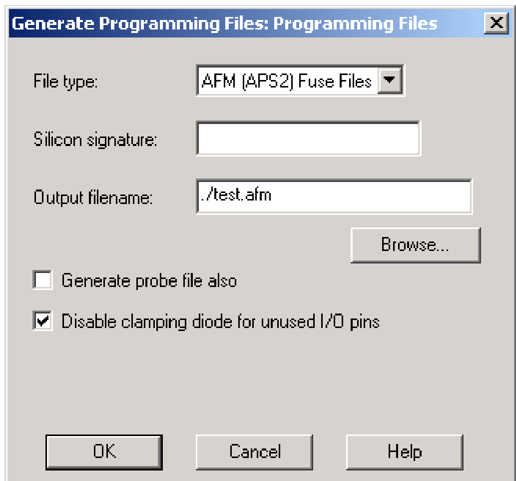

Figure 3 **• Disabling Clamping-Diodes for Unused I/O Pins**

	Port Name	Macro Cell	Pin #	Fixed	I/O Standard	IO Threshold	Slew	Power Up State	Hot Swap	Loading (pf)
1	q2	ADLIB:OUTBUF	58	☑	CUSTOM	PCI	Low	High	Off	35
2	q6	ADLIB:OUTBUF	35	☑	LVTTL	LVTTL	High	Low	On	35
3	q5	ADLIB:OUTBUF	57	☑	LVTTL	LVTTL	Low	None	On	35
4	q0	ADLIB:OUTBUF	24	☐	PCI	PCI	High	None	Off	10
5	q7	ADLIB:OUTBUF	36	☐	LVTTL	LVTTL	High	None	On	35
6	q3	ADLIB:OUTBUF	61	☐	LVTTL	LVTTL	High	None	On	35

Figure 4 **• Snapshot of I/O Attribute Section from the PinEditor Tool**

Drive Capability

The output drive strength depends on the VCCI value. For example, if VCCI is 3.3 V then the maximum output drive will be 3.3 V. Table 4 lists the available power supply, maximum input tolerance, and maximum output drive combinations for SX-A, eX, and RTSX-SU devices.

Table 4 • **Power Supplies**

VCCI (VCCA= 2.5 V)	Device			Maximum Input Tolerance[2]	Maximum Output Drive[2]
	SX-A	eX	RTSX-SU		
2.5 V	✓	✓		5.5 V	2.5 V
3.3 V	✓	✓	✓	5.5 V[1]	3.3 V
5.0 V	✓	✓	✓	5.5 V	5.0 V

Notes:

1. *3.3 V PCI mode is not 5.0 V- tolerant due to the clamp diode, but instead it is 3.3 V tolerant.*
2. *Check the datasheet of the device family for the maximum input tolerance and maximum output drive.*

All I/Os have sufficient current drive capabilities to meet the logic levels defined in JEDEC specifications. Microsemi®system-on-chip (SoC) Products Group provides IBIS models for these devices. Source and sink currents can be calculated from these models. Also, any IBIS editor (for example, the Hyperlynx Visual IBIS editor) can be used to generate I/V curves from these models. The values are taken from a sample group of devices under specific operating conditions. Not all models were generated from lab measurement; some of them are from SPICE simulation — check the header of each file. IBIS values are NOT guaranteed for every device under worst-case conditions.

Note that these models should not be used to determine total current drive capability of a device. They only give an AC estimate of source and sink currents on a per-I/O basis. For example, the source current of an SX-A device with 3.3 V LVTTL, high slew is 64mA (from the I/V curve in Figure 5), which means 64mA can be supplied through one output for a short period of time. This is NOT the same as the source/sink (IOH/IOL) current values stated in the datasheet.

In addition, the device cannot necessarily supply the same amount of current through multiple I/Os simultaneously. This is due to the power dissipation limit of the device's package. Refer to the 'Package Thermal Characteristics' section of each datasheet for the maximum power dissipation of each package and electromigration considerations.

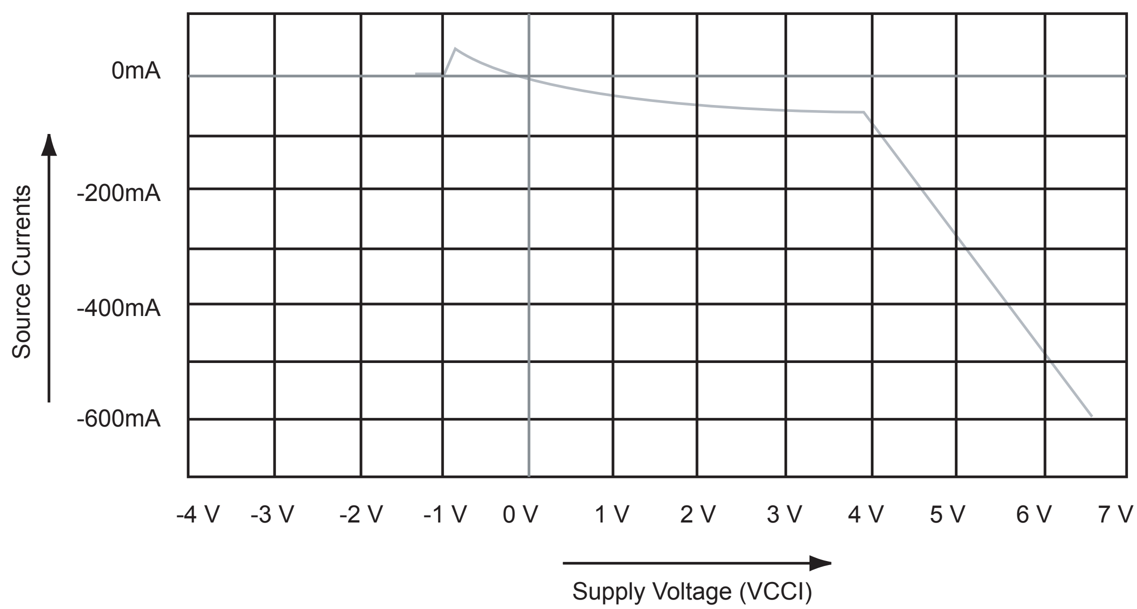

Figure 5 **• SX-A 3.3 V LVTTL I/O I/V Curve**

Sometimes outputs may be tied together externally to increase the drive capability, provided the device does not exceed the maximum allowable power dissipation as well as the IOH/IOL specification in the datasheet. Although this is a relatively common design practice, FPGA designers must be diligent in their timing analysis to ensure that the delays from the common source to the multiple output pins are as closely matched as possible to avoid contention in the outputs. This may require manual placement of the driving source cells and the I/O cells.

Unused I/Os and Clocks

In SX-A, RTSX-SU, and eX devices, each unused I/O is configured as a TRIBUF with the enable permanently tied to GND (disabled) by Microsemi's Designer software (Figure 6).

Microsemi recommends tying unused pins to ground.

Driving unused I/Os is acceptable if the driving signal is below the level of input tolerance (Table 4 on page 7). For SX-A/RTSX-SU, if the clamping-diode is disabled in the Designer software (refer to Figure 2 on page 4), the unused I/Os are 5 V-tolerant; otherwise, the unused I/Os are only tolerant to VCCI.

If the JTAG pins are not reserved in the design (Figure 7 on page 9), the unused JTAG pins behave as normal unused I/Os. Hence, you should follow the above recommendation. If the JTAG pins are reserved, then these pins are dedicated test pins. The JTAG pins are also 5 V-tolerant if the clamping-diodes are disabled in the Designer software

For RTSX72SU and A54SX72A, CLKA/B and the QCLKA/B/C/D pins are Clock-I/O pins that can be configured as clock and/or user I/O. When these pins are not used, they should be tied to 'High' or 'Low' on the board. For all other eX, SX-A, and RTSX-SU devices, the CLKA/B pins are clock-only pins (not clock-I/Os). The unused CLKA/B and HCLK pins must NOT be left floating.

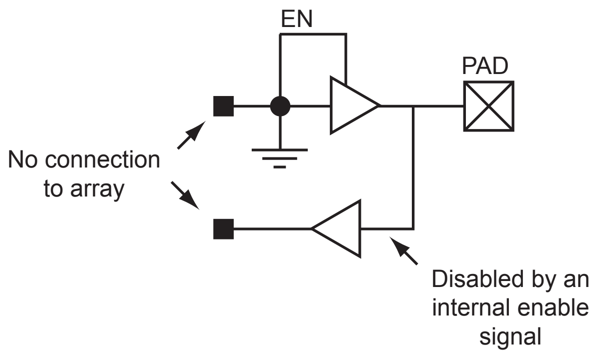

Figure 6 **• Unused I/O Configuration**

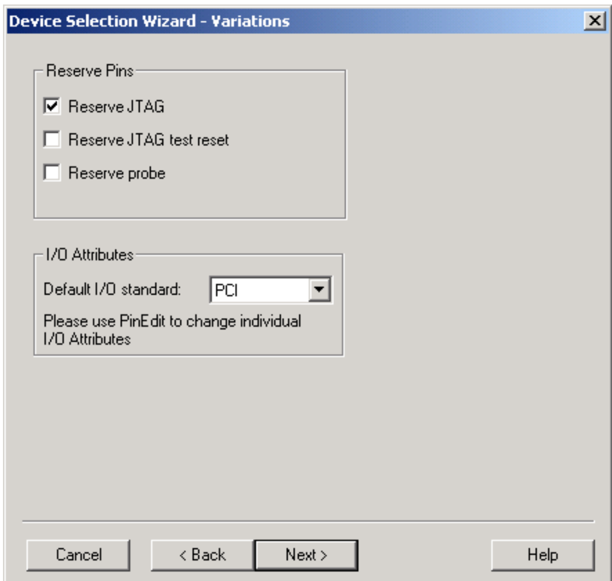

Figure 7 **• Reserving JTAG Pins in Designer Software**

Floating Input Behavior

Microsemi does not recommend floating input pins (including clock pins). Any floating input can cause the input buffer to go into an unpredictable state. It can float to an intermediate state where both transistors of the input buffer may turn on and current may flow from VCCI to ground. Microsemi strongly recommends that any unused input pins should be terminated in a known state on the board.

Design Practices

Achieving 5 V Drive with 3.3 V VCCI

To configure a Microsemi SX-A or RTSX-SU device to drive 5 V with VCCI=3.3 V, you can utilize an Open Drain configuration of the I/O cell with an array inverter cell and an external pull-up resistor to 5 V. The recommended configuration is illustrated in Figure 8 on page 10. The I/O configuration must be set to LVTTL to disable the PCI clamp-diode. For the recommended resistor value in a specific application, please contact Microsemi Technical Support.

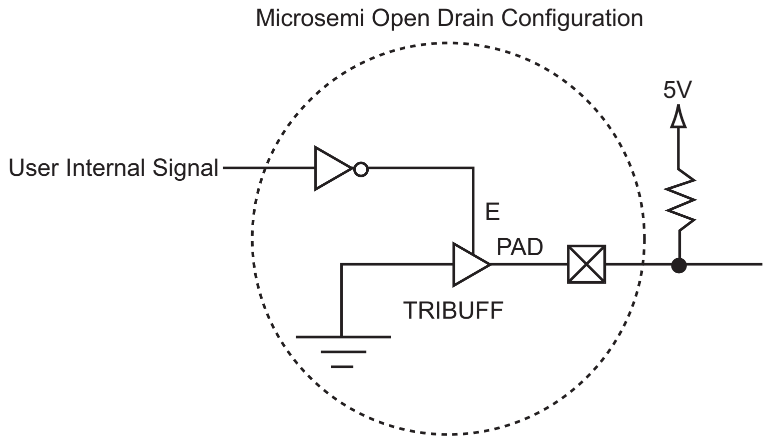

Figure 8 **• Open-Drain Configuration for SX-A or RTSX-SU**

Input Signal Rise and Fall Times Exceeding the Maximum Specified Values

Input signals must meet the input transition time (tR, tF) requirements given in the datasheet. If an input signal is too slow, then noise around the FPGA's input threshold can cause multiple transitions.

During the transition time, both input buffer transistors could potentially turn on at the same time. This could result in unpredictable input buffer oscillations. In this situation, the input buffer could still pass signals. However, these short, unpredictable oscillations would likely cause the device to malfunction. One way to eliminate problems with slow input signals is with external Schmitt triggers. The Schmitt trigger is a buffer used to convert a slow or noisy signal into a clean one before passing it to the FPGA. This is a simple, low-cost solution when working with slow input signals. Refer to the *Using Schmitt Triggers for Low Slew-Rate Input* application note for details.

TRST Pin for RTSX-SU in Space Application

The TRST pin is a dedicated reset pin for RTSX-SU and therefore you should reserve this pin (Figure 9) in a prototype design using SX-A.

In final production with RTSX-SU for space applications, this pin must be hardwired to the ground.

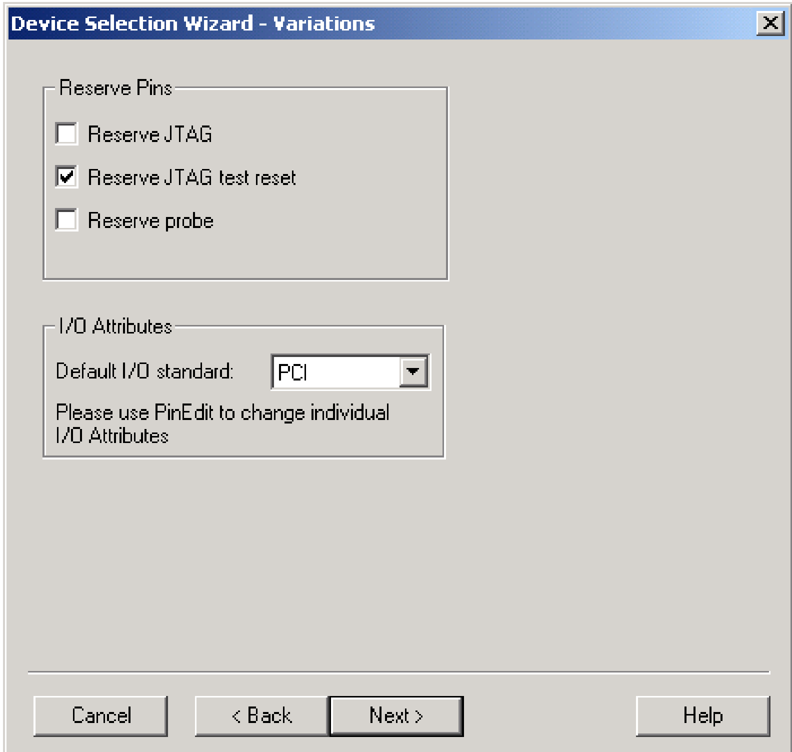

Figure 9 • **Reserving TRST Pin in Designer Software**

Conclusion

Microsemi eX, SX-A, and RTSX-SU devices support a variety of advanced I/O features for commercial and aerospace applications. To take advantage of these features, follow the recommendations described in this document and consult the "Related Documents" section for more information.

Related Documents

Application Notes

Microsemi SX-A and RTSX-SU Devices in Hot-Swap and Cold-Sparing Applications

Using Schmitt Triggers for Low Slew-Rate Input

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision*	Changes	Page
Revision 3 (April 2012)	The "Configuring I/Os with Microsemi Software" section was revised (SAR 35813).	4
	Table 4 was removed (SAR 35813).	
Revision 1 (July 2002)	The "I/O Power-Up Behavior" section is new.	2
	The "I/O Architectural Features" section is new.	2
	The "Configuring I/Os with Microsemi Software" section is new.	4
	The "Drive Capability" section is new.	7
	Table 4 was updated.	
	The "Unused I/Os and Clocks" section is new.	8
	Figure 5 was updated.	8

*Note: *This is the part number located on the last page of the document.*

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