I/O Cell Selection for ProASIC™ 500K Devices

Introduction

The ProASIC 500K family offers a variety of different I/O cells to meet specific application requirements. These I/O cells can be configured with a 3.3V or 2.5V I/O ring supply voltage. In addition, every pad except output pads can be configured with or without a pull-up. Output pads also offer different drive strengths and slew rates, increasing flexibility for different applications.[1] This Application Note describes the available I/O cells to help designers select the best cell to meet their requirements.

Input Pads

The selection of an input pad is determined by the I/O ring voltage and the voltage of the incoming signals. All input pads are capable of receiving CMOS and TTL level signals. In addition, each input can be configured individually with or without a pull-up. There is a separate library cell for each of these configurations.

If the I/O ring is powered at 3.3V, the I/Os can receive either 3.3V or 2.5V signals. If the I/O ring is powered at 2.5V, the I/Os can only receive 2.5V (low power) signals. The suffix LP has been added to the 2.5V power supply I/Os to enable ASICmaster™, the backend tool, to check whether a netlist contains both 3.3V and 2.5V I/O cells. Figure 1 shows input pad cells for 3.3V and 2.5V I/O ring supply voltages. Available input pads are shown in Table 1.

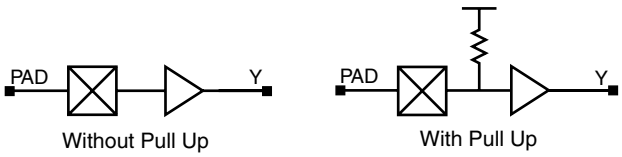

Figure 1 • 3.3V/2.5V Input Pad Cells

Table 1 • Input Pads

	Signal Voltage 3.3V	Signal Voltage 2.5V
Without Pull-Up		
3.3V I/O Ring	IB33	IB25
2.5V I/O Ring	N/A	IB25LP
With Pull-Up		
3.3V I/O Ring	IB33U	IB25U
2.5V I/O Ring	N/A	IB25LPU

Global Input Pads

To place an input signal on one of the four global input pins, a global input pad should be used. Three types of global input pads are available, normal global, multiplexed global, and global input pads for internal signals.

Normal global input pads put a signal directly on the global network. Figure 2 shows global input pad cells for 3.3V and 2.5V I/O ring supply voltages. Table 2 lists available normal global pad cells.

Figure 2 • 3.3V/2.5V Global Input Pad Cells

Table 2 • Normal Global Input Pads

	Signal Voltage 3.3V	Signal Voltage 2.5V
Without Pull-Up		
3.3V I/O Ring	GL33	GL25
2.5V I/O Ring	N/A	GL25LP
With Pull-Up		
3.3V I/O Ring	GL33U	GL25U
2.5V I/O Ring	N/A	GL25LPU

1. Unused pads are automatically configured as IB33U or IB25LPU, depending on the I/O ring supply voltage.

Multiplexed global input pads enable the designer to multiplex an external input signal or an internal signal to the global network. Figure 3 shows multiplexed global input pad cells for 3.3V and 2.5V I/O rings.

Table 3 lists multiplexed global pads with positive enables. Table 4 lists multiplexed global pads with negative enables.

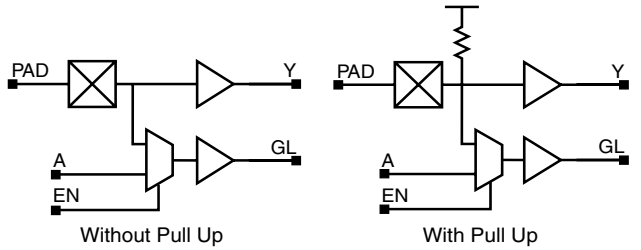

Figure 3 • 3.3V/2.5V Multiplexed Global Input Pad Cells

Table 3 • Multiplexed Global Input Pads with Positive Enable

	Signal Voltage 3.3V	Signal Voltage 2.5V
Without Pull-Up		
3.3V I/O Ring	GLMIB33	GLMIB25
2.5V I/O Ring	N/A	GLMIB25LP
With Pull-Up		
3.3V I/O Ring	GLMIB33U	GLMIB25U
2.5V I/O Ring	N/A	GLMIB25LPU

Table 4 • Multiplexed Global Input Pads with Negative Enable

	Signal Voltage 3.3V	Signal Voltage 2.5V
Without Pull-Up		
3.3V I/O Ring	GLMIBL33	GLMIBL25
2.5V I/O Ring	N/A	GLMIBL25LP
With Pull-Up		
3.3V I/O Ring	GLMIBL33U	GLMIBL25U
2.5V I/O Ring	N/A	GLMIBL25LPU

Another variety of global pads, global input pads for internal signals, can connect an external input signal to a normal routing resource while connecting an internal signal to the global routing resource. These cells are needed if a pin is constrained to place a signal on a global pin location of the chip. This signal would normally be routed to the global routing resource whether it is a clock signal or not. With the use of the GLIB input pads, the signal is routed to normal routing resources and another clock signal can be connected to the global routing resource from within the chip. Figure 4 shows these global pads for 3.3V and 2.5V I/O ring supply voltages. Table 5 lists the available global input pads for internal signals.

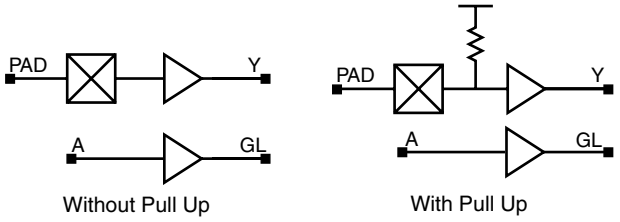

Figure 4 • 3.3V/2.5V Global Input Pad Cells for Internal Signals

Table 5 • Global Input Pads for Internal Signals

	Signal Voltage 3.3V	Signal Voltage 2.5V
Without Pull-Up		
3.3V I/O Ring	GLIB33	GLIB25
2.5V I/O Ring	N/A	GLIB25LP
With Pull-Up		
3.3V I/O Ring	GLIB33U	GLIB25U
2.5V I/O Ring	N/A	GLIB25LPU

Output Pads

As with input pads, the selection of output pads depends on the voltage of the I/O ring as well as the voltage at which the signals have to be driven. The output pads do not have pull up resistors, but they offer three slew rates and two drive strengths. The three available slew rates are high (H), normal (N), and low (L), where H is 100mA/s, N is 50mA/s and L is 25mA/s. This slew rate applies to both rising and falling edges. The strong and weak drivers for each voltage setup are identified with H for high and L for low. The exception to this rule is the high driver strength setup for 3.3V signals. This driver is compliant with the PCI Specification Revision 2.2 and is referenced with the letter P for PCI.

The output pads can also be tristated. Tristated output pads have a positive or negative active select signal that enables the driver. The user can select slew rate and driver strength of each pad regardless of whether or not it is tristated. Figure 5 shows output pads without tristates for 3.3V and 2.5V I/O ring supply voltages. Figure 6 shows output pads with tristates for 3.3V and 2.5V I/O rings. Table 6 and Table 7 show the combinations of output pads without tristate and Table 8 and Table 9 show the possible combinations of pads with tristate.

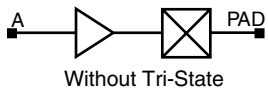

Figure 5 • *3.3V/2.5V Output Pad Cells without Tristate*

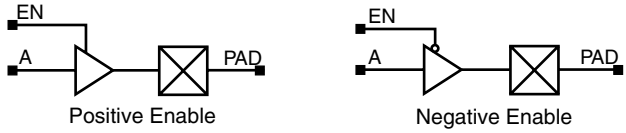

Figure 6 • *3.3V/2.5V Output Pads with Tristate*

Table 6 • *Output Pads without Tristate for 2.5V I/O Ring Power Supply*

	Signal Voltage 2.5V	
	High Drive	**Low Drive**
High Slew Rate	OB25LPHH	OB25LPLH
Normal Slew Rate	OB25LPHN	OB25LPLN
Low Slew Rate	OB25LPHL	OB25LPLL

Table 7 • *Output Pads without Tristate for 3.3V I/O Ring Power Supply*

	Signal Voltage 3.3V		Signal Voltage 2.5V	
	PCI Drive	**Low Drive**	**High Drive**	**Low Drive**
High Slew Rate	OB33PH	OB33LH	OB25HH	OB25LH
Normal Slew Rate	OB33PN	OB33LN	OB25HN	OB25LN
Low Slew Rate	OB33PL	OB33LL	OB25HL	OB25LL

Table 8 • *Output Pads with High Active Enabled Tristate for 3.3V I/O Ring Power Supply*

	Signal Voltage 3.3V		Signal Voltage 2.5V	
	PCI Drive	**Low Drive**	**High Drive**	**Low Drive**
High Active Enable				
High Slew Rate	OTB33PH	OTB33LH	OTB25HH	OTB25LH
Normal Slew Rate	OTB33PN	OTB33LN	OTB25HN	OTB25LN
Low Slew Rate	OTB33PL	OTB33LL	OTB25HL	OTB25LL
Low Active Enable				
High Slew Rate	OTBL33PH	OTBL33LH	OTBL25HH	OTBL25LH
Normal Slew Rate	OTBL33PN	OTBL33LN	OTBL25HN	OTBL25LN
Low Slew Rate	OTBL33PL	OTBL33LL	OTBL25HL	OTBL25LL

Table 9 • Output Pads with High Active Enabled Tristate for 2.5V I/O Ring Power Supply

	Signal Voltage 2.5V	
	High Drive	**Low Drive**
High Active Enable		
High Slew Rate	OTB25LPHH	OTB25LPLH
Normal Slew Rate	OTB25LPHN	OTB25LPLN
Low Slew Rate	OTB25LPHL	OTB25LPLL
Low Active Enable		
High Slew Rate	OTBL25LPHH	OTBL25LPLH
Normal Slew Rate	OTBL25LPHN	OTBL25LPLN
Low Slew Rate	OTBL25LPHL	OTBL25LPLL

Bidirectional Pads

Bidirectional pads offer designers the most variety. These pads incorporate all the features of the input and output pads into a single pad.

Figure 7 shows bidirectional pads with positive tristate enable for 3.3V and 2.5V I/O rings. Table 10 lists bidirectional pads with high active enable and 3.3V I/O ring supply.

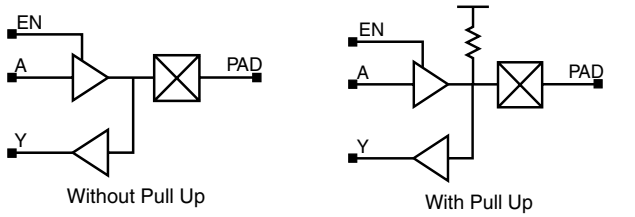

Figure 7 • 3.3V/2.5V Bidirectional Pads with Positive Tristate Enable

Table 10 • Bidirectional Pads with High Active Enabled Tristate for 3.3V I/O Ring Power Supply

	Signal Voltage 3.3V		Signal Voltage 2.5V	
	PCI Drive	**Low Drive**	**High Drive**	**Low Drive**
Without Pull-Up				
High Slew Rate	IOB33PH	IOB33LH	IOB25HH	IOB25LH
Normal Slew Rate	IOB33PN	IOB33LN	IOB25HN	IOB25LN
Low Slew Rate	IOB33PL	IOB33LL	IOB25HL	IOB25LL
With Pull-Up				
High Slew Rate	IOB33PHU	IOB33LHU	IOB25HHU	IOB25LHU
Normal Slew Rate	IOB33PNU	IOB33LNU	IOB25HNU	IOB25LNU
Low Slew Rate	IOB33PLU	IOB33LLU	IOB25HLU	IOB25LLU

Figure 8 shows bidirectional pads with low active enable for 3.3V and 2.5V I/O rings. The bidirectional pads with negative enable and 3.3V I/O ring power supply are listed in Table 11. Table 12 lists the bidirectional pads for 2.5V I/O ring power supply.

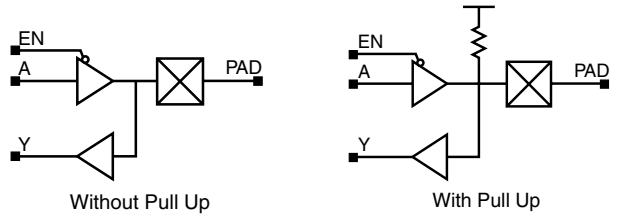

Figure 8 • *3.3V/2.5V Bidirectional Pads with Negative Tristate Enable*

Table 11 • *Bidirectional Pads with Low Active Enabled Tristate for 3.3V I/O Ring Power Supply*

	Signal Voltage 3.3V		**Signal Voltage 2.5V**	
	PCI Drive	**Low Drive**	**High Drive**	**LowDrive**
Without Pull-Up				
High Slew Rate	IOBL33PH	IOBL33LH	IOBL25HH	IOBL25LH
Normal Slew Rate	IOBL33PN	IOBL33LN	IOBL25HN	IOBL25LN
Low Slew Rate	IOBL33PL	IOBL33LL	IOBL25HL	IOBL25LL
With Pull-Up				
High Slew Rate	IOBL33PHU	IOBL33LHU	IOBL25HHU	IOBL25LHU
Normal Slew Rate	IOBL33PNU	IOBL33LNU	IOBL25HNU	IOBL25LNU
Low Slew Rate	IOBL33PLU	IOBL33LLU	IOBL25HLU	IOBL25LLU

Table 12 • *Bidirectional Pads for 2.5V I/O Ring Power Supply*[a]

	High Active Enable		**Low Active Enable**	
	High Drive	**Low Drive**	**High Drive**	**Low Drive**
Without Pull-Up				
High Slew Rate	IOB25LPHH	IOB25LPLH	IOBL25LPHH	IOBL25LPLH
Normal Slew Rate	IOB25LPHN	IOB25LPLN	IOBL25LPHN	IOBL25LPLN
Low Slew Rate	IOB25LPHL	IOB25LPLL	IOBL25LPHL	IOBL25LPLL
With Pull-Up				
High Slew Rate	IOB25LPHHU	IOB25LPLHU	IOBL25LPHHU	IOBL25LPLHU
Normal Slew Rate	IOB25LPHNU	IOB25LPLNU	IOBL25LPHNU	IOBL25LPLNU
Low Slew Rate	IOB25LPHLU	IOB25LPLLU	IOBL25LPHLU	IOBL25LPLLU

a. References: *ProASIC Macro Library Guide*

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