ProASIC® to ProASIC^PLUS® Design Migration

Introduction

The ProASIC^PLUS family of FPGAs with FlashLock® combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC^PLUS family offers a clock conditioning circuit based on 2 on-board phase-locked loops (PLLs). The family offers up to 1 million system gates while providing up to 198 kbits of 2-port SRAM and up to 712 user I/Os. All devices allow 50 MHz PCI performance.

Although architecturally related to the earlier ProASIC family, there are enhancements over ProASIC that should be considered when migrating designs to ProASIC^PLUS. This application note is intended to help designers take advantage of these enhancements.

Design Migration

There are restrictions and specific requirements to consider when migrating designs from ProASIC to ProASIC^PLUS. In addition, the design migration process is affected if the device is being converted to a higher density device. The following is a summary of the restrictions and specific requirements that need to be considered when moving a design from ProASIC to ProASIC^PLUS:

- "Logic Tiles and Memory"
- "Advanced Features in ProASICPLUS"
- "Power Supply and Board-Level Considerations"
- "Package Compatibility"
- "Timing Differences"
- "Design Flow"
- "Programming"

Logic Tiles and Memory

The ProASIC^PLUS family offers seven devices versus the ProASIC family's four. During migration from ProASIC to ProASIC^PLUS, it is necessary to move either up or down in size between ProASIC and ProASIC^PLUS. The basic logic tile structure is the same for the ProASIC and ProASIC^PLUS families, so the logic tile usage is identical. Based on logic tiles, Table 1 on page 2 list the number of logic tiles available in the two families.

ProASIC^PLUS devices also have more memory than ProASIC devices (hence the higher system gate count values in the part names for ProASIC^PLUS). Like all of the ProASIC family, the APA075 and APA150 devices only have memory on the north side of the chip. The other ProASIC^PLUS devices have memory on both the north and south sides of the device. Table 2 on page 2 list the embedded memory available in the two families.

Based on logic tiles alone, logical migration paths would be from the A500K050 to the APA150, from the A500K130 to the APA450, from the A500K180 to the APA600, and from the A500K270 to the APA750 devices.

Table 1 • **Number of Logic Tiles in the ProASIC^{PLUS} and ProASIC Families**

ProASIC^{PLUS}							
Device	**APA075**	**APA150**	**APA300**	**APA450**	**APA600**	**APA750**	**APA1000**
Logic Tiles	3,072	6,144	8,192	12,288	21,504	32,768	56,320
ProASIC							
Device		**A500K050**		**A500K130**	**A500K180**	**A500K270**	
Logic Tiles		5,376		12,800	18,432	26,880	

Table 2 • **Memory in the ProASIC^{PLUS} and ProASIC Families**

ProASIC^{PLUS}							
Device	**APA075**	**APA150**	**APA300**	**APA450**	**APA600**	**APA750**	**APA1000**
RAM Bits	27 k	36 k	72 k	108 k	126 k	144 k	198 k
RAM Blocks	12	16	32	48	56	64	88
ProASIC							
Device		**A500K050**		**A500K130**	**A500K180**	**A500K270**	
RAM Bits		14 k		45 k	54 k	63 k	
RAM Blocks		6		20	24	28	

Advanced Features in ProASIC^{PLUS}

The ProASIC^{PLUS} family has improved clock support and uses a smaller process technology than the ProASIC family. In addition, ProASIC^{PLUS} offers more advanced I/O features. Some of these features are explained below:

1. Advanced I/O Features in ProASIC^{PLUS}

   As with the ProASIC family, each pad can be configured as an input, an output, a tristate driver, or a bidirectional buffer. All the pads have a built-in configurable Schmitt Trigger input. ProASIC^{PLUS} devices have AVDD and AGND pins on the east and west sides to power the PLL block.

   ProASIC^{PLUS} devices have LVPECL input pads as special high speed differential inputs on the east and west sides of the device. The PECL input pad cell, unlike the standard I/O cell, is operated from V_{DD} only (not V_{DDP}) and exclusively used as an input. Please see the Actel *ProASIC^{PLUS} Flash FPGA Family* datasheet for details.

2. Advanced Global Networks in ProASIC^{PLUS}

   ProASIC^{PLUS} devices provide designers with very flexible clocking capabilities. The east and west sides of the chip each contain a clock conditioning circuit based on a 240 MHz phase-locked loop (PLL) block. Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side. The PLL is configured during programming and can be reconfigured during operation if desired.

Both the ProASIC and the ProASIC^{PLUS} families have four global networks. Any internal net or any external input can drive these global networks. ProASIC^{PLUS} also allows the global lines to be driven by the PECL input pads, or outputs from the PLL block, or both. For more information about this, refer to the Actel *Using ProASIC^{PLUS} Clock Conditioning Circuits* application note.

Power Supply and Board-Level Considerations

ProASIC^{PLUS} devices require 2.5 V for the core voltage and either 3.3 V or 2.5 V for I/Os, which is similar to the requirement for ProASIC devices. However, the internal power supply circuit has been modified in the ProASIC^{PLUS} family. During normal operation of both ProASIC and ProASIC^{PLUS} devices, the V_{PP} pin (programming supply pin) can have a voltage from 0 V to 16.5 V or be left floating (there is an internal pull up on this pin). Similarly, the V_{PN} pin (programming supply pin) in either family can have a voltage from –13.8 V to 0 V or be left floating (there is an internal pull down on this pin). However, for ProASIC devices, these two pins must not be floated. Table 3 shows the power supply requirements for the board.

Table 3 • **Power Supply Requirements for ProASIC and ProASIC^{PLUS} Families**

Power Supply	ProASIC	ProASIC^{PLUS}
V_{DDL}/V_{DD}	2.5 V	2.5 V
V_{DDP}	2.5 V ± 0.2 V or 3.3 V ± 0.3 V	2.5 V ± 0.2 V or 3.3 V ± 0.3 V
V_{PP} (Normal Operation)	V_{DDP}	0 V to 16.5 V or floating
V_{PN} (Normal Operation)	0	–13.8 V to 0 V or floating
V_{PP} (During Programming	15.9 V < V_{PP} < 16.5 V	15.9 V < V_{PP} < 16.5 V
V_{PN} (During Programming)	–13.8 V < V_{PN} < –13.0 V	–13.8 V < V_{PN} < –13.0 V
AVDD	N/A	V_{DD}
AGND	N/A	0V

Package Compatibility

Both ProASIC and ProASIC^{PLUS} have a number of packages available. Table 4 on page 4 displays the package availability for both families. ProASIC^{PLUS} devices do not have a BG272 package, whereas ProASIC devices do not have TQ100, FG484, FG896, or FG1152 packages.

Some of the package pins are not compatible between the two families. The PECL pads are specifically designed for global networks. These pins are placed closer to the global multiplexer/PLL, so the position of the GL (global) pads has been modified. This results in some of the I/O pins in ProASIC devices becoming special pins in ProASIC^{PLUS}. In addition, to have more available I/Os, some of the NC (No Connect) pins in ProASIC devices are I/Os in the ProASIC^{PLUS} family. In general, the NC pins in ProASIC^{PLUS} devices are subsets of the ProASIC NC pins. Since global pins are bidirectional in ProASIC^{PLUS} devices, the user can assign a regular ProASIC I/O pin to the GL (Global) pins. However, other pins need to be modified. Table 5 on page 4 lists the pins that are incompatible between the ProASIC and the ProASIC^{PLUS} design. Study Table 5 on page 4 carefully if converting a design from a ProASIC device to a ProASIC^{PLUS} device in the same package.

Table 4 • **Pin Assignments in ProASIC and ProASIC^PLUS Devices**

Packages	ProASIC Devices	ProASIC^PLUS Devices
TQFP100	N/A	APA075, APA150
PQFP208	A500K050, A500K130, A500K180, A500K270	APA075, APA150, APA300, APA450, APA600, APA750, APA1000
PBGA272	A500K050, A500K130	N/A
PBGA456	A500K130, A500K180, A500K270	APA150, APA300, APA450, APA600, APA750, APA1000
FBGA144	A500K050, A500K130	APA075, APA150, APA300, APA450
FBGA256	A500K130, A500K180, A500K270	APA150, APA300, APA450, APA600
FBGA484	N/A	APA450, APA600
FBGA676	A500K270	APA600, APA750
FBGA896	N/A	APA750, APA1000
FBGA1152	N/A	APA1000

Note: *Package Definitions*
TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

Table 5 • **Pin Differences between ProASIC and ProASIC^PLUS**

Pin Number	ProASIC Device Pin Type	ProASIC^PLUS Device Pin Type
PQ208		
24	I/O	GL
25	GL	AGND
26	GL	NPECL
27	I/O	AVDD
28	I/O	PPECL (I/P)
30	I/O	GL
128	I/O	GL
129	I/O	PPECL (I/P)
131	I/O	AVDD
132	I/O	NPECL
133	GL	AGND
FG144		
H2	I/O	NPECL
H4	I/O	AGND
H14	I/O	NPECL
H15	I/O	AGND
J2	I/O	PPECL (I/P)
J3	I/O	AVDD
J13	I/O	PPECL (I/P)
J15	I/O	AGND

Note: **The A500K130-BG456 device has many NC and I/O pins, which are incompatible with other devices. Please check the* ProASIC 500K Family *and the* ProASIC^PLUS Flash Family FPGAs datasheets *for those pins.*

Table 5 • **Pin Differences between ProASIC and ProASIC^PLUS (Continued)**

Pin Number	ProASIC Device Pin Type	ProASIC^PLUS Device Pin Type
FG256		
H2	I/O	NPECL
H4	I/O	AGND
H14	I/O	NPECL
H15	I/O	AGND
J2	I/O	PPECL (I/P)
J3	I/O	AVDD
J13	I/O	PPECL (I/P)
J15	I/O	AVDD
FG676		
G10	NC	I/O
G12	NC	I/O
G14	NC	I/O
G16	NC	I/O
G18	NC	I/O
K7	NC	I/O
K20	NC	I/O
N2	I/O	AGND
N5	I/O	NPECL
N24	I/O	NPECL
P2	I/O	AVDD
P5	I/O	PPECL (I/P)
P20	NC	I/O
P24	I/O	PPECL (I/P)
P25	I/O	AVDD
P26	I/O	AGND
V7	NC	I/O
V20	NC	I/O
Y10	NC	I/O
Y12	NC	I/O
Y14	NC	I/O
BG456		
N3	I/O	AGND
N4	I/O	PPECL (I/P)
N5	I/O	AVDD
N22	I/O	NPECL
N24	I/O	AVDD
N26	I/O	AGND
P5	I/O	NPECL
P26	I/O	PPECL (I/P)

Note: **The A500K130-BG456 device has many NC and I/O pins, which are incompatible with other devices. Please check the* ProASIC 500K Family *and the* ProASIC^PLUS Flash Family FPGAs datasheets *for those pins.*

Timing Differences

ProASIC and ProASIC^PLUS are fabricated on different process technologies and have different device geometries. Although functionality is the same after the conversion of a design, the user should verify that the faster timing and revised place-and-route of ProASIC^PLUS do not cause timing errors. ProASIC^PLUS I/Os are faster than their ProASIC counterparts. This will generally give smaller input-to-data and clock-to-output delays. Users should check the input/output buffer delays as well as the input-to-clock and clock-to-out delays. In addition, the external setup and hold times should be recalculated using the SmartTime tool after successful layout to ensure that no timing violations have been introduced. Table 6 shows the input buffer delays in worst-case commercial conditions.

Please check the *ProASIC 500K Family* and *ProASIC^PLUS FPGA Family* datasheets for more detailed timing information.

Table 6 • **Input Buffer Delays**
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DD} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Macro Type	Description	ProASIC		ProASIC^PLUS		Units
		Max. t_{INYH}	Max. t_{INYL}	Max. t_{INYH}	Max. t_{INYL}	
IB25	2.5V, CMOS Input Levels, No Pull-up Resistor	2.2	0.7	0.5	0.8	ns
IB25LP	2.5V, CMOS Input Levels, Low Power	2.2	1.4	1.1	0.7	ns
IB33	3.3V, CMOS Input Levels, No Pull-up Resistor	1.9	1.0	0.9	0.6	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y HIGH*
2. *t_{INYL} = Input Pad-to-Y LOW*

Design Flow

Generally, the Actel Designer software requires four key steps. These steps are Compile, Layout, Fuse, and Back-Annotate. During the conversion process from ProASIC to ProASIC^PLUS, all of the steps must be redone. There are two possible design flows when migrating from the ProASIC to the ProASIC^PLUS family:

1. The user does not care about the macro placement of the old design.
2. The user wants to keep the placement of the old design. This is mainly required if some floor-planning is already completed, and the optimal relative placement of blocks is to be retained.

Migration from ProASIC to ProASIC^PLUS without Keeping the Old Placement

1. Import the **edn/edif/vhdl/verilog** netlist file into the Designer.
2. Import the pin **or.gcf** file into the Designer software. Note that all the pins are not compatible. Refer to the "Package Compatibility" section on page 3 and modify your file accordingly. If you do not want to use the old pin location, ignore this step.
3. Run **Compile** and **Layout**.

Migration from ProASIC to ProASIC^PLUS Keeping the Old Placement

1. Import the **edn/edif/vhdl/verilog** netlist file into the Designer software.
2. In order to keep old placement, import the **last_placement.gcf** file. This file contains pin information as well as placement information. As mentioned earlier, all pins are not compatible. Please check the "Package Compatibility" section on page 3 and modify your file accordingly.

3. Regarding logic placement, you may or may not have to modify the location based on the family. If you want to migrate to APA150 or APA075, you do not have to modify the logic placement; the first logic tile location is (1,1). However, for other ProASIC^PLUS family devices, the first logic tile location is (1,5) because of the RAM blocks. If you want to keep the old placement, you must modify your old locations from (x,y) to (x,y+4). Open the lastplacement.gcf file in Microsoft® Excel and then modify the coordinates can accomplish this. Also, in order to fix the location, edit the last_placement.gcf file and change all “set_initial_” constraints to “set_” constraints. (A global change from "set_initial_" to "set_" will do this quickly). Import the modified GCF file.
4. Run Compile and Layout again.

RAM Placement

ProASIC^PLUS devices have RAM in both the north and south sides of the device (except the APA075 and APA150), whereas ProASIC only has RAM on the north side of the device. Designer software will automatically place the RAM. During automatic placement, Designer software may place the RAM on the south side instead of the north side. If you want keep placement similar that used in the ProASIC device, modify the memplmt.gcf file. Table 7 shows the locations of memory cells in ProASIC and ProASIC^PLUS devices. This should help modify the manual memory placement.

Table 7 • **Memory Locations for ProASIC and ProASIC^PLUS Families**

Part	Possible RAM locations	Formula
A500K050	(1,57), (17, 57), ..., (81, 57)	x = 16*n+1; n= {0,1,2,3,4,5}; y = 57;
A500K130	(1,81), (17, 81), ..., (145,81) (1,89), (17, 89), ..., (145,89)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9} y = {81, 89}
A500K180	(1,97), (17,97), ..., (177, 97) (1,105), (17,105), ..., (177, 105)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9,10,11} y = {97, 105}
A500K270	(1,121), (17,121), ..., (209,121) (1,129), (17,129), ..., (209,129)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9,10,11,12,13} y = {121, 129}
APA075	(1,33), (17,33), ..., (81,33) (1,41), (17,41), ..., (81,41)	x = 16*n+1; n= {0,1,2,3,4,5} y = {33, 41}
APA150	(1,49), (17,49), ..., (113,49) (1,57), (17,57), ..., (113,57)	x = 16*n+1; n= {0,1,2,3,4,5,6,7} y = {49, 57}
APA300	(1,1), (17,1), ..., (113,1) (1,8), (17,8), ..., (113,8) (1,69), (17,69), ..., (113,69) (1,77), (17,77), ..., (113,77)	x = 16*n+1; n= {0,1,2,3,4,5,6,7} y = {1,8,69,77}
APA450	(1,1), (17,1), ..., (177,1) (1,8), (17,8), ..., (177,8) (1,69), (17,69), ..., (177,69) (1,77), (17,77), ..., (177,77)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9,10,11} y = {1,8,69,77}
APA600	(1,1), (17,1), ..., (209,1) (1,8), (17,8), ..., ((209,8) (1,101), (17,101), ..., (209,101) (1,109), (17,109), ..., (209,109)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9,10,11,12,13} y = {1,8,101,109}
APA750	(1,1), (17,1), ..., (241,1) (1,8), (17,8), ..., (241,8) (1,133), (17,133), ..., (241,133) (1,141), (17,141), ..., (241,141)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15} y = {1,8,133,141}
APA1000	(1,1), (17,1), ..., (337,1) (1,8), (17,8), ..., (337,8) (1,165), (17,165), ..., (337,165) (1,173), (17,173), ..., (337,173)	x = 16*n+1; n= {0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18,19,20,21} y = {1,8,165,173}

Programming

ProASIC and ProASIC^{PLUS} devices both use the JTAG pins TCK, TMS, TDI, and TDO for programming. During migration from ProASIC to ProASIC^{PLUS}, you do not have to change these pins as they occupy the same locations. For ProASIC^{PLUS} devices, both V_{DDP} and V_{DD} supply power to the programming circuit, while for ProASIC only V_{DDP} supplies the programming circuit. Also, ProASIC^{PLUS} devices do not require any plug-in connector (needed in ProASIC) to prevent the user from unintentionally programming the device while the board is powered. Both ProASIC and ProASIC^{PLUS} support In-System Programming (ISP). However, the ProASIC^{PLUS} solution has many enhancements over ProASIC ISP. Please see Actel's *In-System Programming ProASIC^{PLUS} Devices* and *In-System Programming ProASIC Devices* application notes for details.

Conclusion

Actel's ProASIC^{PLUS} family shares numerous architectural features with its predecessor, the ProASIC family, and offers higher speed, expanded I/O standard support, and special clock conditioning PLL circuitry. By understanding the differences between the two families, migration from ProASIC to ProASIC^{PLUS} is possible.

Related Documents

Datasheets

ProASIC 500K Family

http://www.actel.com/documents/ProASIC_DS.pdf

ProASIC^{PLUS} FPGA Family

http://www.actel.com/documents/ProASICPlus_DS.pdf

Application Notes

Using ProASIC^{PLUS} Clock Conditioning Circuits

http://www.actel.com/documents/APA_PLL_AN.pdf

In-System Programming ProASIC^{PLUS} Devices

http://www.actel.com/documents/APA_External_ISP_AN.pdf

In-System Programming ProASIC Devices

http://www.actel.com/documents/A500K_ISP_AN.pdf

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (5192718-1/5.07*)	Page
5192918-0/7.02	In Table 5, J15 was changed from AGND to AVDD for the ProASIC^{PLUS} FG256 devices.	5

Note: **The part number is located on the last page of the document.*

www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

5192718-1/5.07