3200DX Dual-Port Random Access Memory (RAM)

With the dramatic changes in the processing power of microprocessors and microcontrollers, peripheral components and systems have become the bottleneck of system performance. An efficient peripheral system must be capable of transferring data in high-speed bursts. Thus, the CPU can optimize the system performance by accessing the system bus with minimal interruption. A common method of increasing data throughput to an I/O interface while minimizing CPU wait states is to use first-in-first-out (FIFO) queues to buffer transferred data between the host bus and the peripheral systems. Some common applications using FIFO buffers are SCSI and IDE interfaces, bus-width conversion applications (e.g., 8-bit to 32-bit conversions), and asynchronous transfer mode (ATM) network interface cards. Typically, FIFOs are either implemented in discrete logic devices or designed using standard dual-port RAM devices with the RAM control logic implemented in PALs or PLDs.

The 3200DX family provides for a system's memory needs by supplying blocks of synchronous dual-port SRAM (Figure 1). Other FPGAs offer memory, but at a high cost of using their SRAM programming elements. Using the SRAM programming elements depletes the already constrained routing resources.

The 3200DX family offers dual-port SRAM capable of supporting a system speed of 100 MHz. The SRAM comes in blocks with a selectable 32 x 8-bit or 64 x 4-bit configuration. Designers can also connect the SRAM blocks to build wider (x16, x32, etc.) or deeper (128, 256, etc.) banks of memory. The block structure of the 3200DX SRAM makes it particularly suitable for data-path designs, in which packets of data must be handled as a unit.

The SRAM of the 3200DX family offers dual independent read and write ports. The dual-port structure makes the memory suitable for FIFO applications such as telecommunication framers. Because the two ports have independent clocks, the memory can also serve in video and graphics applications, in which data arrives in bursts and is read out at a steady rate. Furthermore, the SRAM blocks will be fully supported by Actel's macro builder, ACTgen. Using ACTgen, the user can generate parameterized dual-port memory and FIFO blocks simply by clicking menu selections.

Figure 1 shows the 3200DX dual-port SRAM block interface. Each RAM block contains 256 bits. These 256 bits can be configured as 32 bytes (32 x 8), or as 64 nibbles (64 x 4). The following is a brief functional overview of the 3200DX SRAM blocks.

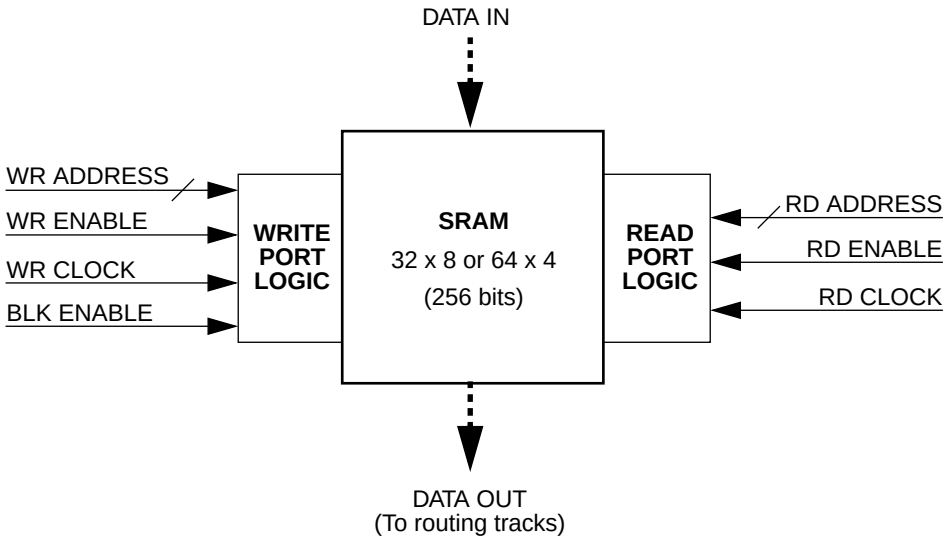

Figure 1 • *3200DX Dual-Port SRAM Block Interface*

Write Operations

The write port is always synchronous. Data is written into the RAM on the rising edge of the write clock (WCLK) whenever BLKEN (block enable) and WEN (write enable) are both active. WCLK and BLKEN have polarity selection. Write addresses (WRAD[5:0]), write data (WD[7:0]), BLKEN, and WEN are synchronized to the appropriate edge of WCLK. The RAM block may function in byte mode (32x8) or in nibble mode (64x4). In byte mode, WRAD5 is not used, since 5 bits can address the 32 bytes of each block. In nibble mode, WRAD5, is used and the data inputs are connected in pairs (WD0 and WD4 to LSB, WD1 and WD5 to next-higher-order bit, etc.).

The SRAM blocks can be cascaded together to create deeper blocks of memory. To cascade the SRAM blocks, one block is configured as active HIGH BLKEN, with the other active LOW, and the two BLKEN input then becomes a seventh address bit. Write operations will occur to the lower block when BLKEN = 0 and to the upper black when BLKEN = 1. WEN, always active HIGH, can be used to disable writes to both blocks.

Read Operations

There are two modes of operation at this port. In synchronous mode, read addresses (RDAD[5:0]) are synchronized to the read clock (RCLK), and the outputs change in response to a rising or falling edge of this clock. In asynchronous mode, outputs (RD[7:0]) change in response to a change of RDAD (Read Address). Read operations occur on RCLK or RDAD and change whenever REN is HIGH. When REN is LOW, the current state of the output is held.

Table 1 summarizes the 3200DX family features, including the dual-port SRAM in each device.

How to Use the 3200DX RAM Blocks

The best way to take advantage of the 3200DX dual-port RAM blocks is through Actel's macro builder, ACTgen. Refer to the *FPGA Application Guide* for a detailed description and examples.

RAM blocks can be instantiated in schematics similar to other library elements. There are 12 library elements that can be used to instantiate a RAM block in schematic. These elements are listed in Table 2.

Table 1 • *3200DX Family*

	3265DX	32100DX	32140DX	32200DX	32300DX
SRAM bits	0	2,048	0	2,560	3,072
Global Clocks	2	2	2	2	2
Quadrant Clocks	0	4	0	4	4
I/O_{max}	126	152	176	202	250
Wide Decode Cells	20	20	24	24	28
JTAG	No	Yes	Yes	Yes	Yes

Table 2 • *Library Elements Mapping into RAM Blocks*

Macro Name	Mode	Write Clock Edge	Read Clock Edge	Read Operation
RAM4RA	Nibble	Rising	NA*	Async
RAM4FA	Nibble	Falling	NA	Async
RAM4RR	Nibble	Rising	Rising	Sync
RAM4RF	Nibble	Rising	Falling	Sync
RAM4FR	Nibble	Falling	Rising	Sync
RAM4FF	Nibble	Falling	Falling	Sync
RAM8RA	Byte	Rising	NA	Async
RAM8FA	Byte	Falling	NA	Async
RAM8RR	Byte	Rising	Rising	Sync
RAM8RF	Byte	Rising	Falling	Sync
RAM8FR	Byte	Falling	Rising	Sync
RAM8FF	Byte	Falling	Falling	Sync

*NA: Not Applicable due to asynchronous read operation.