System Power Optimization Controller Using IGLOO FPGAs

Introduction

Actel has introduced its new low power IGLOO® family, based on the third generation Flash-based ProASIC®3 FPGA architecture. Actel IGLOO low power features and small footprint package address the needs of the growing portable electronics market. These portable, battery-operated devices now include more features at a higher level of performance and have a longer battery life—all of which is contained in an ultra-thin package that meets the demands of today's users. Actel IGLOO FPGAs offer portable device designers the flexibility of an FPGA with the static and dynamic low power features of an ASIC.

Actel IGLOO FPGAS can be used in numerous portable applications, particularly as a system power optimization controller. The system controller monitors the system events and manages the power usage for optimization. Since Actel IGLOO FPGAs offer a dynamic power less than 50% of the 1.8 V low power PLD alternative, IGLOO devices used as system controllers can run continuously in the system at a low 32 kHz frequency to reduce the overall power consumption even further.

Target Applications

- SmartPhones
- Digital cameras
- Portable media players
- PDAs
- Wireless gadgets
- Portable printers
- RFID readers
- Portable test and measurement equipment
- Point-of-sale

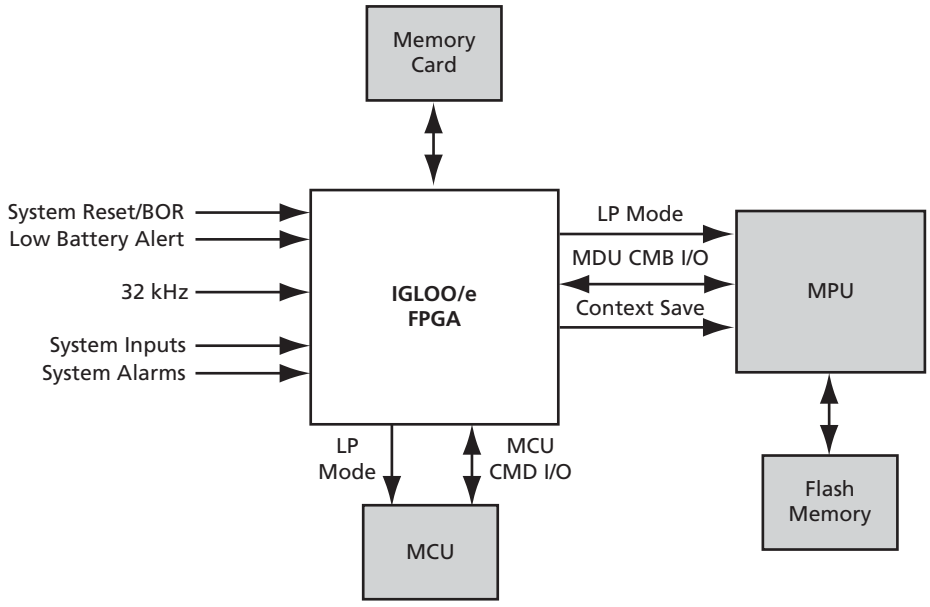

Figure 1 • **System Power Optimization Controller Application Diagram**

The Actel IGLOO Advantage

The Actel IGLOO FPGA is a full-featured FPGA with on-chip nonvolatile (Flash) memory, true dual-port SRAM memory, PLLs, and 19 I/O standards. It has a core voltage of 1.2 V/1.5 V to minimize the dynamic power and eliminate the need for an additional DC/DC converter. In addition, IGLOO FPGAs offer several low power modes, each designed to address the individual needs of an application.

- Flash*Freeze technology enables easy entry and exit from the static low power mode where IGLOO consumes as little as 5 µW while retaining the contents of the system memory and data registers.
- Sleep (and shutdown) mode allows for the IGLOO FPGA core power supply (or all power supplies) to be powered down when functionally not required while the rest of the system remains powered.
- The user low static ICC macro (ULSICC) reduces IGLOO FPGA dynamic and static power consumption.

Implementation

The system power optimization controller can be designed to manage the critical activities in the system while the higher power consuming devices in the system, such as the system microprocessor (MPU) and/or microcontroller (MCU), are placed in low power sleep/shutdown mode. The system controller will remain active at all times so that the system's critical events are not missed. The system controller is then tasked to monitor the following system events:

- Low battery level alerts and other system alarms
- System reset and brown-out resets (BOR)
- Memory extension card plug and unplug activity
- User I/O (such as button presses, etc.)

Figure 2 illustrates a block diagram of the system controller design, which includes an optional IDLE timer with a multi-input wake-up circuit for additional power savings.

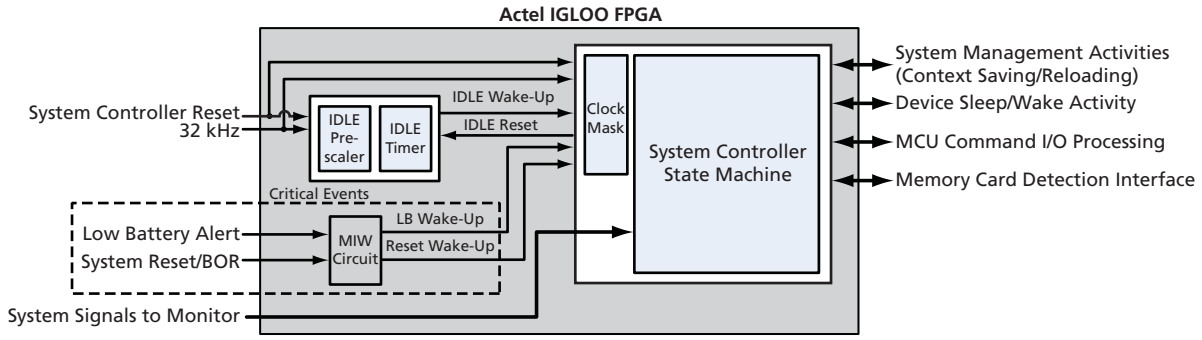

Figure 2 • **System Controller with IDLE Timer Block Diagram**

Once the system controller detects an event that must be processed (for example from user I/O), the appropriate system device is taken out of low power mode for event processing. After the event is processed or is flagged via handshaking logic, the device is then returned to low power mode. This activity helps to optimize the overall power usage, keeping the system devices in an active state only when needed.

In the case of system critical events such as a low battery alert, system reset, or BOR, the system controller must place all managed devices in low power mode. However, it must first preserve the critical system data (by performing a context-save) to Flash memory. Once the system recovers, the system controller may then restore all context data during the boot stage so that the system can resume normal functionality without losing its critical data.

The nature of the system controller is to remain active so that critical event can be processed. Actel IGLOO FPGA low dynamic power can be enhanced by enabling the ULSICC macro. The ULSICC macro, when

enabled, disables the FlashROM, reducing the overall power of the device. In addition, the IGLOO FPGA can be sourced by a low frequency clock (32 kHz), reducing the switching speed of the registers and thus reducing its power consumption. With a low frequency clock, the Actel IGLOO FPGA can continuously scan for external events and execute critical tasks or store the information to process once the system wakes.

If the application permits, a low power IDLE mode with multi-input wake-up circuit can also be implemented on an IGLOO FPGA to reduce the overall power consumption even further. The low power IDLE mode with multi-input wake-up circuit is comprised of a state machine, IDLE timer, and a multi-input wake-up (MIW) circuit. The entire design is meant to automatically or asynchronously wake the system controller from IDLE mode after a timer overflow or an external event has occurred. Once the state machine has detected that the last event has been processed, it will enter the IDLE state, which will mask the system clock, sourcing the other internal circuits and then enabling the IDLE timer. The IDLE timer will then run continuously until an overflow or wake-up event occurs. If no wake-up event occurs and the timer overflows, the device can then unmask the system clock, allowing the other circuits to process any noncritical events that may have occurred during IDLE mode. The multi-input wake-up circuit is designed to asynchronously wake the system from IDLE mode from an edge (rising or falling) of a critical input such as a low battery alert. The MIW circuit's output is synchronized to unmask the system clock, and then transitions the state machine from the IDLE state.

Conclusion

The system power optimization controller serves as the portal to the high power consuming devices in battery-operated portable device systems. The system controller must be active at all times so that critical events can be processed appropriately. In addition to managing the power usage, it can perform the system context saving so that critical data is not lost during a low battery event or an asynchronous system reset, for example. Actel IGLOO devices offer the flexibility of creating the necessary custom logic. They feature a low dynamic power with minimal cost to the overall system power consumption, and have the small footprint needed to implement the system power optimization controller for the battery-operated portable device. In applications that do not require real-time system monitoring, IGLOO FPGAs have the benefits of Flash*Freeze technology, which reduces the static low power consumption to as little as 5 µW. The Actel IGLOO system controller offers system designers the advantage of optimizing the power usage to extend the life of the battery and meet the growing demands of the portable electronics market.

Related Documents

Application Notes

IGLOO Flash FPGAs Brochure

http://www.actel.com/documents/IGLOO_PIB.pdf

White Papers

Reducing System Power

http://www.actel.com/documents/Reduce_System_Power.pdf

Datasheets

*IGLOO Low Power Flash FPGAs with Flash*Freeze Technology Datasheet*

http://www.actel.com/documents/IGLOO_DS.pdf

*IGLOOe Low Power Flash FPGAs with Flash*Freeze Technology Datasheet*

http://www.actel.com/documents/IGLOOe_DS.pdf

Refer to the Actel Libero® Integrated Design Environment (IDE), Designer, and SmartGen online help for more information.

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