

Power System Verification During Accelerated Life Testing

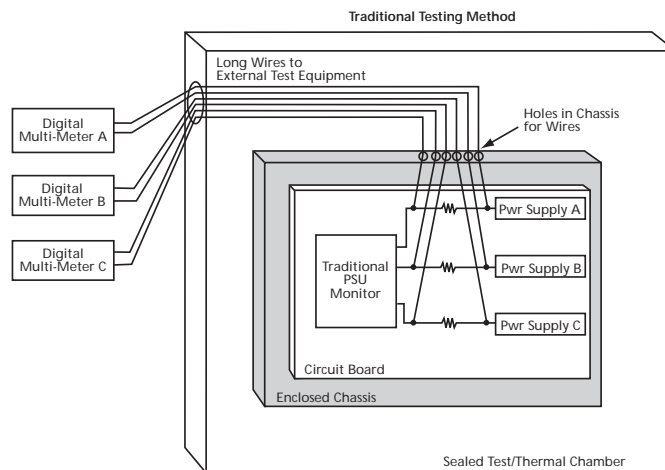
Table of Contents

Introduction	1
Advantages of Microsemi Fusion Analog Quad Technology	2
Conclusion	3
List of Changes	4

Introduction

Design verification of a power system during Accelerated Life Testing (ALT) and Highly Accelerated Life Testing (HALT) can pose many challenges to the design engineer (Figure 1). Critical signals might not be accessible when the board is being tested in a system. Test equipment might not be capable of functioning within specification at elevated temperatures or humidity, and remote monitoring through cables is often impractical. Further, traditional data-logging capabilities available during automated testing often do not capture all of the data needed to determine the root-cause of hardware faults.

Microsemi Fusion[®] Field Programmable Gate Array (FPGA) brings a whole new range of capabilities to bear on this problem. As the world’s first mixed-signal FPGA family, the Fusion family integrates mixed-signal analog, flash memory, and FPGA fabric in a monolithic device. Fusion offers a variety of mechanisms to capture and report critical data for power system verification and root cause analysis. This benefit goes beyond simple monitoring and reporting functions to include sophisticated system management and control function as well as traditional FPGA logic functions, giving the designer the ability to get double duty out of the device for no real incremental cost increase. Fusion devices enable the designer to be more efficient at the verification stage of development with less time spent on setup and troubleshooting board-level issues and more time available for analyzing test data.

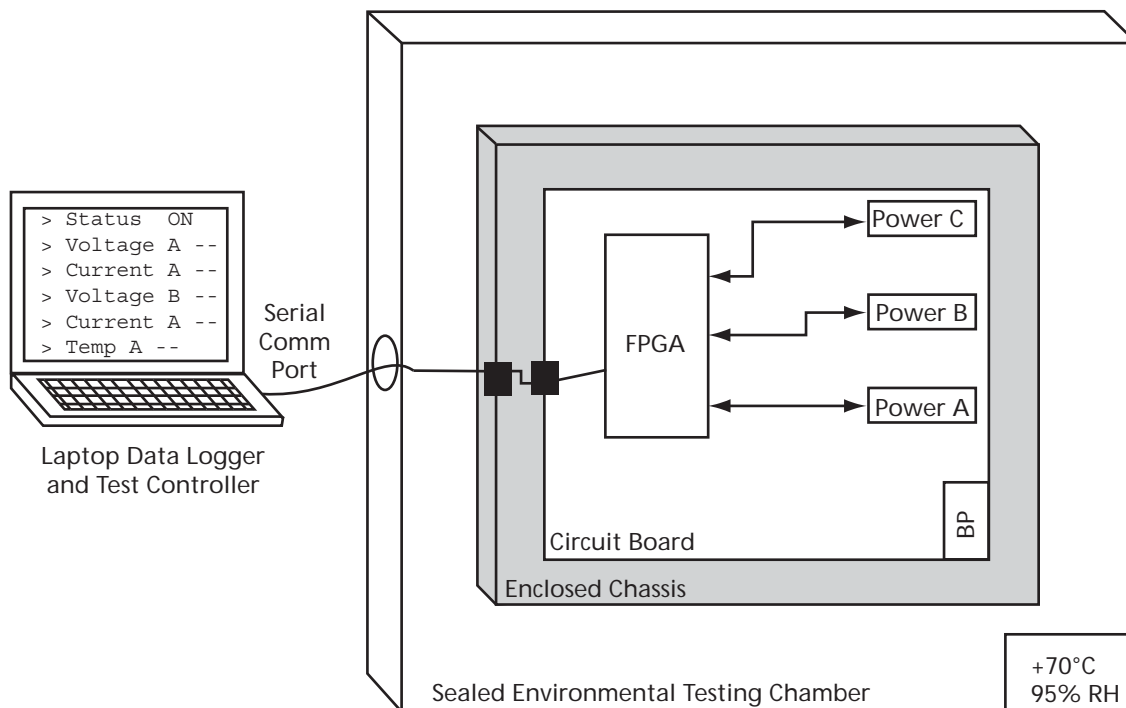


• Long wires and chassis contents have negative impact on test accuracy in a traditional (non-Fusion) test setup.

Figure 1 • Typical ALT Setup

Advantages of Microsemi Fusion Analog Quad Technology

The Fusion analog I/O structure, the Analog Quad, gives the designer access to voltage, current, and temperature measurements as well as a time stamp for easy data logging of various events within the design. This environmental data can be reported in real-time through a serial interface to a PC or recorded to the internal flash for recovery after testing or on demand (Figure 2).



- Emphasizes a design being tested at 70°C, 95% relative humidity. With no additional test equipment inside chamber and no long wires strung outside chamber to view and record voltage, current, or temperature data.
- Note that both environmental chamber and product chassis are sealed, with limited access to circuit board and components.

Figure 2 • ALT Test of System Using Fusion Mixed-Signal FPGA

Voltage and Current

With Fusion on-board, voltage and current measurements are made without external test equipment. Up to 30 separate voltages and 10 currents can be measured using a Fusion device. The designer does not need to run wires outside of a thermal chamber for voltage measurements and does not need to add wire loops for attaching current probes. This approach also eliminates errors due to noise induced on overly long lead wires, which can mask the issues needing review. Further, the designer need not risk placing test probes or test equipment within a thermal chamber that might be operating outside of the equipment's specified temperature range.

Temperature

With a dedicated thermal monitor block, Fusion requires only an external diode connected NPN transistor to measure temperature at any location on the board. Up to 10 separate temperature measurements can be made with a single Fusion device. This capability can give the designer access to temperature measurements at multiple locations on the board instead of relying on ambient temperature readings of the thermal chamber air. Soak times can be more accurately determined, since measurements at the board level can be made real-time and thermal sink areas in the chamber can be determined to optimize the thermal test. This capability can also be used to monitor for hot-spots on a board, or to individually monitor various devices to determine if air-flow or heat-sink area is adequate for processors or large datapath devices. With multiple temperature monitors designed onto the board, a designer can test a large number of boards without attaching thermocouples to each board. The extra sensors are easily depopulated to reduce cost for volume production.

Real-Time Counter (RTC) and Data Logging

Combining Fusion's integrated RTC and embedded flash memory allows the designer to record and recover operational performance data. The RTC supports multiple uses models, including the ability to preload the counter in order to synchronize the RTC, or leaving the RTC free running to measure total operational product life. Measured data can be written to the flash at predetermined intervals or can be written at the moment when a failure occurs. In the event of a hardware fault during ALT testing, the designer can recover the time-stamped voltage, current, and temperature conditions that existed just prior to the fault. This data improves the designer's ability to recreate the environmental conditions at the time of failure and perform root cause analysis on the board.

Beyond ALT and HALT testing, all of these test functions can co-exist with operational monitoring functions, control logic, and other FPGA functions within the Fusion device. With some planning, these monitoring, logging, and reporting functions can be used while the system is in normal service. Built-in test features used initially for design verification and characterization can then be used for in-situ diagnostics, either through a special data port made available to service technicians, or remotely through LAN access to the system.

Conclusion

The Microsemi Fusion FPGA gives the design engineer the ability to accurately monitor, control, log, and report on power system operation in a system or chassis when access to signals is limited. The Fusion FPGA can capture and report the data critical for power system troubleshooting and root cause analysis.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision	Changes	Page
Revision 1 (August 2015)	Non-Technical Updates.	N/A
Revision 0 (July 2007)	Initial Release.	N/A



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