

# Trainable Image Recognition System Using Low Power Flash FPGAs

## Introduction

Image recognition is a technology that can be used in a variety of applications. It is often used in medical imaging devices, security, defense video tracking, and factory automation. The typical image recognition system is powered by a microprocessor or digital signal processor (DSP). These image processors are limited to sequential image comparisons with a response time that increases exponentially with the number of image examples to compare. CogniSight™, a new trainable image recognition technology developed by General Vision, uses an artificial intelligence approach to video sensing, employing a parallel neural network inspired by the human brain and visual cortex.

General Vision's CogniSight Miniature Trainable Vision Sensor (MTVS) is targeted for battery-operated applications that sink less than 15 mA of current. The CogniSight MTVS captures and recognizes images at a rate of 60 images per second on a single board smaller than a matchbox, and its intelligence is neatly bundled in a single Actel low power Flash FPGA.

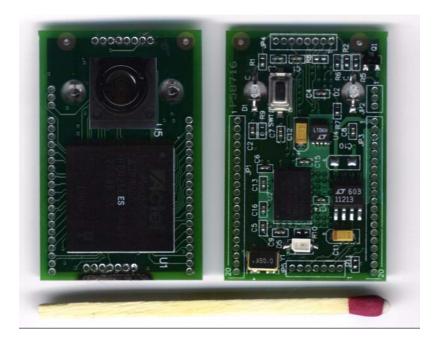


Figure 1 • CogniSight MTVS

# **Background**

CogniSight MTVS is trained by the user with General Vision's Image Knowledge Builder Tool via a USB connection to a PC. This tool collects the images and allows the user to categorize each image. A signature vector is extracted from the captured image and stored in the neuron memory during the training process. Once the recognition system has been trained, CogniSight MTVS operates on its own and compares the incoming image vector data with the data stored in neuron memory. It then uses a 16-bit output bus or the I2C interface to communicate with the main system application design to perform the desired tasks.

# **Implementation**

General Vision uses a third generation Actel Flash-based FPGA with one million system gates for the implementation of the digital image recognition system in the design. The image recognition engine consists of an image signature generator, the neural-network-based recognition engine, and an I2C-slave communication interface. The complete FPGA design consists only of an LVDS video connection port, two I2C communication ports, and 16 category output ports.

The recognition processing engine consists of the parallel neural network and the main decision logic. Each neuron is comprised of an SRAM memory cell with its own comparison logic. The comparison logic helps to determine if the incoming image vector data from the signature generator is similar to the one or more examples stored in its neuron memory during the learning process. Since the neuron comparisons are performed in parallel, the recognition engine has a constant response time independent from the number of examples to match. This allows for a lower clock frequency, reducing the overall power consumption of the device. The I2C interface is then used by the main system application to control and retrieve data from the CogniSight MTVS device. Refer to Figure 2 for more information.

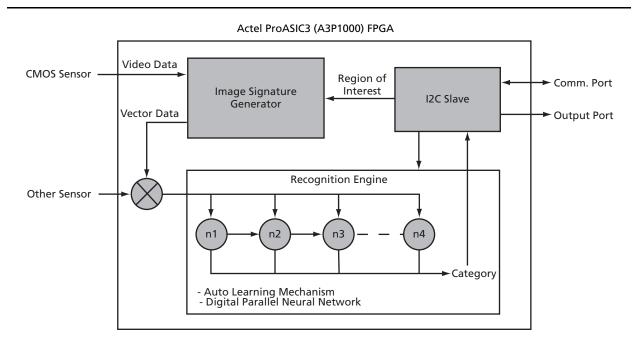


Figure 2 • Image Recognition System Engine FPGA Design



# **Portable Applications Using Image Recognition**

Image recognition can be used in multiple applications that utilize this effective technology. Below is a list of some of the applications:

- Industrial applications
  - Industrial inspection and sorting
  - Presence/absence, pass/fail
  - Alignment/positioning
  - Anomaly detection
- Security applications
  - Video surveillance
- Consumer applications
  - Learning systems, toys
  - Cellular phones
  - Smart appliances
- Automotive applications
  - Fingerprint recognition for security and personalizing
  - Passenger height detection for airbag safety

For some of these applications, portability and long battery life are key requirements; hence, power and size are extremely important features. Actel low power Flash FPGAs, IGLOO<sup>TM</sup> and ProASIC<sup>®</sup>3 devices, provide extremely low power—as low as 5  $\mu$ W. IGLOO devices also offer Flash\*Freeze<sup>TM</sup> mode capability, which allows the system to place the device in a low power mode while retaining SRAM and registers.

# The Benefits of Using Low Power Flash FPGAs

Actel Flash-based FPGAs offer a high performance, high security, and low power solution for General Vision's CogniSight MTVS Image Recognition design.

- The high performance of the device allows for the integration of the entire digital recognition engine within a single FPGA device, minimizing the number of components on the board.
- The device's low quiescent current provides added benefits, while offering a low power CogniSight MTVS battery-operated device.
- The small size SRAM memory arrangement in the Flash FPGA family is well suited for the neuron storage requirement of the CogniSight technology, making it an ideal solution when implementing the parallel neural network.
- The use of Flash\*Freeze mode results in power as low as 5  $\mu$ W in applications where extreme low power is a feature, thus prolonging the battery life.
- The small footprint packages (8×8 mm QN132 and 8×8 mm CS196) allow the integration of many features in a tiny, portable-friendly board.
- The FlashLock® feature of the Flash FPGA family offers General Vision the ability to secure the FPGA contents, protecting its innovative IP.

## **Conclusion**

Actel low power, Flash-based FPGAs offer a high performance, high security, and low power solution for the implementation of the Trainable Image Recognition design. This innovative technology implements an artificial intelligence approach to video sensing using a parallel neural network inspired by the human brain and visual cortex. The small size and low power of CogniSight MTVS make it an ideal solution for the growing image recognition needs of the automotive, consumer, security, and industrial markets. Actel low power Flash FPGAs offer necessary performance, features, and security, making them an ideal solution in implementing this unique technology.

## References

#### **Datasheet**

ProASIC3 Flash Family FPGAs Datasheet

http://www.actel.com/documents/PA3\_DS.pdf

IGLOO Low Power Flash FPGAs

http://www.actel.com/documents/IGLOO\_DS.pdf

CogniSight Miniature Trainable Vision Sensor (MTVS) Datasheet

http://general-vision.com/publications/CogniSight\_Core\_DS.pdf

## **Application Notes / White Papers**

ProASIC3/E Production FPGAs Features and Advantages White Paper

http://www.actel.com/documents/PA3\_E\_Tech\_WP.pdf

CogniSight™, Image Recognition Technology

http://general-vision.com/publications/CogniSight\_Techno\_Intro.pdf

Image Recognition Using Neural Networks

 $http://general-vision.com/publications/WP\_Image \% 20 recognition \% 20 using \% 20 neural \% 20 networks.pdf$ 

#### **User's Guides**

IGLOO FPGA Fabric User's Guide

http://www.actel.com/documents/IGLOO\_UG.pdf

ProASIC3/E Starter Kit User's Guide & Tutorial

http://www.actel.com/documents/PA3\_Startkit\_UG.pdf

SmartGen Cores Reference Guide

http://www.actel.com/documents/gen\_refguide\_ug.pdf

Fusion and ProASIC3/E Macro Library Guide

http://www.actel.com/documents/pa3\_libquide\_ug.pdf

CogniSight Image Knowledge Builder User Manual

http://general-vision.com/manuals/CogniSight\_IKB\_Manual.pdf

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